IMSAI

SIO 2

SIO 2 Board

FUNCTIONAL DESCRIPTION

The SIO Board provides a serial input/output capability for the IMSAI 8080 System. It contains two serial I/O ports, providing two complete RS232 full duplex data lines with all control signals. Data lines for both channels are provided in RS 232, TTL Level and current loop formats. Asynchronous or synchronous lines utilizing full or half duplex can be run with this board at any rate up to 9600 baud in the Asynchronous mode and 56,000 baud in the Synchronous mode.

The SIO Board may be jumper-selected to respond either to input and output instructions from the IMSAI 8080 System or to memory reference instructions for memory-mapped I/O.

Operation of the board requires 16 I/O port or address locations, which are selected by address bits 0 through 3. When the board is used with input and output instructions, address bits 4 through 7 form the remainder of the board address and are jumper selectable. When the board is used as memory-mapped I/O, the lower byte of address is jumper selected exactly the same as an I/O port address and the upper byte of address is hex FE or octal 376.

The SIO Board is structured around a pair of Intel 8251 USART (Universal Synchronous-Asynchronous Receiver-Transmitter) devices.

The 8251 chips provide for extensive program control of the input/output functions including the RS232 Control Line and sync character selection in the Synchronous mode and error condition sense and recovery. The board provides interrupt generation for received characters, empty transmitter buffers, and sync characters detected with provision for jumper selecting the priority of the interrupt. The interrupt works in conjunction with the Priority Interrupt/ Clock board (PIC-8).

All functions may also be program controlled so that the full capability of the board is available to the machine without the use of interrupts. All RS232 level drivers and receivers necessary for two complete RS232 lines are included on the board.

Control lines included are DSR, DTR, RTS, CTS, and Carrier Detect. RS232 level drivers and receivers are also provided for receive and transmit clocks for use in Synchronous Mode. Jumper options permit the SIO board to be used either as the receiving (terminal) end of an RS232 line, or as the originating (computer) end.

Jumper options are available so that the two serial I/O ports may be used together so that the control lines are connected together on the two ports and the data lines are received and originated by the 8251 USARTS.

This configuration permits breaking an existing RS232 line and inserting the IMSAI 8080 System between the ends so that the control signals pass straight through and the IMSAI 8080 System intercepts, processes, and retransmits the data. This configuration is extremely useful where format adaptation or other changes must be made to data travelling on RS232 Systems.

Jumper-selectable baud rates are provided on the board for standard asynchronous and synchronous rates up to 9600 baud asynchronous and up to 38,400 baud synchronous. Other rates may be obtained through the use of the SIOC board which contains a jumper-programmable divider which mounts directly onto the SIO Board.

The two output connectors on the top of the board are designed to use the 3M flat cable system to connect directly to 25 pin EIA connectors so that no hand wiring is required to either receive or originate an RS232 line.

TTL and current loop serial input and output are connected to unused pins on the input/output connector. TTL levels are available on the connector for DTR, DATAIN, and DATAOUT, to provide maximum flexibility and utility. A current source is available on the connector for use with current loops. Current loop driving is done through opto-isolators for complete isolation of current loop lines.

Integrated circuit power regulation is provided with high quality tantalum and disc ceramic by-pass capacitors. The board is made on G10-type, 1/16 inch laminate with contact fingers gold-plated over nickel for reliable contact and long life. The remainder of the circuitry is tin-plated for good appearance and reliable solder connections.

Plated through-holes eliminate the need for any circuit jumpers. All jumper options are provided in 16 pin dual in-line package patterns so that jumpers may be installed on headers plugged into IC sockets for convenient and quick changing.

SIO THEORY OF OPERATION

To enable the SIO board, it must be properly addressed. In the I/O port addressed mode, address bits A4 through A7 are jumpered to the 74LS30 (8 input NAND) in C8. The status bits SINP and SOUT are NORed, this intermediate value inverted, and applied (via jumper on D6) to another of the NAND inputs. Remaining NAND inputs in this mode are jumpered (via D6) to a +5 volt level. Thus, when the selected address appears on A4-A7, and the MPU sends a SINP or SOUT pulse, the NAND output goes low and the board is enabled. See schematic.

In the memory-mapped I/O mode, the jumpering in socket C7 still selects an address. The high-order address is interpreted in another 8 input NAND (D8), and hard-wired to respond to the hex value FE. The jumper in socket D6 should be wired to put the inverted output of D8 into an input of C8, and the NORed output of the status bits SINP and SOUT directly connected to the (C8) NAND's input.

The +5 volt tie line jumper in D6 should not be connected for memory-mapped I/O. In this mode, when the corrected high and low order bits are on A4 through A15, and the MPU does not send a SINP or SOUT pulse, the board is enabled. See Diagram.

The SIO board has a bi-directional data bus on the board which connects to the 8251 chips and to the input and output portion of the SIO board control port. The bi-directional bus is connected to the DATA IN and DATA OUT busses on the IMSAI 8080 back plane through 8216 bi-directional bus driver chips. The board enable signal selects these bi-directional bus driving chips and the processor's data bus in signal (DBIN) is used to determine the direction of driving of the bi-directional chips.

8T97's are used to gate the control port data on the bi-directional data bus on the board. They are enabled by the DBIN strobe from the processor and address bit 3.

The 4 output bits of the control port on the SIO board are latched into the 74177 which is clocked by a combination of board enable and address bit 3 and the write strobe either from the processor or from the front panel.

The 8251 chips are selected by address bits 1 and 2, respectively, with address bit 0 determining whether the chip is in control or data mode. The read and write strobes are supplied to complete the control, enabling the chip to read data or write data onto the bi-directional data bus on the board.

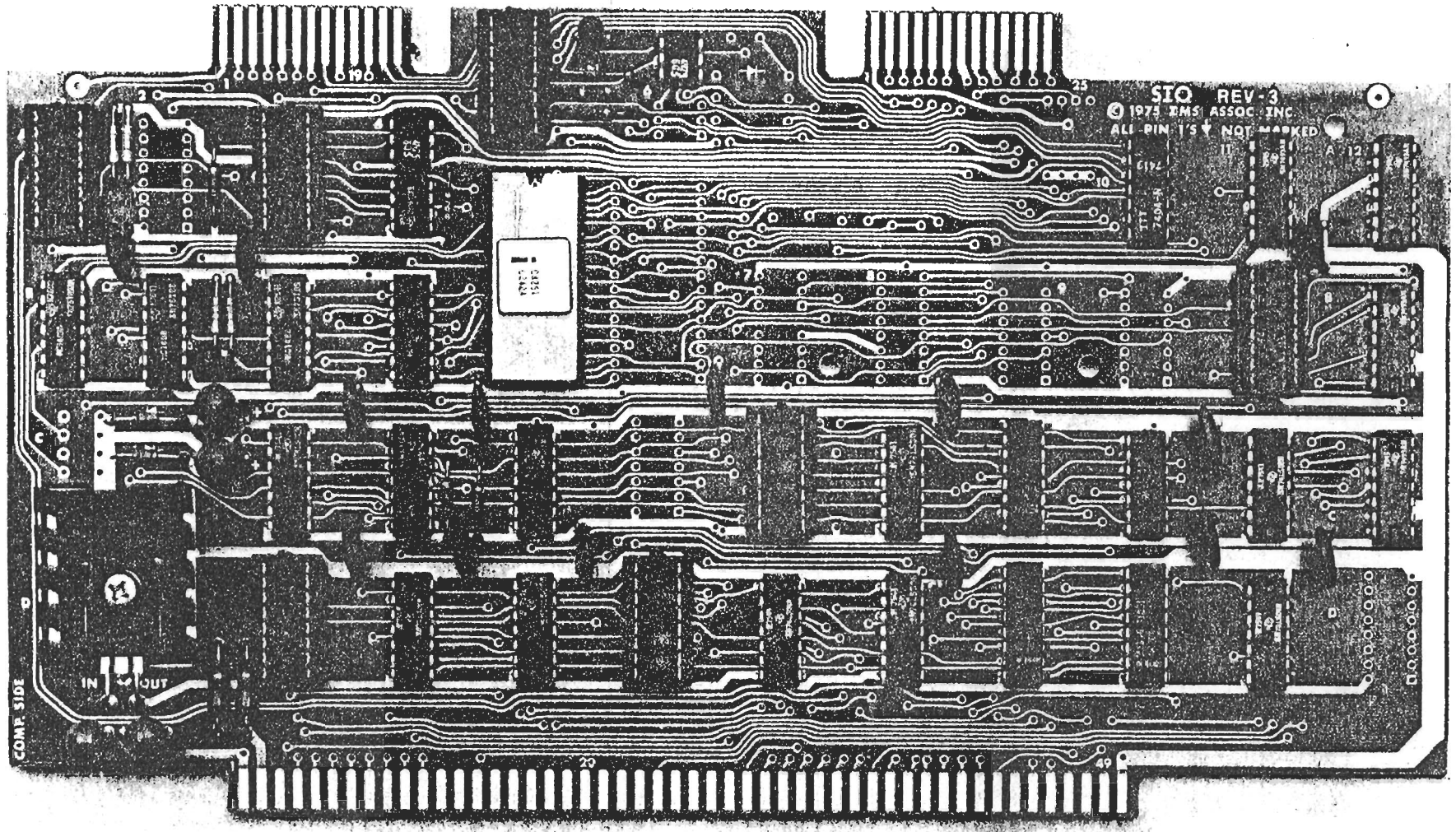
The four control lines desired for interrupt generation are ORed through 7425 and the resultant value supplied to an interrupt select jumper socket (D3). The 7425 OR gate may be disabled by two of the output port bits (IEA or IEB) when interrupts are not desired.

The two megacycle system clock phase II is divided to provide the standard baud rates for jumper selection to channel A and B. It is first divided by 13 through the use of a 7493 with external gating. This produces a rate extremely close to 16 times 9600 baud.

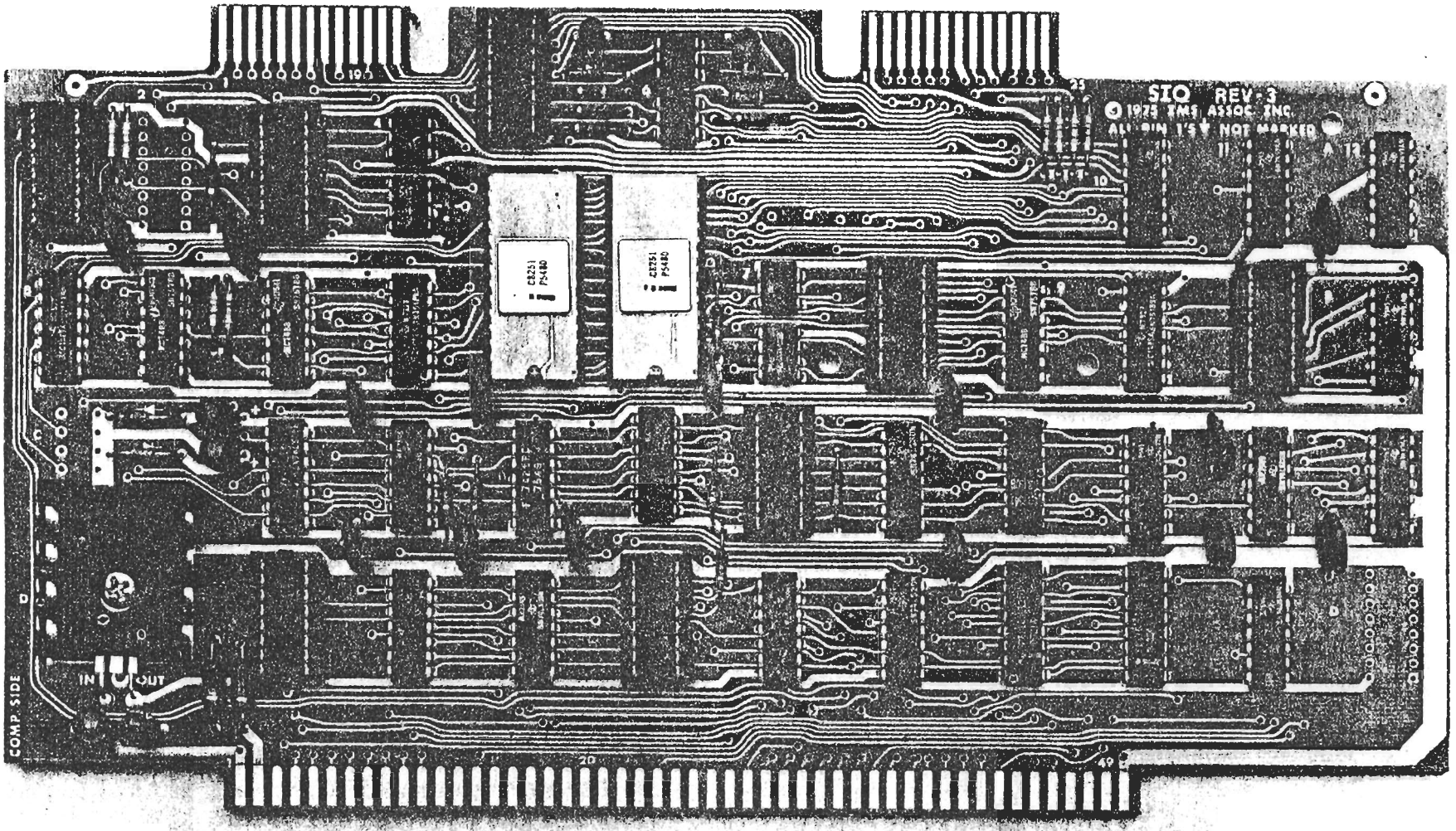
Further division of two are made by 7493's to provide most of the other standard baud rates. 110 baud for a standard teletype is achieved by a divide by 11 from the 2400 baud line which is then divided by 2 to create a symmetrical output and supplied to the jumper socket for 110 baud.

The phase II clock, +5 volts and ground are also supplied to the data rate select socket for use by the SIOC board which connects to the SIO board through the data rate select socket (B11) to provide a jumper-selectable baud rate generator for special rates.

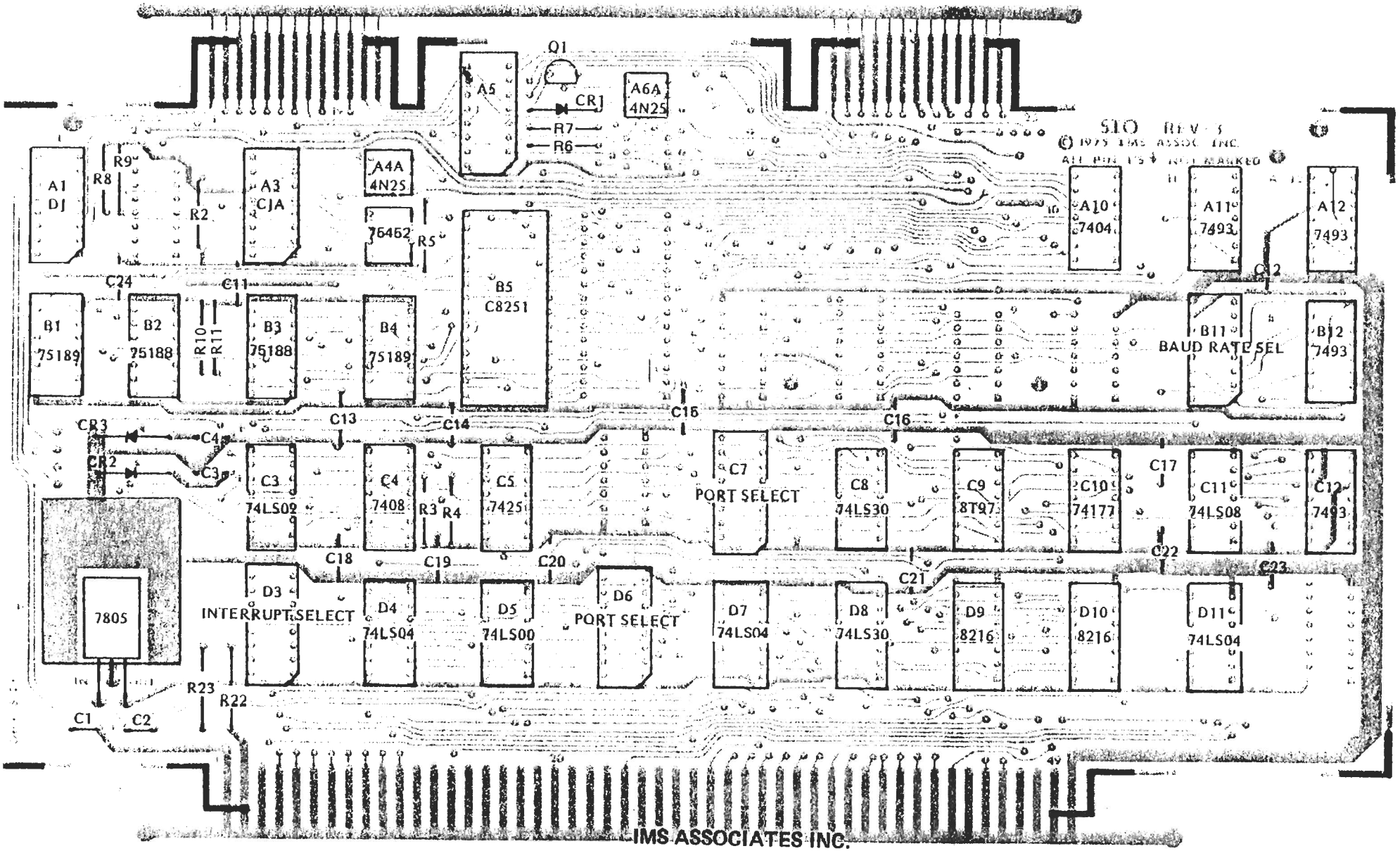
The data and control outputs of the 8251 chips are driven or received through 1488 or 1489 TTL to RS232 level converters as appropriate to the functions. The TTL levels for data and control are driven through open-collector peripheral drivers and a 220 ohm pull-up to +5 volts. The current loop input and output are driven through opto-isolators and are designed to work adequately with either 20 or 60 miliampere current loops.


SIO REV-3
© 1975 IMSAI ASSOC. INC.
ALL PIN 1'S NOT MARKED
COMP. SIDE
IN
OUT

SIO 2-1 REV. 3



SIO 2-2 REV. 3



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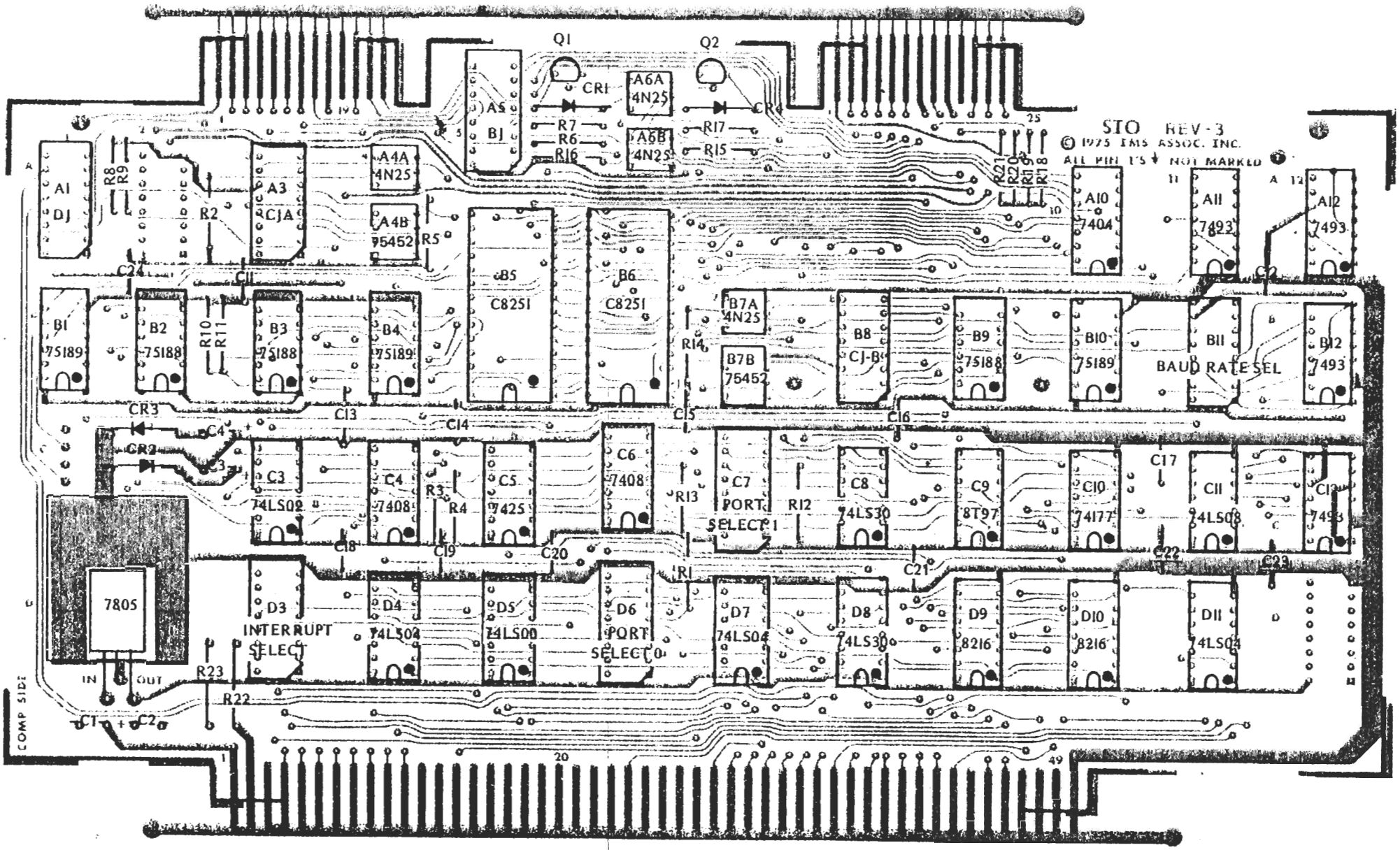
ASSEMBLY DIAGRAM
SIO 2-1 REV 3 2/76

5/18/76



IMS Associates Inc.

ASSEMBLY DIAGRAM

SIO 2-2 REV 3 2/76

SIO
Parts List
Revision 1

BOARD: SIO

Part#	Quantity	Description	Identifying Marks
741s00	1	Quad 2 Input NAND (Low Power Schottky)	SN74LS00N
741s02	1	Quad 2 Input NOR (Low Power Schottky)	SN74LS02N
7404	1	Hex Inverter	SN7404N
741s04	3	Hex Inverter (Low Power Schottky)	SN74LS04N
7408	2	Quad 2 Input AND	SN7408N
741s08	1	Quad 2 Input AND (Low Power Schottky	SN74LS08N
7425	1	Dual 4 Input NOR with Strobe	SN7425N
741s30	2	8 Input NAND (Low Power Schottky)	SN74LS40N
7493	4	4 Bit Binary Counter	SN7493N
74177	1	4 Bit Binary Counter-35 MHz	SN74177N
75188	3	RS 232 Driver	SN75188
75189	3	RS 232 Receiver	SN75189A
75452	2	Dual Peripheral Driver	SN75451BP
7805	1	5 V. Positive Voltage Regulator	MC7805CP
8216	2	Bi-directional Bus Driver	D8216/S1261
8251	1 on 2-1 2 on 2-2	Programmable Communication Interface	C8251
1n914	2	Silicon Diode	1N914 (blue/black)
2n3904	2	Transistor	2N3904
4n25	4	Opto-Isolator	4N25

SIO
Parts List
Revision 1

Part#	Quantity	Description	Identifying Marks
8t97	1	Hex Tri-State Buffer	N8T97B
dc-.1-30	14	Disk Capacitor	.1
h-hsto-220	1	Heat Sink	Thermalloy/6106B-14
ich-16	8	Integrated Circuit Header.	Numbered 1-16
pc-sio	1	Printed Circuit Board	SIO
r-56-1/2	2	56 Ohm, 1/2 Watt Resistor	green/blue/black
r-220-1/4	6	220 Ohm, 1/4 Watt Resistor	red/red/brown
r-470-1/4	8	470 Ohm, 1/4 Watt Resistor	yellow/violet/brown
r-1K-1/4	6 (7 for 2-2)	1K Ohm, 1/4 Watt Resistor	brown/black/red
r-4.7K-1/4	2	4.7K Ohm, 1/4 Watt Resistor	yellow/violet/red
sts-16	8	Solder Tail Socket	16 Pin Socket
tc-33-25	4	Tantalum Capacitor	33-25
z-12-1	2	Zener Diode	1N4/742
s/n/lw	1 ea.	5/16" screw/nut/lockwasher	
solder			
sts-28	1 2(for SIO 2-2)	Solder Tail Socket	28 Pin Socket
12" Wire Wrap Wire	7		

ASSEMBLY INSTRUCTIONS

Assembly of the SIO board is straightforward and should be conducted in the normal sequence as described on the general instructions for assembly. That is, insert the resistors, one value at a time, check their position and solder in place. Next, insert 2 12-volt zener diodes near position C2. Check for proper orientation (cathode is the banded end) and location, and solder.

Then insert the integrated circuit-chips with the exception of the 8251's. Double check them to make sure that Pin 1's are in the right direction, and that all pins are correctly inserted through the board. All pin 1's on this board are inserted toward the bottom of the board towards the 100 pin edge connector. After checking, the IC's can be soldered in place.

The two 25 pin sockets for the 8251's and the sockets in positions D3, D6, C7, A1, A3, B8, and A5, can be inserted and soldered in place.

The .1 mf disc ceramic capacitors can be inserted in place, checked as to correct locations, and soldered.

Next, fasten the 7805 regulator and heat sink to the board with #6 screw, nut and lockwasher. Solder the regulator pins in place. Install 4 tantalum .33 uf capacitors. Check for proper polarity (+ to +), check for proper location, and solder.

Finally, the 8251 chips should be inserted in their sockets with Pin 1 down toward the 100 pin edge connector at the bottom of the board. Addressing and baud rate jumpers should be installed and other option jumpers installed as required. The board is ready for use.

USER GUIDE

The IMSAI SIO Board provides 2 independent channels of serial data input and output. Utilizing the Intel 8251 USART devices, the SIO Board provides 2 channels of RS232, TTL, and current loop data lines with complete control signals.

The SIO Board also includes all logic necessary to control the 8251 devices from the IMSAI 8080 Back Plane.

For reference information on the programming and operation of the 8251 chip, the user should refer to the Intel 8080 Microcomputer Systems User's Manual.

The User's Guide is intended to cover the information beyond that contained in the Intel Data Book necessary to make full use of the SIO board.

Both the memory-mapped and jumper-wired I/O configurations use the lower 4 bits of the address bytes (A1 through A3) to select and control the board's functions. Bit 4 through 7 of the board address (A4 - A7) are jumper-selected as described on another page. If the board is jumper-selected to run as an input and output port type board, then A0 - A7 form a complete address. If the board is jumper-selected to respond to memory-mapped I/O, then A0 - A7 form the lower byte of address and the upper byte of address is hex FF or octal 376.

Address bits 1 and 2 select serial I/O channel A or channel B respectively. That is, when address bit 1 (A1) is high, serial I/O channel A is enabled. When address bit 2 (A2) is on, serial I/O channel B is enabled.

Address bit 0 determines whether the I/O channel selected will respond to the current byte as a control byte or a data byte. If address bit 0 is a 1, the control functions are selected, and if address bit 0 is a 0, the byte is assumed to be data. Thus, to write a control byte into serial I/O channel A, the lower 4 bits of address would normally contain hex 3 or octal 03, while the normal address

SIO BOARD ADDRESSING

Address Bit	Function	
0	C/$\overline{D}$ on 8251's	1 = CONTROL 0 = DATA
1	SELECT CHANNEL A	1 = SELECT
2	SELECT CHANNEL B	1 = SELECT
3	SELECT CONTROL I/O	1 = SELECT
4	CARD ADDRESS	
5	Jumperable to any one of 16 addresses	
6		
7		

This byte is I/O port address to run SIO card from INP & OUT instructions.

If SIO card is to be run from memory reference instructions (memory mapped I/O), the above byte is the low order address byte; the high order address byte is FE_{hex} (376_{octal}) (1111 1110 $_{binary}$)

SIO CONTROL I/O BIT DEFINITIONS

Bit	Input Byte	Output Byte
0	always 1	Interrupt Enable chan. A
1	always 1	Carrier Detect chan. A
2	Carrier Detect chan. A	non - functional
3	Clear To Send chan. A	non - functional
4	always 1	Interrupt Enable chan. B
5	always 1	Carrier Detect chan. B
6	Carrier Detect chan. B	non - functional
7	Clear To Send chan. B	non - functional

Carrier detects need option jumper to select originate/receive

Interrupts occur on TxRDY, TxEMTY, RxRDY, and SYNDET

TxRDY and RxRDY interrupts are removed if the respective functions (transmit and receive) are disabled by software command byte. TxEMTY interrupt is removed only by filling transmit buffer with a byte. This may be done while the transmit function is disabled .if desie

for channel B control bytes would be hex 5 or octal 05. Address bit 3 (A3) selects the board control I/O port. When address bit 3 (A3) is high, the control port will be enabled. Thus, when use is being made of the control port, the lower 4 bits of address would normally be hex 8 or octal 10.

The control I/O byte selected by address bit 3 is divided into the upper 4 bits and the lower 4 bits. The lower 4 bits, 0 through 3, serve the channel A serial I/O circuit. The upper four bits, 4 through 7, serve the second I/O channel B functions. Bits 0 and 4, for channel A and B respectively, control the interrupt enable separately for each channel. When this bit is a 1, the interrupts are enabled and the processor will receive and interrupt whenever any one of the following 4 lines are active: the transmitter ready line, the transmitter empty line, the receiver ready line, and the sync detect line.

If bits 0 or 4 (as appropriate to channel A or B) are made 0, then no interrupts will be generated from the affected channel. Bits 1 and 5 serve channel A and B, respectively, to output the carrier detect signal. This is operative only when the jumper in jumper socket BJ has selected the board to act as the originator of the carrier detect line.

Bits 2, 3, and 6, and 7 are not functional in the output mode for the SIO control byte. When an input is read from the SIO control byte, bits 0, 1, 4 and 5 are not functional. These 4 bits will always be read as a 1.

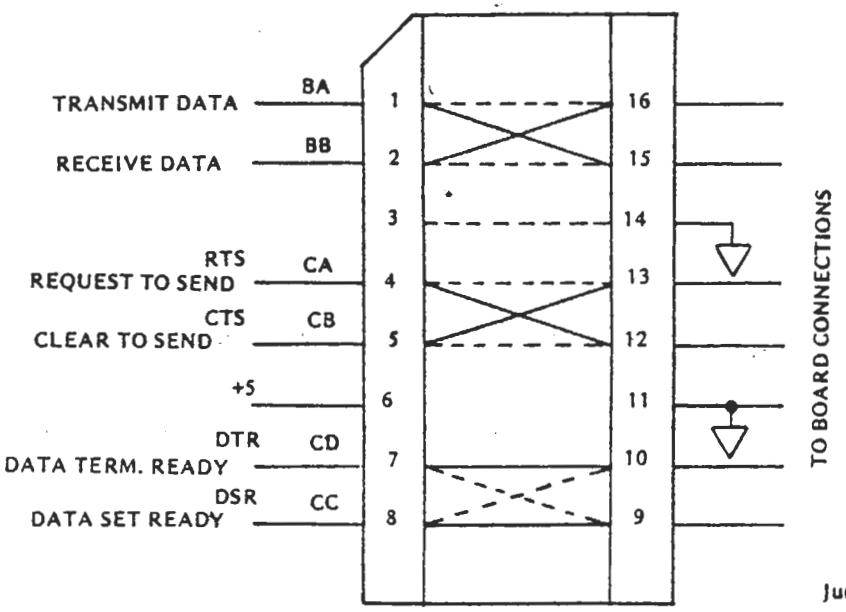
Bits 2 and 6 read the condition of the carrier detect receiver for channels A and B, respectively. The signal is operative only when jumper socket BJ is jumpered to read the condition of the carrier detect line.

Bits 3 and 7 serve channel A and B, respectively, to read the condition of the clear-to-send (CTS) control signal. This is provided because it is not possible to read the condition of CTS through programmed input from the 8251.

SIO BOARD I/O PIN DEFINITIONS

EIA 25 pin connector	26 pin edge connector	RS232 LEVELS	TTL LEVELS	CURRENT LOOP
1	1	AA chassis ground		
2	3	BA Trans. Data		
3	5	BB Rec. Data		
4	7	CA Req. to Send		
5	9	CB Clr. to Send		
6	11	CC Data Set Rdy.		
7	13	AB signal ground		
8	15	CF Carrier Det.		
9	17	+ V		+ V + Current Source
10	19			
11	21			In Loop +
12	23			Out Loop +
13	25			Out Loop −
14	2		$\overline{\text{Data Term. Rdy.}}$	
15	4	DB Trans. Clk.		
16	6		$\overline{\text{Data Set Rdy.}}$	
17	8	DD Rec. Clk.		
18	10		$\overline{\text{Data Out}}$	
19	12		$\overline{\text{Data In}}$	
20	14	CD Data Term. Rdy.		
21	16			Current sink 1
22	18			
23	20			Current sink 2
24	22			
25	24			In Loop −

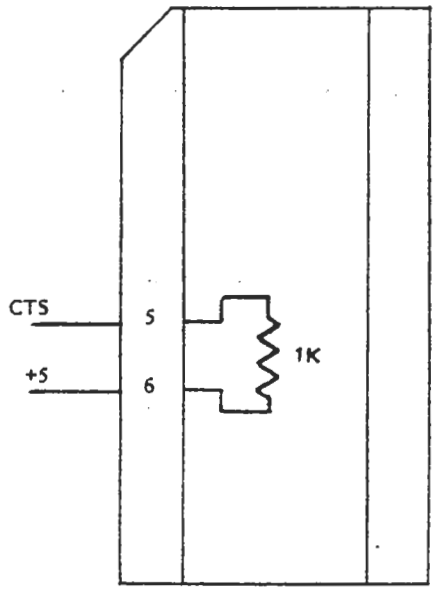
RS 232 OPTION



LOCATIONS A3 CHANNEL A
B8 CHANNEL B

Jumpers shown for connection as terminal or computer end of an RS232 line.
Jumper connection 3 to 14 is always to be made.

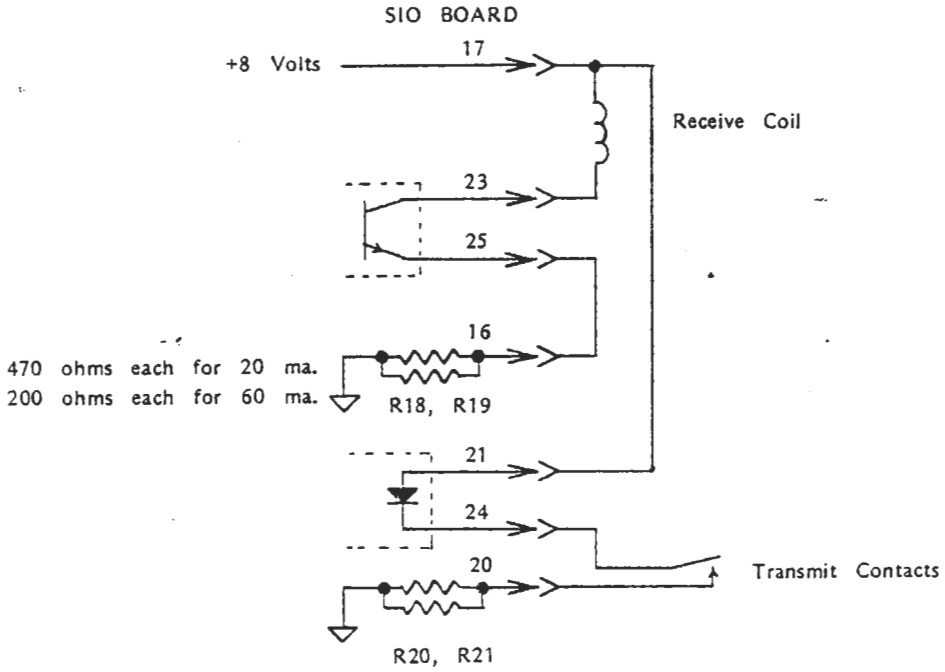
TERMINAL ——·
COMPUTER ——



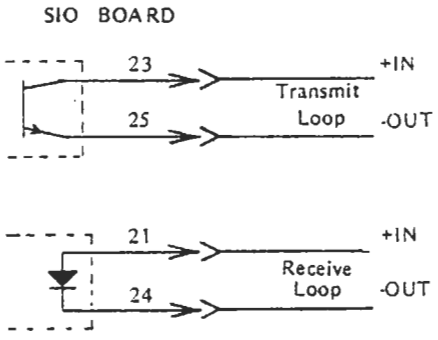
CURRENT LOOP OPTION

CURRENT LOOP CONNECTIONS

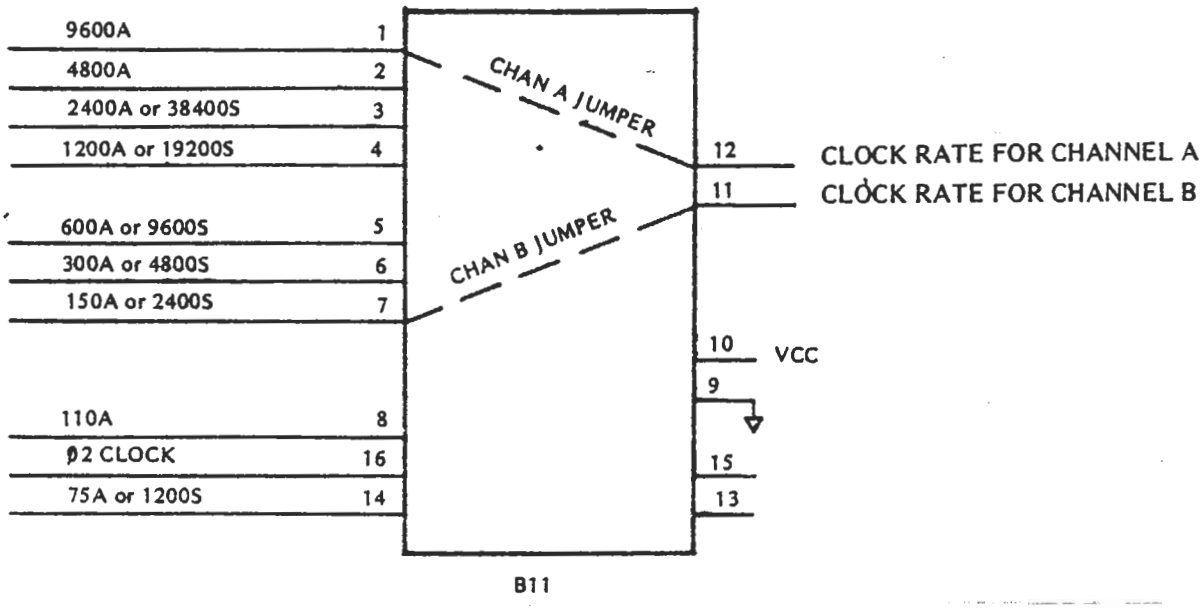
WITH CURRENT SOURCE



WITHOUT CURRENT SOURCE



BAUD RATE SELECT JUMPER DIAGRAM



TO SELECT A DESIRED BAUD RATE SIMPLY JUMPER IT ACROSS TO THE DESIRED CHANNEL

THE SUFFIX

S= SYNCHRONOUS
A= ASYNCHRONOUS

EXAMPLE SHOWS: 9600 ASYNCHRONOUS TO CHANNEL A
150 ASYNCHRONOUS OR 2400 SYNCHRONOUS TO CHANNEL B

The TTL output levels are driven by a 75452 dual peripheral driver, with open collector outputs, and a 220 ohm pull-up to +5 volts. The TTL data inputs drive 1TTL input load and a 1K pull-up to +5 volts.

When the TTL inputs are not being used, they should be left open or held high so as not to affect data input from other sources.

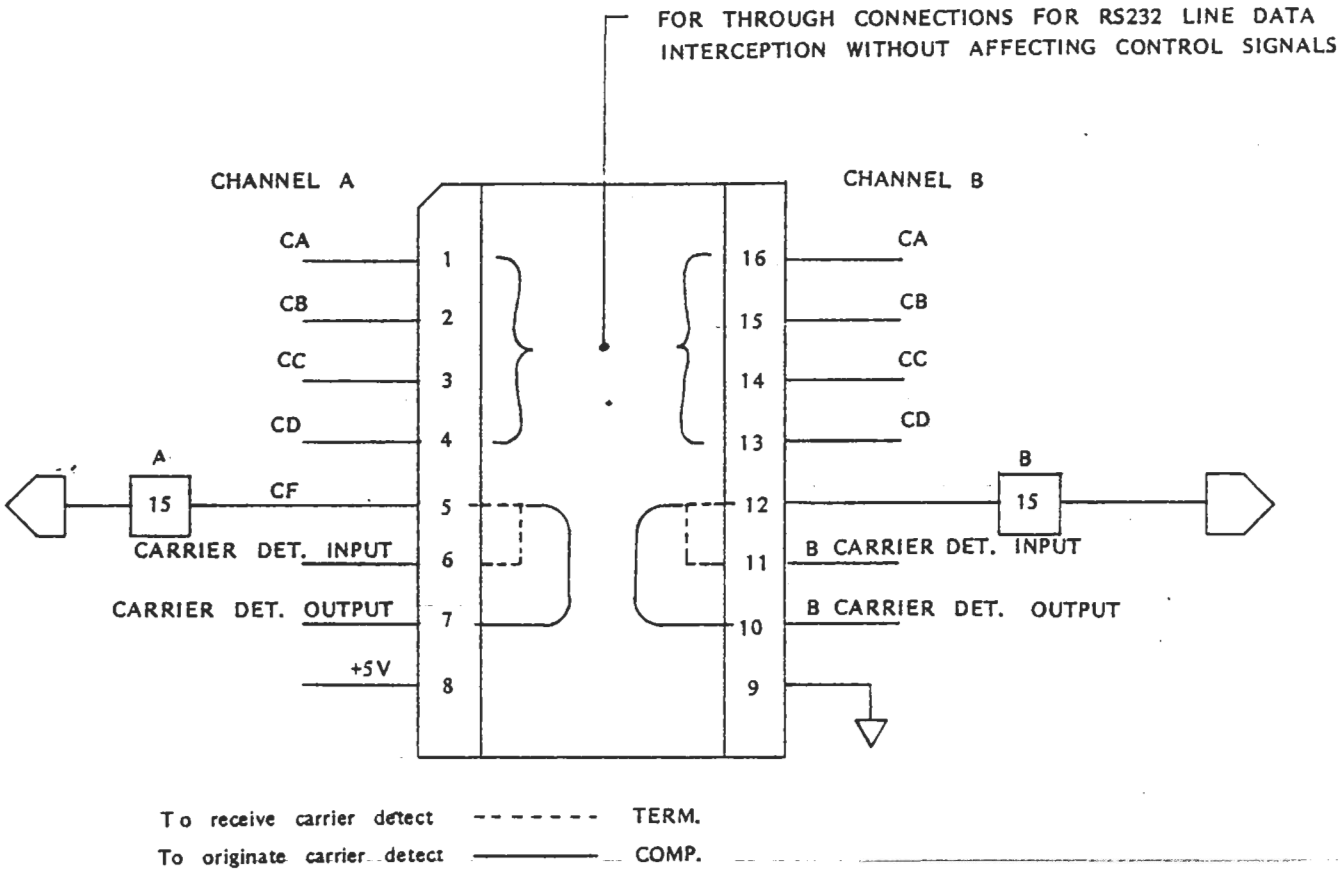
The TTL Data Input line must be left open and not held high when the current loop inputs are used. The current loop input drives opto-isolators and will respond to either 20 or 30 milliamperes. In applications where a significant reverse voltage may be experienced, such as when inductive circuits (i.e., relays) are coupled to the data line, a protective diode should be put across the line such that any reverse voltage spikes will cause the diode to conduct and thus protect the LED in the opto-isolator from too large a reverse voltage.

The current loop output is switched by an isolated transistor through an opto-isolator and is provided with a transient-shunting diode across the output transistor so that it may be used to drive relays without risk of damage to the output circuit. Typical wiring connections are diagramed on another page, both with and without the current source being used.

Setting the baud rate for serial I/O channels A and B is done on the jumper select socket RJ in position B11. The baud rates designated on the detailed sheet for rate select are correct when the 8251 is programmed for a 16X asynchronous clock rate and a 1X synchronous clock rate.

The details of selecting the desired baud rates are located on the schematic.

SIO RS232 INTERCHANNEL CONTROL JUMPERS and CARRIER DETECT



Jumper CJ-A or CJ-B

The jumper selection socket in A3 serves serial I/O channel A and the jumper selection socket in B8 serves serial I/O circuit B. Their functions are the same for their respective channels. The function of this jumper socket is to permit the serial I/O port RS232 levels to be wired so as to either serve as the terminal end of a 232 line or the computer end of a 232 line with no special cable wiring required off the Serial I/O board.

With pins 1, 2, 4, 5, 7 and 8 wired directly across the jumper socket as shown in the diagram for the terminal end, the function of the lines correspond one to one with the names of the RS232 control lines referred to in the 8251 specifications.

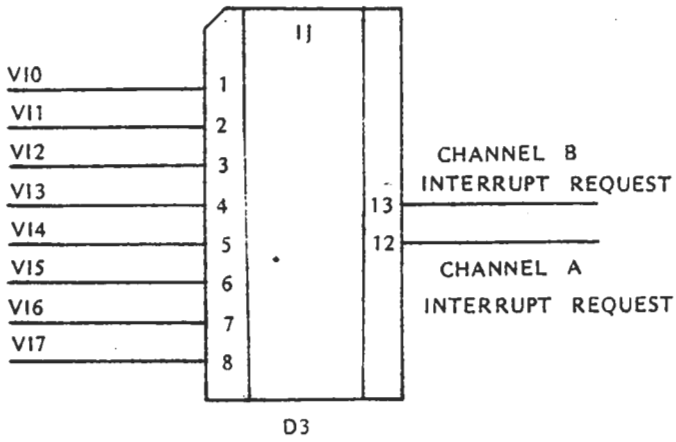
The inputs and outputs are arranged as appropriate for the SIO board to serve as the terminal end of an RS232 line. Should it be desired for the SIO board to serve as the computer end of a standard RS232 line, use jumpers connected as shown in the diagram. The 3 pairs of lines are reversed so that TRANSMIT DATA is now driving what is received data for the terminal and RECEIVE DATA is receiving what is transmit data from the terminal, and similarly, REQUEST TO SEND and CLEAR TO SEND are reversed and DATA SET READY and DATA TERMINAL READY are reversed.

Ground and +5 volts are available on the socket for providing permanent mark or space levels to any of the control lines if CLEAR TO SEND is not driven by an external source. It should be wired to pin 6 to provide a constant enable for the transmitter section of the USART.

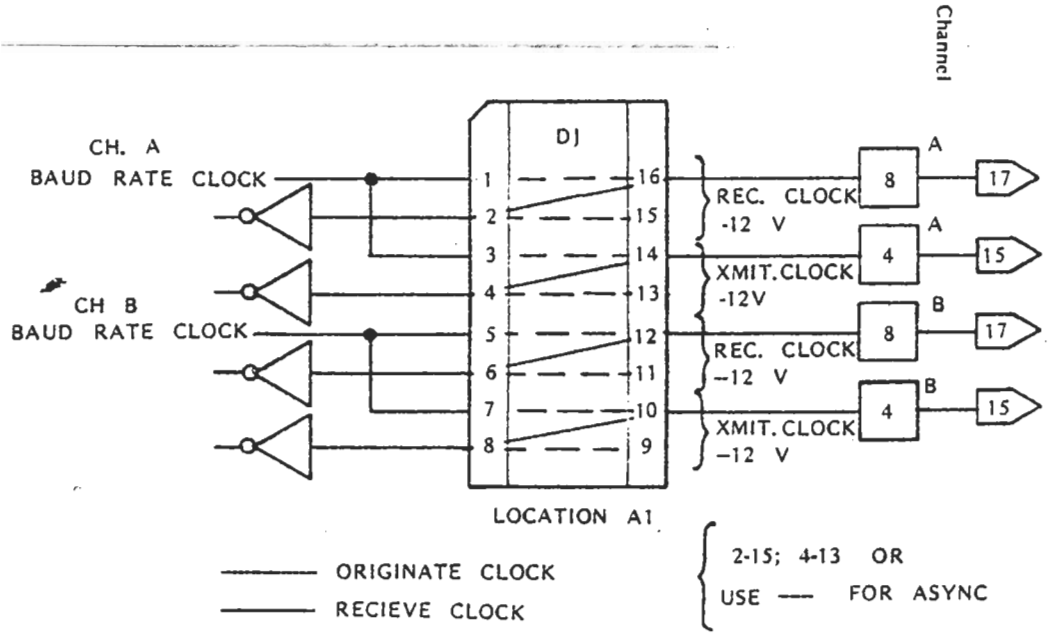
Jumper Socket BJ

Socket BJ serves both to determine whether CARRIER DETECT is being originated or received by the SIO board. It is also used to jumper the control lines between channel A and channel B for applications where the control lines are desired to be passed through and data intercepted and

SIO INTERRUPT SELECT SOCKET



SIO 232 CLOCKS JUMPER OPTIONS



Program 8251 for x16 for asynchronous operation,
x1 for synchronous.

handled. The four primary control lines for both channel A and channel B appear in this jumper socket, and can be jumper-wired straight across as desired.

It should be remembered that only one source should be driving an RS232 line at a time. If the control lines are jumpered straight across so that the modem and data terminal are driving the lines, then appropriate jumpers in jumper socket locations A3 or B8 should be removed so that the SIO board will not be attempting to drive these lines at the same time. If it is desired to detect the DATA TERMINAL READY line, then a jumper needs to be placed as shown between pins 5 and 6 for channel A, or between pins 11 and 12 for channel B.

If it is desired to originate the CARRIER DETECT line, a jumper should be placed instead between pins 5 and 7 for channel A, for 10 and 12 for channel B.

Ground and +5 volts are available in this jumper socket for providing a permanent mark or space level to any of these control lines.

The interrupt line from channel A and channel B both appear on the interrupt select socket in position D3. All 8 of the IMSAI 8080 system priority interrupt lines on the back plane, also appear on the interrupt select socket. A jumper may be placed between the appropriate channel's interrupt line and any one of the priority interrupt system lines to provide an interrupt of the desired priority.

Jumper Location DJ, Located in A1

The jumper select socket in A1 provides facilities for originating and receiving clock signals for receive or transmit for use in the synchronous mode of communication. One-half of the socket controls lines for Channel A and the other half is dedicated to Channel B. Pins 1, 2, 3, 4, and 13, 14, 15 and 16 serve the channel A jumper functions. The remainder of the pins have the identical function for Channel B.

When it is desired to originate the clock signal the pins for that channel should be jumpered straight across, as shown in the diagram, so that the clock signal from the SIO board is driven through converters to RS232 levels onto the DD and DB lines.

The inputs to the data clock receive circuits are tied to -12 volts to provide an inactive output to the OR-gate supplying the receive clock to the USART chip.

When it is desired instead to receive the clock from the RS232 cable, then these jumpers are removed and the RS232 lines DD and DB are jumpered to the input of the clock-receive circuits as shown in the diagram.

When this is done, the data rate select socket for the appropriate channel must be jumpered so that the clock line from this jumper select socket is held at ground or low in order to avoid interference between the onboard clock circuit and the incoming clock from the RS232 line.

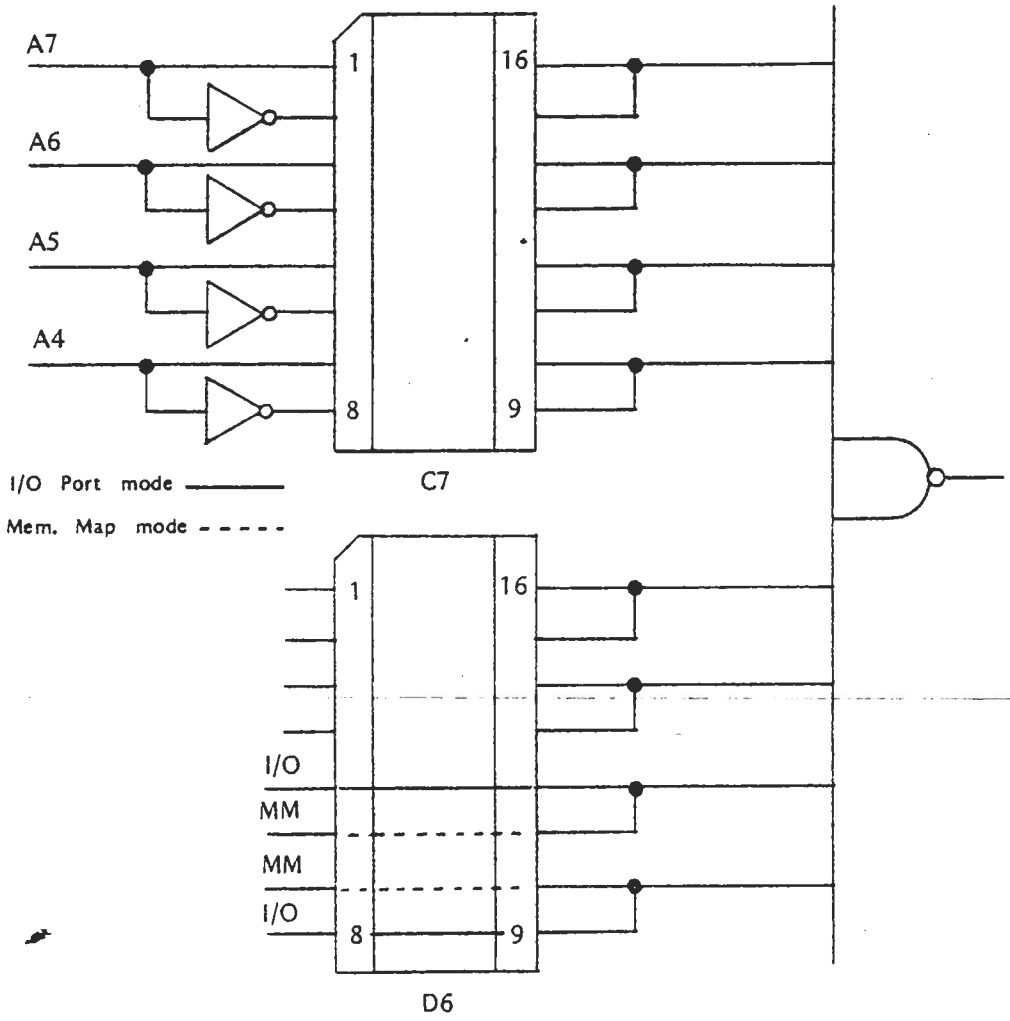
Data Rate Select Socket

The jumper socket in position B11 provides for selecting different baud rates for both Channel A and Channel B from the set of standard rates provided by the SIO board. The pin numbers and baud rates are indicated in the diagram.

The clock lines for Channel A and Channel B are completely independent and may be jumpered to the same rate or different rates.

When the chip is being used in the synchronous mode, the chip is running at a 1X clock rate rather than 16 X rate as in the asynchronous mode. Thus, the baud rates are 16 times as great for the same jumper location when used in the synchronous mode.

Board Address Selection Jumper Sockets



The board address is selected by jumpers or a DIP switch in locations C7 and D6. There are two cases for which this board may be jumpered: 1) to respond to input/output instructions and 2) to respond to memory access instructions. The case of input/output instructions will be treated first.

In selection location D6 pins 8 and 9 must be jumpered together and pins 5 and 12 must be jumpered together. The user must jumper socket C7 so when the desired I/O Port Address appears on the Address lines, the inputs to the NAND gate from bits A4 through A7 are high. If, for instance, address bit 6 is desired to be a 0 when the board responds, then pins 4 and 13 would be jumpered together. If address bit A6 was desired to be a 1, then

either pins 3 and 14 may be jumpered together or 3 and 13 may be jumpered together, since 13 and 14 are tied to the common address selection input.

It is suggested, however, that when jumpers are being used, pins 3 and 13 be connected together to provide an easy visual indication of whether the address bit is a 1 or a 0 . since that will correspond to whether the jumpers are slanted or straight across the jumper socket. Pins 13 and 14 were tied together so that an 8 position DIP switch can be inserted in this location and used to select the address. Address bits 4, 5, and 7 are jumpered in a similar manner on position C7.

See the diagram on the previous page for pin numbers for each address bit.

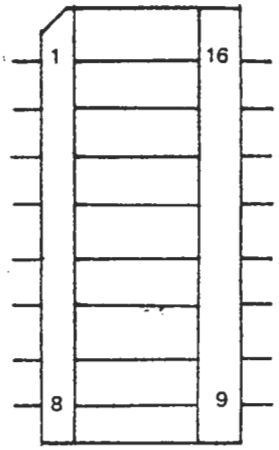
If it is desired to use the board in a memory-mapped I/O capacity, then in position D6 the jumpers between pins 8 and 9 and 5 and 12 must be removed and two jumpers inserted between pins 7 and 10 and between 6 and 11. The remaining jumpers for bits 4 through 7 function exactly the same and affect the lower eight bits of the memory address. The upper eight bits of the address will always be all ones, that is hex FE or octal 376.

When used as a memory-mapped I/O board, all instructions that normally affect the memory will operate on the I/O ports. For example, an increment memory instruction would read the data from the addressed input port, increment that data by one and output it on the same address output port.

Example Jumpers -

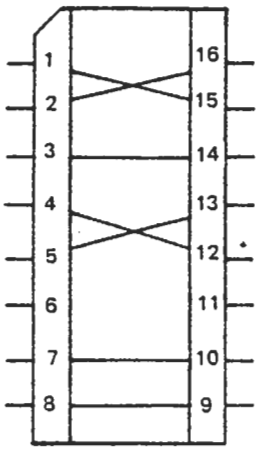
To use the SIO Board in its simplest form, non-interrupted input/output instruction controlled, create jumpers as shown.

A1

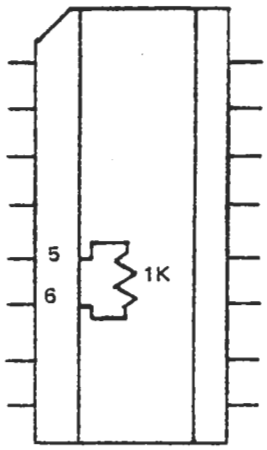


RS232 or Current Loop

A3 (B8)

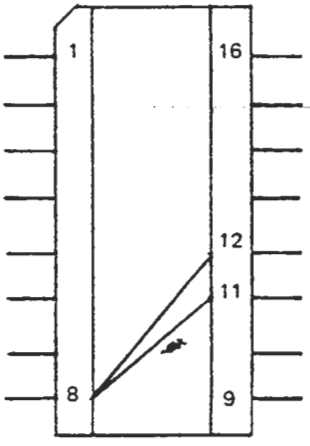


RS232

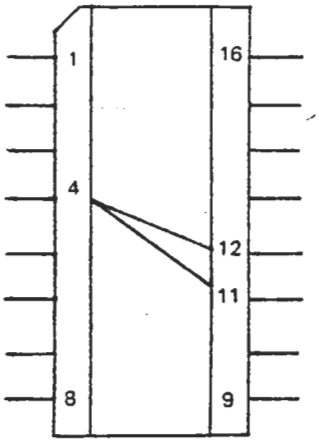


Current Loop

B11

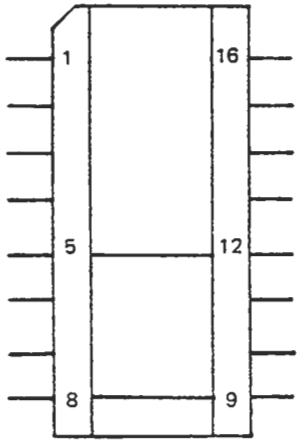


110 BAUD

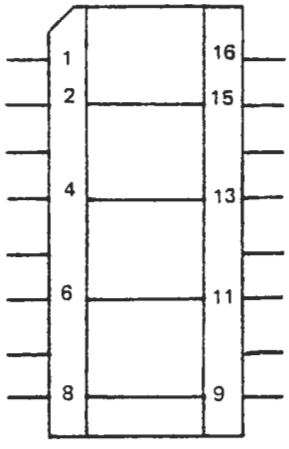


1200 BAUD

D6



C7



Select appropriate address-
Shown is 0- as required by SCS

Sample sequence to set up SIO for teletype and echo from keyboard to printer:

Format used is 2 stop bits, no parity, and 7 data bits. Reset IMSAI 8080 before running. Address and constants are in hexadecimal.

```
LIST
0010      MVI A,0CAH          MODE BYTE
0020      OUT 03
0030      MVI A,27H           COMMAND BYTE
0040      OUT 03
0050 LOOP IN 03               READ CHAN A STATUS
0060      ANI 02              MASK OUT ALL BUT RECEIVER READY
0070      JZ LOOP             IF NOT READY LOOP
0080      IN 02               READ CHAR
0090      OUT 02              WRITE CHAR
0100      JMP LOOP
```

```
ASSM 3700

3700 3E CA      0010      MVI A,0CAH          MODE BYTE
3702 D3 03      0020      OUT 03
3704 3E 27      0030      MVI A,27H           COMMAND BYTE
3706 D3 03      0040      OUT 03
3708 DB 03      0050 LOOP IN 03               READ CHAN A STATUS
370A E6 02      0060      ANI 02              MASK OUT ALL BUT RECEIVE
370C CA 08 37   0070      JZ LOOP             IF NOT READY LOOP
370F DB 02      0080      IN 02               READ CHAR
3711 D3 02      0090      OUT 02              WRITE CHAR
3713 C3 08 37   0100      JMP LOOP
```

Notes on the SIO Board.

This is an Excellent but complicated board, and IMSAI's instructions don't help any. The board is currently set up for two Identical channels as follows

Baud Rate : 300 Baud — Parity : ODD, Disabled
Stop Bits : 1 — Word Length : 8 Bits
Addresses : 0-15, I-O mapped — Signal Type : RS-232

Use 4E as a mode Byte and 37 as a Command byte.
For odd parity enabled, use 5E for mode
For Even parity enabled use 7E for mode
For two stop bits, change the 4E, 5E or 7E to CE, DE or FE, respectively
For 7 Bit word, Change Low order Four bits of mode byte From E to A.

Command Byte will be 37 for virtually any application you are likely to encounter (27 will also work)

for more information, See the Intel 8080 System users manual 8251 section, pgs 5-140 thru 5-141

The board occupies 16 ports as follows:

0 – Not used *
1 – Not used *
2 – Data I/O for channel 1
3 – Control/Status I/O for channel 1 (write Mode or Control; Read status)
4 – Data I/O for channel 2
5 – Control/status I/O for channel 2
6 – Simultaneous data output only for channels 1+2
7 – Simultaneous control output only for channels 1+2
8 – Control Channel select (see lower half of pg 9-19)
9
A
B
C
D
E
F
} not used *

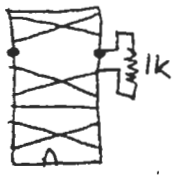
only addresses 2,3,4,5 (and possibly 8) will be used in most applications
see IMSAI manual pg 9-19

* Not used means that the board address space occupies this address or I/O port, but it is of no actual use to a user. However other devices cannot also occupy this address or I/O port

1. Board addressing is set up at socket (C7) and (D6)
2. Baud Rate is set up (B11).
3. Interrupts (if desired) may be set up at socket (D3).
4. To select use the board as either the computer end end of the line or the terminal end, use the sockets at (A3) and (B8).
5. Synchronous clock signals (if desired) are set up at (A1)
6. Provision for tying the two channels together is provided at (A5) (the Book calls this BJ).

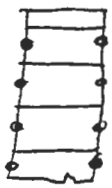
As supplied:

1. D6 selects Memory or I-O mapped. Set for I-O
2. C7 selects I-O addresses. Set for Ø-F.
3. B11 sectects Baud Rate. Set for 300 Baud (Both channels).
4. A3, B8 select computer or Terminal End. Set for computer End. Also set for RS-232 (not current loop).
5. Interrupts not used; D3 not jumpered.
6. For Asynch (as set up), jumper A1 straight across
7. A5 not used, not jumpered.



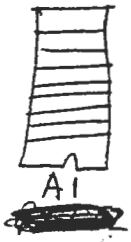
A3, B8
computer end
RS232

D6
I/o mapped



C7
0-F

B11
300 Baud



Asynch

IMSAI's instructions for setting up A1/B8 are incorrect, as is schematic (connections between A3/B8 and edge connectors are reversed - A3 9 goes to A11 and A3 10 goes to A14). On pg 922, at top of pg, wires between pins 7-8-9-10 have dotted + dash lines reversed, should be just like 1-2-15-16 and 4-5-12-13.

Using the Board

The board Requires software initialization. Following a system Reset, you must send out a mode byte and a command byte to each port to be used, and it must be 1st thing Sent to the board Following a system Reset. (a dummy mode byte + command byte can be substituted for the Reset -- Dummy command byte should be 40 hex). The software on pg 9-34 is a good example, but is for 7 data bits + two stop bits. See pgs 5-140 + 5-142 of Intel 8080 book (sept 75 ed) for correct format for your system.

For each channel, bit 0 is transmitter Ready and bit 1 Received Data Avail (when reading that channels Status port).

Bill,

Re: using the board with North Star

There is a jump to INIT at 2013H in the NORTH STAR DOS.; The instruction jumped to is probably a Return (C9)* -- Replace that INSTRUCTION with the following code:

```
INIT:   MVI   A, 4EH      ; Dummy mode
        OUT   03H
        MVI   A, 40H      ; Command = Internal RESET
        OUT   03H
        MVI   A, 4EH      ; Real Mode Byte
        OUT   03A
        MVI   A, 37H      ; Real Command
        OUT   03H
        RET
```

Note: this initializes only 1 channel unless the address is OUT 07H

03 = Channel A
05 = " B

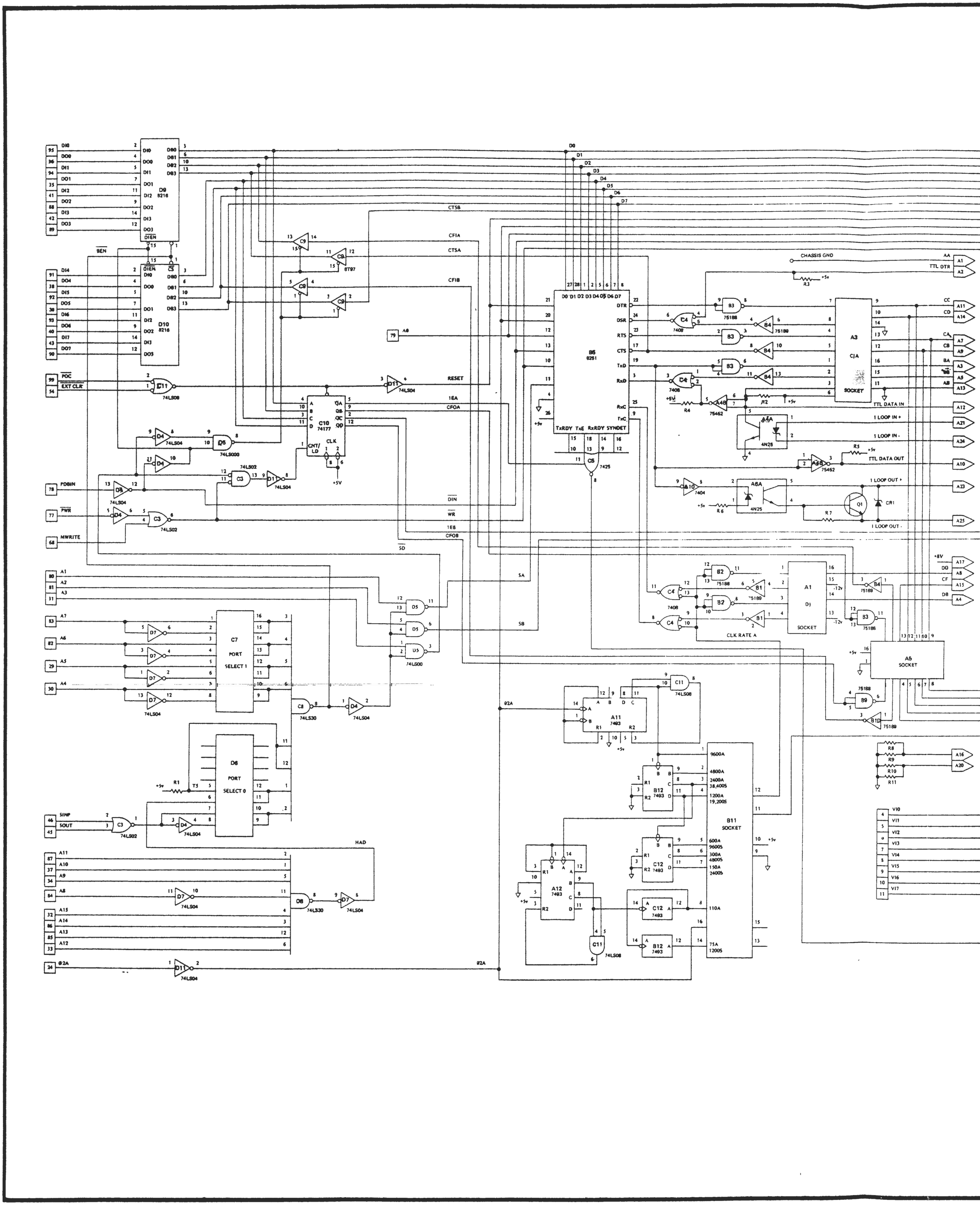
Of course you will have to either move (eg re-assemble) all of the code in the North Star DOS's I/O Block (2900H to 29FFH) or put the above at the end of the code on that page & change the Jump at 2013. The above initialization sequence may be changed depending on board location & Also whether or not you use same data format it was written for -- but only circled bytes will change -- others will work in all cases.

* IF it's NOT A return add the above code to the INIT section

IF you have any questions or need help, feel free to call -- thanks,

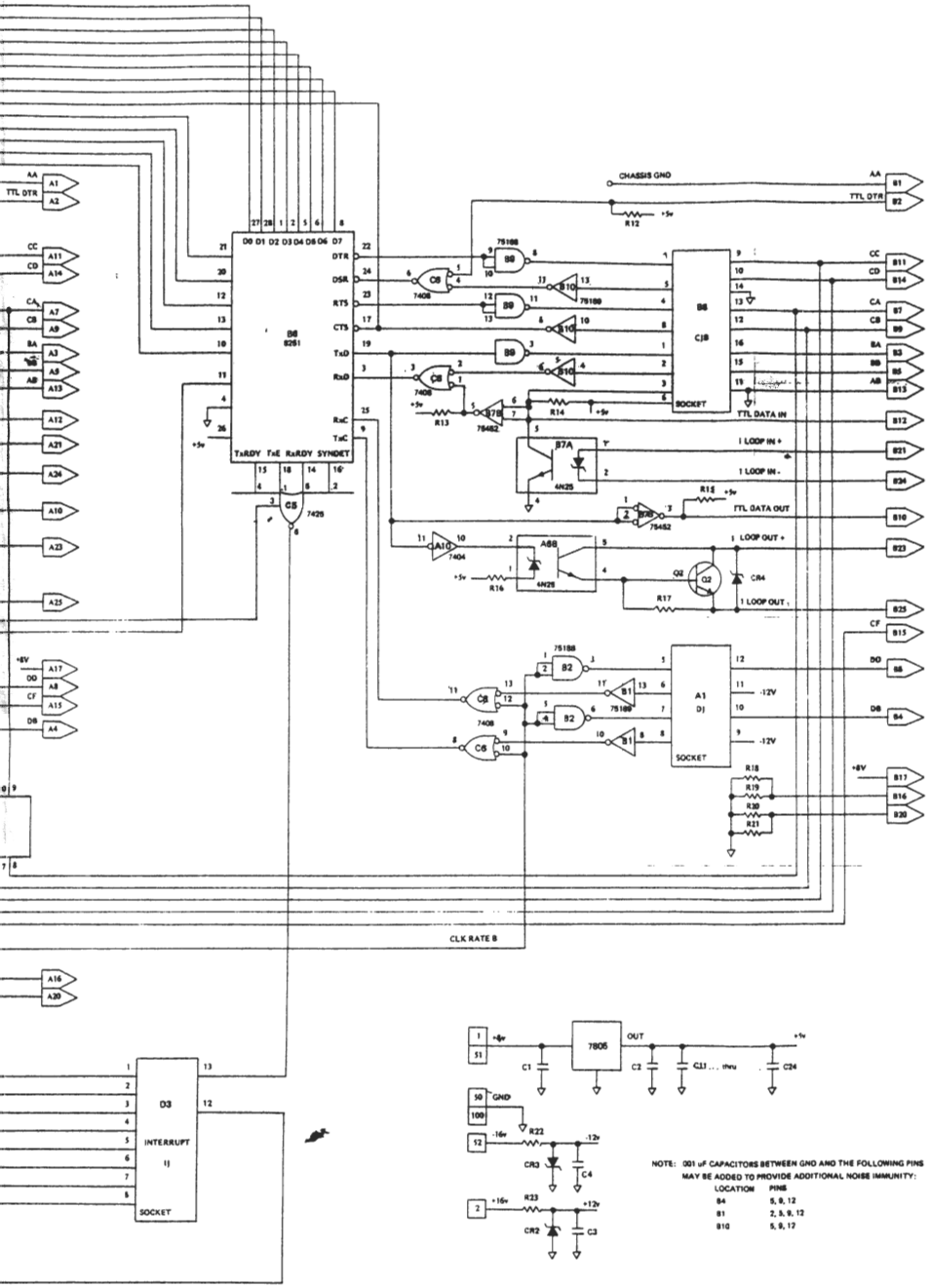
Barry Watzman

BARRY WATZMAN
2330 MILLENNIUM LN
RESTON VA, 22091
703- 860-9411 (home)
821-6188 (Bus)



D9
8216
D10
8216
B5
8251
C10
74177
CLK
RESET
CTSB
CF1A
CTSA
CF1B
1EA
CFOA
DIN
WR
1E8
CFOB
SD
SA
SB
BEN
POC
EXT CLR
PDBIN
PWR
MWRITE
SINP
SOUT
HAD
φ2A
C7
PORT
SELECT 1
D6
PORT
SELECT 0
A11
7493
A12
7493
B12
7493
C12
7493
B11
SOCKET
A3
CJA
SOCKET
A1
DJ
SOCKET
A5
SOCKET
CHASSIS GND
TTL DTR
TTL DATA IN
1 LOOP IN +
1 LOOP IN -
TTL DATA OUT
1 LOOP OUT +
1 LOOP OUT -
CLK RATE A
9600A
4800A
2400A
38,400S
1200A
19,200S
600A
9600S
300A
4800S
150A
2400S
110A
75A
1200S
4N25
75188
75189
75452
7408
7425
7404
74LS04
74LS08
74LS02
74LS00
74LS30
8T97

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
0	ORIGINAL REV. 3	5/76	
1	UPDATE & MOD.	12/76	



NOTE: .001 uF CAPACITORS BETWEEN GND AND THE FOLLOWING PINS MAY BE ADDED TO PROVIDE ADDITIONAL NOISE IMMUNITY:

LOCATION	PINS
B4	5, 9, 12
B1	2, 5, 9, 12
B10	5, 9, 12

A1, A3, A5	OPTIONAL JUMPER SOCKET	R1, R2, R3, R13, R14	1K ¼W
A4B	75452		
A4A, A6A, A6B	4N25	R4, R5, R6, R12, R15, R16	220 ¼W
A10	7404		
A11, A12	7493		
B1, B4, B10	75189	R7, R17	4.7 ¼W
B2, B3, B9	74188	R8, R9, R10, R11, R18, R19, R20, R21	470 ¼W
B5, B6	8251		
B7A	4N25		
B7B	75452		
B8, B11	OPTIONAL JUMPER SOCKET	R22, R23	56 ½W
B12	7493		
C3	74LS02		
C4, C6	7408		
C5	7425		
C7	PORT SELECT 1		
C8	74LS30		
C9	8T97		
C10	74177		
C11	74LS08		
C12	7493		
D3, D6	OPTIONAL JUMPER SOCKET		
D4, D7, D11	74LS04		
D5	74LS00		
D8	74LS30		
D9, D10	8216		
C1 thru C4	33 uF		
C11 thru C24	.1 uF		
CR1, CR4	1N914		
CR2, CR3	1N4742		
Q1, Q2	2N3904		

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC. ANGLES ± . ±	IMSAI MFG. CORP. SAN LEANDRO, CA.	
APPROVALS / DRAWN / CHECKED	DATE	SCHEMATIC DIAGRAM SIO 2–2 REV. 3 12/76
		SCALE: — SIZE: — DRAWING NO: 91–4010018
		DO NOT SCALE DRAWING — SHEET