RAM 4A BOARD

FUNCTIONAL DESCRIPTION

The IMSAI RAM 4A board provides up to 4K bytes of static random access memory. The board is implemented with 2102-style memory chips that each have the capacity to store 1024 words of one bit for each word. Thus eight chips are used to store one block of 1024 eight-bit words. Up to four sets of eight-chip units can be used on the board, giving a maximum capacity of 4096 eight-bit words.

Each eight-chip unit has the circuitry to allow or prevent the ability to write information into their memory storage space. This "write-protect" feature can be controlled either by software commands or from the computer front panel. Software commands can both affect the write protect and test the status of the write protect. If the program attempts to write into a write-protect block of memory, an interrupt will be generated. (This feature may be disabled if desired.) Four red LED's are provided to indicate the protect status of each of the 1K blocks of memory. Four green LED's are also provided which illuminate when their respective block of memory is addressed.

The RAM 4A board will support a front panel write protect switch. If the machine is stopped, the 1024 word block at which the machine address is pointing will have its memory write protect status affected through the use of a PROTECT/UNPROTECT switch on the front panel. Attempts to write into this section of the memory will, of course, not succeed.

The RAM 4A board is designed to allow the user to provide battery backup power. Trickle-charging facilities to allow the battery to be charged while the computer is running may also be installed on the board by the user.

The 8080A microprocessor can address up to 65,536 words of memory, thus allowing up to 16 4096 word RAM 4A-4 boards to be installed in one IMSAI 8080 system. (Additional memory can be accessed by using IMSAI's Shared Memory Facility.)

RAM 4A BOARD

THEORY OF OPERATION

The memory circuits used on the IMSAI RAM 4A memory board are 2102-style integrated circuits housed in sixteen pin DIP packages. Their organization is 1024 words, each of which is one bit wide. Ten address inputs are used to select the desired word and there is a chip enable to select the chip. There is a read/write input. One input is provided for data in, and one output is provided for data out. To implement the storage of data words that are eight bits wide, eight of the above described chips are used to store 1024 words. Three more of these eight chip groups can be used to give the IMSAI RAM 4A memory board a maximum storage capacity of 4096 eight bit words.

Bits A9, A8, A7, A6, A5, A4, A3, A2, A1, and A0 of the address bus come onto the memory board and go directly to the appropriate address pins on each memory chips. Bits A11 and A10 are decoded by a section of the 74LS156 at location D8 to select the desired 1024 word block by assertion of the chip enable signal for only those eight memory chips comprising the desired 1024 word block.

Bits A15, A14, A13, and A12 of the address bus are used to give each memory board on the bus a unique address. These bits first go through (if the memory board is involved in the utilization of its memory function through a memory-read operation, or memory write operation) the 74LS157 data selector at location D5. The direct output, and the complement of the direct output (obtained through the 74LS04 inverters at location C6) of the four output pins of the 74LS157 at location D5 go to DIP jumper provision at location C5. Provision is made so that either the equivalant polarity, or its complement, of the above mentioned four address bits can be implemented through the correct use of jumpers at location C5. When the polarity of the above-mentioned four address bits are in such an arrangement that they satisfy the address requirements of a particular memory board the four input pins of a section of the 74LS20 at location C4 will be high. This effects the selection of an individual memory board. Thus, only one board should respond in this manner for each of the sixteen different polarity arrangements of these four address bits.

Each 1024 word block of memory has its own circuitry to implement the write-protect feature. This feature is manipulated in two ways. One is from the "PROTECT/UNPROTECT" switch on the front panel. The other is from program commands contained in software.

There are four flip/flops whose two states enable or prevent the changing of the contents of their respective 1024 word blocks when a memory write is received. Each of these four flip/flops is a section of a 74LS74 at location C10 and at location C9. Memory block 0 is controlled by half of C9, memory block 2 is controlled

by the other half of C10, and the other half of C9 controls memory block 3. The individual status of these four flip/flops is indicated by the desigated red light-emitting diodes located in the upper left hand corner of the board. If the red LED for a block is illuminated then that block is protected and writing into that block cannot occur. NOTE: A system reset will unprotect all blocks of memory.

If a 1024 word block of memory is selected by its chip enable being decoded by the 74LS156 at location D8, and its respective write protect flip/flop at locations C10 or C9 are not in the protect state, then the section or the 74LS02 at location C8 associated with this block will have a high output. This high output, seen at the input of the 7425 at location C7, will cause the output of C7 to go low and this will assert one of the chip enable pins (pin 15) of the 74LS156 at location D10. The second chip enable of D10 is asserted on the PWR bus line; the second is an assertion on the MWRITE bus line. D10 will decode address bus bits A11 and A10 (as at D8) and issue a write pulse only to the selected 1024 word block.

The four write protect flip/flops at locations C10 and C9, as described earlier, are set and reset under the control of two sets of decoders whose outputs are wired ORed. One set, a section of the 74LS156 at location D10 that is used to set the flip/flops, and a section of the 74LS156 at location D8 that is used to clear (or reset) the flip/flops, is utilized when the protect/unprotect switch controls the assertion of the protect and the unprotect bus lines whose assertion is utilized via the chip enable input (pin 1) of D10 and D8. The other chip enable (pin 2) of both D10 and D8 is connected to the BDENA signal generated by the output (pin 8) of the 74LS20 at location C4. The two input lines to D10 and D8 that will be decoded to one of four output assertions are the address bus lines A11 and A10.

The other set of decoders are both sections of the 74LS156 at location D9. These are utilized when the four write protect flip/flops are going to have their status changed by programmed commands in the software. The command used is an output command, one of 256 available. The board is created to use output command FE, and only this one command is used for all (a maximum of 16) RAM 4A memory boards on a bus. The necessary board selection, and block selection, is done by putting board address (the same one as is used for board selections from the address bus-this feature is provided by the 74LS157 data selector at location D5), the two bits used to select one-of-four blocks of memory, and the two bits that are decoded to perform one-of-three actions, out on the system data bus at the time an FE output command bus is used. Two of the actions decoded by the 74LS139 at location D4 are the setting or the clearing (resetting) of the write protect flip/flop of the memory block as decoded from DO 3 and DO 2 by the 74LS156 one-of-four decoder at location D9.

The third action decoded from DO 1 and DO 0 by the 74LS139 one-of-

four decoder at location D4 is the setting of the board select flip/flop, a section of the 74LS74 at location D2, which is used to select that board which puts data on the DATA IN (DI) bus when a data input FE command is issued so that the protect status can be read by the microprocessor. DI 0, DI 1, DI 2, and DI 3 carry the status of the write protect flip/flops for memory blocks 0, 1, 2 and 3. This status information is gated onto the DI bus through the 8T97 at location D3. The remaining four bits of the DATA IN bus, DI 4, DI 5, DI 6, and DI 7, carry the board address as set by the jumpers at location C5.

There is a flip/flop, a section of a 74LS74 at location D2, that becomes set if a write operation is attempted into a block of memory that is write protected. This flip/flop drives a transistor whose open collector output can be jumper connected to the INTERRUPT REQUEST (PINT) bus line pin 73, or to one of the vectored interrupt lines on bus pins 4 through 11. This interrupt notifies the user that a write has been attempted in a protected block of memory. The user may handle this interrupt with an interrupt routine.

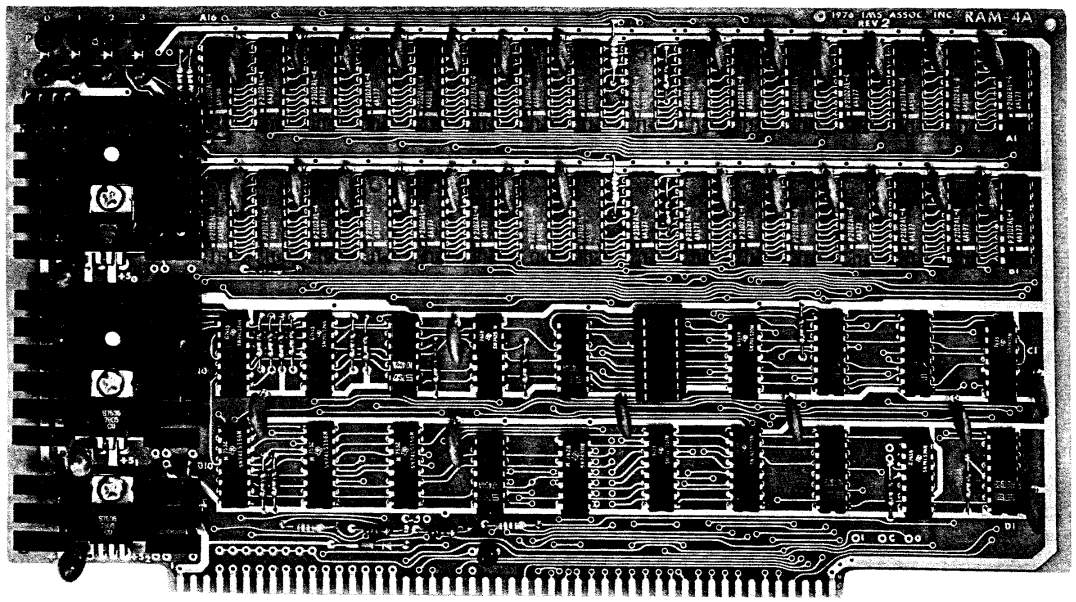
RAM 4A
Parts List

BOARD: RAM 4A

ITEM	IMSAI PART #	QUANTITY	DESCRIPTION/IDENTIFYING MARKS
Solder	15-0000001	10'	Solder
Heat Sink	16-0100003	1	3-Prong Heat Sink
Heat Sink	16-0100004	2	6-Prong Thermalloy Heat Sink
Screw	20-3302001	3	6-32x5/16" Phillips Pan Head Machine
Nut	21-3120001	3	6-32 Hex Nut
Lockwasher	21-3350001	3	#6 Internal Star Lockwashers
Header	23-0400001	1	16 Pin IC Header
Socket	23-0800001	1	16 Pin Solder Tail Socket
Resistor	30-3100362	1	100 Ohm, ¼ Watt/brown, black, brown
Resistor	30-3220362	10	220 Ohm, ¼ Watt/red, red, brown
Resistor	31-4100362	18	1K Ohm, ¼ Watt/brown, black, red
Capacitor	32-2010010	15 34	(For 1K) .1uF Disk Ceramic (For 4K)
Capacitor	32-2233070	1	33-25 Tantalum (or 22-25)
Diode	35-1000005	1	1N751-A Diode
Diode	35-1000007	6	1N4002 Rectifier Diode
LED	35-3000001	1 4	(For 1K) Red LED (For 4K)
LED	35-3000002	1 4	(For 1K) Green LED (For 4K)
8T97	36-0089701	3	Hex Tri-State Buffer/N8T97B
8T98	36-0089801	1	Hex Tri-State Buffer/N8T98B

RAM 4A
Parts List

ITEM	IMSAI PART #	QUANTITY	DESCRIPTION/IDENTIFYING MARKS
2102	36-0210201	8	(For 1K) 1Kx1 Organization Static Memory Chip/P2101AL4
		32	(For 4K)
7402	36-0740201	1	Quad 2 Input NOR/DM7402N
7404	36-0740401	2	Hex Inverter/7404-N
74LS20	36-0472002	1	Dual 4 Input NAND (Low Power Schottky)/ SN74LS20N
7425	36-0742501	1	Dual 4 Input NOR with Strobe/SN7425N
7430	36-0743001	1	8 Input NAND/SN7430N
7432	36-0743201	1	Quad 2 Input OR/SN7432N
74LS74	36-0747402	3	Dual D Flip-Flop Preset and Clear (LPS)/SN74LS74
7805	36-0780501	3	5V Positive Volt Regulator/MC7805CP
74LS139	36-7413902	1	Dual 2 to 4 Line Decoder (LPS)/ SN74LS139N
74LS156	36-7415602	3	Open Collector (LPS)/ SN74156N
74LS157	36-7415702	1	Quad 2 to 1 Line Data Selector (LPS)/ SN74157N
PC Board	92-0000017	1	RAM 4A, Rev. 3



RAM 4A–4 REV. 2

RAM 4A
Assembly Instructions

RAM 4A-4 Assembly Instructions

1) Unpack your board and check all parts against the parts lists enclosed in the package.

2) If gold contacts on the edge connector appear to be corroded, use pencil eraser to remove any oxidation. NOTE: Do not use Scotch-bright or any abrasive material as it will remove the gold plating.

RESISTOR INSTALLATION

3) Insert and solder each of the eighteen 1K ohm 1/4 watt resistors (brown/black/red) R1 through R18. See Assembly Diagram for location.

4) Insert and solder each of the ten 220 ohm 1/4 watt resistors (red/red/brown) R19 through R28. See Assembly Diagram for location.

5) Insert and solder the one 100 ohm 1/4 watt resistor (brown/black/brown) R29. See Assembly Diagram for location.

6) Insert and solder each of six 1N4002 diodes, CR1 through CR6, as shown in the Assembly Diagram. NOTE: Observe polarity marks as indicated on board.

7) Insert and solder one 1N751A zener diode, Z1 observing polarity marks as shown on the board.

IC INSTALLATION

NOTE: All IC pin 1's point in the direction of the edge connector as indicated with the square solder pad in each hole pattern.

8) Insert and solder each of the three 74LS74 at locations C10, C9, a and D2.

9) Insert and solder each of the three 74LS156 at locations D8, D9, and D10.

10) Insert and solder each of the three 8T97 at locations C2, C3, and D3.

11) Insert and solder one 8T98 at location D1.

12) Insert and solder one 7402 at location C8.

13) Insert and solder one 74LS20 in location C4.

14) Insert and solder one 7425 at location C7.

15) Insert and solder two 7404 at location C6 and D7.

16) Insert and solder one 7430 at location D6.

17) Insert and solder one 74LS157 at location D5.

18) Insert and solder one 74LS139 at location D4.

19) Insert and solder one 7432 at location C1.

20) Insert and solder each of the eight 2101 memory chips at locations A9 through A16 for 1K RAM Board and each of the thirty-two 2102 memory chips at locations B1 through B16 for 4K RAM Board.

DISCRETE COMPONENT INSTALLATION

21) Insert and solder the 16 pin IC socket located at C5 and plug in the 16 pin jumper header. (This jumper header is used for board addressing).

22) Insert and solder one 2N3904 transistor at location Q1 as shown on the Assembly Diagram. NOTE: Observe orientation as shown on the Assembly Diagram.

23) Insert and solder each of the fifteen .1uF capacitors at locations C7 through C13 and C27 through C34 for 1K RAM Board and each of thr thirty-four .1uF capacitors at location C1 through C34 for 4K RAM Board as shown on the Assembly Diagram.

24) Insert and solder each of the three 33uF 25 volt tantalum capacitors at locations C35 through C37 as shown on the Assembly Diagram. NOTE: Observe polarity as shown on board.

25) Insert and solder one red LED at location P0 for 1K RAM Board and each of the four red LED's at locations P0 through P3 for 4K RAM Board as shown on the Assembly Diagram.

26) Insert and solder one green LED at location E0 for 1K RAM Board and each of the four green LED's at location E0 through E3 for 4K RAM Board as shown on the Assembly Diagram. NOTE: The LED's should be positioned so that the flat side of the cathode is to the right.

REGULATOR AND HEAT SINK INSTALLATION

27) Take each of the three 7805 regulators and bend the leads at 90 degree angles approximately ¼" from the bottom edge of the regulator to facilitate insertion on top of the heat sink.

28) The smallest heat sink is used near the bottom of the board, closest to the edge connector. Insert the #6 screw and lockwasher through the regulator and heat sink and tighten with the nut on the back side of the board. Repeat this procedure with the two remaining heat sinks and solder each of the regulator leads in place. NOTE: Be sure to hold the screw in order to prevent shorting to adjacent traces.

29) Add jumper wires for desired address onto the jumper header. (See User Guide Section). This indicates the address of the board.

JUMPER OPTIONS

30) A) Using clipped resistor leads (or bus wire) to select 0 wait states, jumper hole (C) to hole (0).

B) For one wait state, jumper hole (C) to hole (1). These holes are located on the board directly below locations D2 and D3.

31) The select interrupt jumper may be installed after reading the User Guide Section and after determining which vectored interrupt is desired.

USER GUIDE

Board Selection

In memory read or memory write operation (as well as responding to the output or input commands of FE) the IMSAI RAM 4A memory board is designed to be selected as one out of a maximum possible of sixteen RAM 4A memory boards present on the bus. To achieve this one-of-sixteen selection, the top four address lines--A15, A14, A13 and A12 in the case of a memory read or memory write operation (or the top four data out lines (D0 7, D0 6, D0 5 and D0 4) in the case of an output or input FE instruction)--are decoded on the board via the positioning of the jumpers installed at location C5 to give each memory board its unique address. These jumpers are implemented so as to route the logic 1 polarity of the above described four lines, or the complements of their polarities, in such a manner that when a board's unique address is present on the above described lines the four inputs to the 74LS20 four input NAND gate at C4 will all be high.

This will make the output (pin 8) go low and will assert the board enable (BDENA) line on the board. If the logic 1 polarity is desired then the jumper for that bit should route the output of the 74LS157 at location D5 direct to the input of the 74LS20 at location C6, associated with that bit shall be routed to the input of the 74LS20 at location C4.

TABLE 1

ADDRESS BIT	DIP POSITION C5		JUMPERING
	Pin 9	Pin 8	Place jumper between pins 9 and 8 if the board is to be selected when this bit is high.
A15			
	Pin 10	Pin 7	Place jumper between pins 10 and 7 if the board is to be selected when the above bit is low.
	Pin 11	Pin 6	Place jumper between pins 11 and 6 if the board is to be selected when this bit is high.
A14			
	Pin 12	Pin 5	Place jumper between pins 12 and 5 if the board is to be selected when the bit is low.
	Pin 13	Pin 4	Place jumper between pins 13 and 4 if the board is to be selected when this bit is high.
A13			
	Pin 14	Pin 3	Place jumper between pins 14 and

			3 if the board is to be selected when the above bit is low.
A12	Pin 15	Pin 2	Place jumper between pins 15 and 2 if the board is to be selected when this bit is high.
	Pin 16	Pin 1	Place jumper between pins 16 and 1 if the board is to be selected when this bit is low.

Hardware Write Protect

If memory PROTECT/UNPROTECT from a switch (located on the front panel or elsewhere) is to be used, jumper D8 pin 1 to I/O pin 20. In cases where a switch will not be used and I/O pin 20 is driven high (such as in the IMSAI CP-A Revision 4 or earlier front panel assembly), D8 pin 1 should be jumpered to ground. Jumper pads are provided to accomodate either case. Refer to Figure 1 for details.

Memory is protected in 1K blocks. With the computer front panel in the stop mode, the switch will affect whichever block contains the address being displayed. To protect or unprotect any block, examine any word in that block and actuate the switch. The memory protect light on the front panel will indicate the protect status of the addressed block.

A system reset will unprotect all blocks of memory.

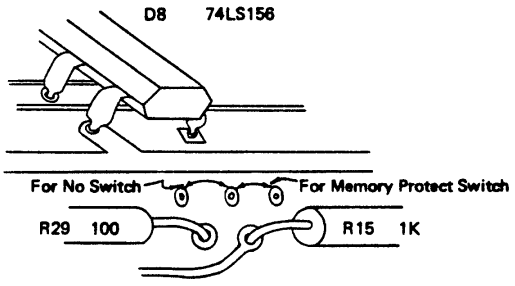


FIGURE 1

Software Write Protect

1K blocks of memory may be write protected or unprotected with an OUT command to port FE*. Selection of memory board and block is selected with the high-order 6 bits in the output data word. Bits 0 and 1 select the function (Protect, Unprotect, Select Board for Status or Clear Interrupt). Bits 2 through 7 should be the same as bits 10 through 15 of the memory address of the desired 1K block. Bits 4 through 7 select the memory board and bits 2 and 3 select the 1K block on that board. Refer to Table 2 for bit functions.

TABLE 2

Output Data Bit

7, 6, 5, 4	Board Select	Same as Memory Address Bits for desired 1K Block	15, 14, 13, 12
3, 2	1K Block Select		11, 10
1, 0	Function Select		

Bit 0	Bit 1	
0	0	Clear Interrupt
1	0	Unprotect Addressed Block
0	1	Protect Addressed Block
1	1	Select Board for Status Read

The output command to select a board for status read must be issued before each status read. This enables the selected board to respond with status to the next INP command from port FE. The board automatically deselects after responding to the INP command. Care should be taken not to select more than one board before reading the status or the boards will interfer with each other. Refer to Table 3 for the meaning of the status data bits.

* This address may be changed if desired by using the inverters in C7 (pins 1, 2, 3, 4). Cut the trace to the desired input pins to D6 and solder jumpers to the spare inverter. The inverter line A8 may similarly be removed and placed in another bit. Be sure to reconnect bit A8.

TABLE 3

STATUS READ

Data Bit		
7	Same as Address Bits (Board Address)	15
6		14
5		13
4		12
3	Block 3	1=Unprotected 0=Protected
2	Block 2	
1	Block 1	
0	Block 0	

The Interrupt Request flip/flop is set by an attempt to write into a protected location. (The data in memory will not be affected.) In addition to requesting an interrupt (if jumpered appropriately) the Interrupt Request flip/flop enables the board to respond to the next Status Read (INP FE). The bit definitions are the same as a normal status read, which indicates what board is affected and which 1K blocks on that board are protected. The Interrupt Request flip/flop is reset by the appropriate output command. See Table 3.

Because of the possible conflict during a status read if the Interrupt Request flip/flop is set between a board select and the following Status Read, it is suggested that all status reads be performed by a subroutine which disables interrupts, selects a board, reads its status, enables interrupts and returns.

To obtain the Interrupt Request feature, a jumper must be installed to connect the RAM 4A to the desired Priority Interrupt line on the back plane. Figure 2 illustrates the placement of this jumper.

Battery Backup Operation

For operating your RAM 4A board with battery backup, simply connect your battery to the board at the location indicated on the Battery Hookup Diagram.

The battery should deliver 3 to 5 volts DC and should supply 300 milliamps of current.

A user defined resistor may be installed on the board to facilitate recharging the battery while the computer is turned on. (See Assembly Diagram for location.)

As an example for picking the value resistor that should be used to supply the trickle charge to your battery:

For a back plane voltage of (+8V)
and a battery voltage of - (+3V)
(+5V)

I=E/R
=5V/220 ohms
=.0227 Amps

A resistor of 220 Ohms will supply approximately 20 ma. current as trickle charge to your battery.

It is also recommended that if you do not intend to use battery back-up, remove the three diodes in the input circuit of the three regulators and replace them with jumper wires. This will allow the board to function with a Mother board voltage of 7 volts DC rather than 7.7 volts DC.

System Features Test

The special functions of this memory board far exceeds the functions of any other memory board on the market today and, because of this, is going to take a little time for the user to understand all its capabilities. A NOTE OF CAUTION: One common mistake that is made when using this board is protecting a block of memory where you may have placed your stack.

A simple test program for testing some of the special features of your new RAM 4A board follows:

Address	Instruction	Description
00	DB	INPUT
01	FF	FROM FRONT PANEL SWITCHES
02	D3	OUTPUT
03	FE	TO MEMORY BOARD
04	DB	INPUT
05	FE	FROM MEMORY BOARD
06	D3	OUTPUT
07	FF	TO FRONT PANEL LIGHTS
08	C3	JUMP
09	00	TO
0A	00	0

If it is desired to prevent the Interrupt Request flip/flop from being set (e.g., to avoid conflict with status reads if interrupts are not being used), cut the flip/flop line between the two pads to the left of D2 on the solder side (see Figure 3).

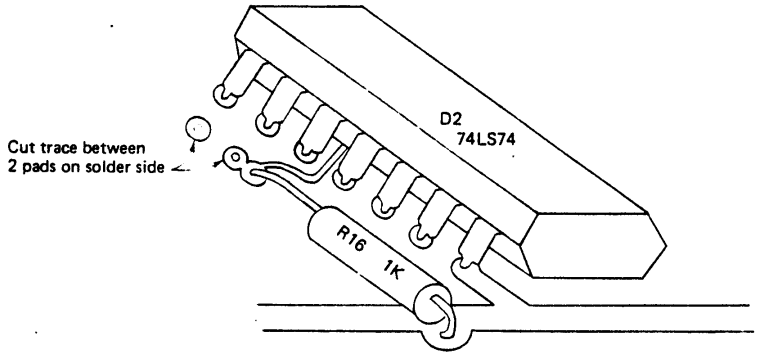


FIGURE 3

Wait Cycle Selection

No wait cycle is required for the memory chips supplied with the RAM 4A board. One wait cycle may be required if slower memory chips are substituted. Selection of the wait cycle option (zero or one wait cycle) is illustrated in Figure 4.

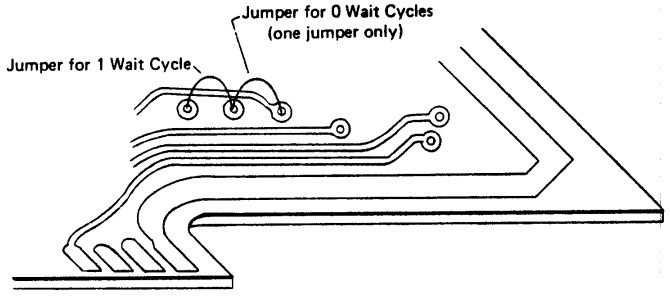
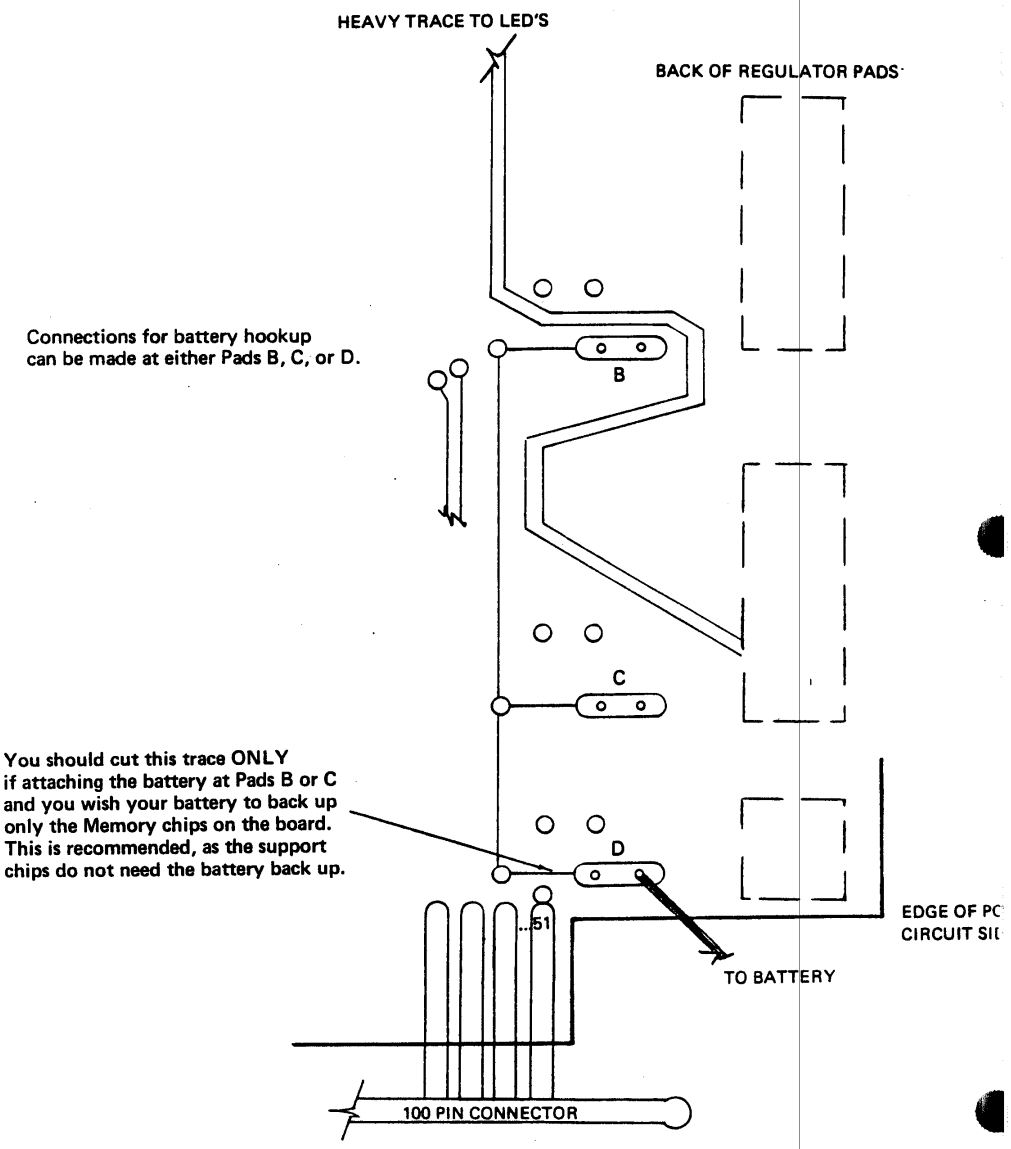


FIGURE 4

RAM 4A BATTERY HOOKUP DIAGRAM



This simple test program allows the operator to output protect and unprotect commands to the memory board under test when the memory board is addressed at location 00 hex, by using the sense switches on the front panel (high address switches). The program resides in the first 1K block of memory of the board that is actually under test.

The interrupt feature of the board may be tested by inserting a store accumulator (32 hex) instruction before the jump to 00 hex. By locating the address of where the data is to be stored in various 1K blocks of memory, an interrupt will be generated when that particular 1K block is given a protected status either from front panel switches or from software. NOTE: Interrupts should be enabled in your program.

INTERPRETATION OF ERRORS:

Phase I simply verifies that every location in RAM will correctly preserve data. The procedure is:

1. Write '00' in location F000.
2. Read location F000 and ensure that it is '00'.
3. Repeat 1-2 using values '01', '02',....'0F' and '10', '11',....'FF'.
4. Repeat 1-3 on F001, F002,....FFFF.

If an error occurs in Phase I, it indicates one of two hardware problems: a) a bad chip on the RAM board, or b) a bad data line (D0-D7) from the CPU to the RAM chip. The chip and a data line involved can be determined from the error data. Generally, case (b) will affect all locations in a chip or on the entire board, while case (a) will affect one locaiton or all locations on the chip. The cases can be distinguished by playing with DEPOSIT/EXAMINE and chip replacement.

Phases II and III are actually two parts of the same test. Phase I has already determined that location "n" (F000/n/FFFF) can hold data correctly (at least for a few microseconds). However, we have not yet proved that "n" references a unique location. Phases II and III verify this (and, in passing, prove that the RAM can hold a value for at least a few milliseconds).

Consider a RAM board in which address line is messed up in such a way that RAM always sees it as 0, regardless of its true state. Then RAM addressing will look like this:

```
True location F000 <-Referencing F000 will access this location
  "     "     F001          "      F001  "      "     "     "
  "     "     F002 <-       "      F002  "      "     "     "
  "     "     F003          "      F003  "      "     "     "
  ↓     ↓      ↓            ↓       ↓    ↓      ↓     ↓     ↓
True location FFFE <-Referencing FFFE will access this location
  "     "     FFFF          "      FFFF  "      "     "     "
```

Phase II will not detect this error.

It will write 00 through FF into F000 which it thinks is location F001. Since this actually accesses F000, the data will be read back correctly. So Phase I will succeed. Now comes Phase III. This starts by writing the low 8 bits of the address of each location into that location, i.e., 00 into FD20, 01 into F001,...., FF into FFFF. Then it goes back and reads this data, verifying it. Let's watch what happens with our bad address line.

The 4K board tester is at PROM location 0400H. The 1K tester is at 0500H.

TO USE:

1. Jumper the board to be tested to respond to addresses FxxxH.
2. Insert the board in an 8080 with CPU-A, CP-A and PROM containing the test routine.
3. Power the 8080 up. Set the switches to 0400H, press EXAMINE and press RUN.
4. The test routine will run, "Messages" are displayed in the 8 LED's labelled "programmed output" in the upper left corner of CP-A.

MESSAGES:

LED Display (Hex)	(Binary)	Meaning
01	00000001	Running Phase I test - no errors yet
02	00000010	Running Phase II test - no errors yet
03	00000011	Running Phase III test - no errors yet
F1	11110001	Error in Phase I: data will follow
F2	11110010	Error in Phase II: data will follow
F3	11110011	Error in Phase III: data will follow
FF	11111111	Test completed without errors: change any "programmed input" switch (#'s 8-15) to start test over.

ERROR PROCESSING:

When an error occurs, a "message" of F1, F2, or F3 will be displayed on the LED's. To get information on the errors:

1. Change one of switches 8-15.
2. The LED's will display the high 8 bits of the address at the location that failed.
3. Change one of switches 8-15.
4. The LED's will display the low 8 bits of the address.
5. Change one of switches 8-15.
6. The LED's will display the data that the location is supposed to contain.
7. Change one of switches 8-15.
8. The LED's will display the data the location actually contains.
9. Change one of switches 8-15.
10. The test will start over with Phase I.

```
:DBUG
IMSAI 8080 DEBUGGER 04/05/76

*0400,04FF;
0400   F3 3E FE D3  FF 21 00 F0  AF 77 46 B8  C2 56 04 3C
0410   C2 09 04 23  B4 C2 08 04  3E FD D3 FF  21 00 F0 74
0420   23 AF B4 C2  1F 04 21 00  F0 7E 94 C2  7C 04 23 B4
0430   C2 29 04 3E  FC D3 FF 21  00 F0 75 23  AF B4 C2 3A
0440   04 21 00 F0  7E 95 C2 88  04 23 B4 C2  44 04 3E FF
0450   21 00 04 C3  94 04 EB 4F  21 60 04 3E  F1 C3 94 04
0460   7A 21 67 04  C3 94 04 7B  21 6E 04 C3  94 04 79 21
0470   75 04 C3 94  04 78 21 00  04 C3 94 04  EB 82 47 4A    4K RAM TES
0480   3E F2 21 60  04 C3 94 04  EB 83 47 4B  3E F3 21 60    ENTRY: 04(
0490   04 C3 94 04  2F D3 FF F9  DB FF 67 DB  FF AC CA 9B
04A0   04 21 18 FC  23 AF B4 C2  A4 04 21 00  00 39 E9 FF
04B0   FF FF FF FF  FF FF FF FF  FF FF FF FF  FF FF FF FF
04C0   FF FF FF FF  FF FF FF FF  FF FF FF FF  FF FF FF FF
04D0   FF FF FF FF  FF FF FF FF  FF FF FF FF  FF FF FF FF
04E0   FF FF FF FF  FF FF FF FF  FF FF FF FF  FF FF FF FF
04F0   FF FF FF FF  FF FF FF FF  FF FF FF FF  FF FF FF FF
*0500,05FF;
0500   F3 3E FE D3  FF 21 00 F0  AF 77 46 B8  C2 5B 05 3C
0510   C2 09 05 23  7C FE F4 C2  08 05 3E FD  D3 FF 21 00
0520   F0 74 23 7C  FE F4 C2 21  05 21 00 F0  7E 94 C2 81
0530   05 23 7C FE  F4 C2 2C 05  3E FC D3 FF  21 00 F0 75
0540   23 7C FE F4  C2 3F 05 21  00 F0 7E 95  C2 8D 05 23
0550   7C FE F4 3E  FF 21 00 05  C3 99 05 EB  4F 21 65 05
0560   3E F1 C3 99  05 7A 21 6C  05 C3 99 05  7B 21 73 05
0570   C3 99 05 79  21 7A 05 C3  99 05 78 21  00 05 C3 99    1K RAM TES
0580   05 EB 82 47  4A 3E F2 21  65 05 C3 99  05 EB 83 47    ENTRY: 05C
0590   4B 3E F3 21  65 05 C3 99  05 2F D3 FF  F9 DB FF 67
05A0   DB FF AC CA  A0 05 21 18  FC 23 AF B4  C2 A9 05 21
05B0   00 00 39 E9  FF FF FF FF  FF FF FF FF  FF FF FF FF
05C0   FF FF FF FF  FF FF FF FF  FF FF FF FF  FF FF FF FF
05D0   FF FF FF FF  FF FF FF FF  FF FF FF FF  FF FF FF FF
05E0   FF FF FF FF  FF FF FF FF  FF FF FF FF  FF FF FF FF
05F0   FF FF FF FF  FF FF FF FF  FF FF FF FF  FF FF FF FF
*
```

TRUE LOC.	CONTENTS	RESPONDS TO:	
F000	00	F000, F001	Step 1: Write 00 into F000
F001	?	nothing	
F000	01	F000, F001	Step 2: Write 01 into F001
F001	?	nothing	
F000	1	F000, F001	Step 4097: Read F000,
F001	?	expecting nothing - and detect an error.	

Thus, Phase III detects our error. Now for some observations on how to find the error.

1. Between steps 1 and 4097, several milliseconds pass without accessing location F000. If RAM is volatile, the data in F000 could go away and generate a Phase III error. This can be found by DEPOSITing into the bad location and EXAMINEing it to see if it changes. The reason Phase I doesn't catch this is that it reads 3.5 μs after it writes, so the data doesn't have time to deteriorate.

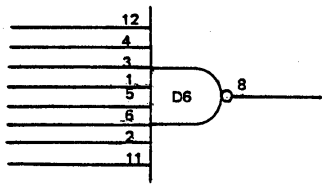
2. If address line 0 were stuck at 1, the same results would appear in Phase III. (Try it.) You can't tell from this test what the line is stuck at.

3. If Phase II or III fails, the bad address bits are the ones where the "supposed to be" data and the "read back" data differ. If the error was Phase II, these represent the high 8 bits of address. If the error was Phase III, these represent the low 8 bits.

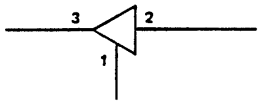
ERRATA RAM 4A Rev. 2 SCHEMATIC

1. The six diodes CR1 through CR6 are NOT Zener diodes as shown by the symbol.

2. At chip D6 the input lines should read:



3. Pin configurations on C2 and C3 should read:



4. Chip positions on 2102's are labelled wrong and should read from TOP to BOTTOM and LEFT to RIGHT:

A16	A8	B16	B8
A15	A7	B15	B7
A14	A6	B14	B6
A13	A5	B13	B5
A12	A4	B12	B4
A11	A3	B11	B3
A10	A2	B10	B2
A9	A1	B9	B1

Errata
2/4/77

RAM 4A-4

NOTE: The RAM 4A Chapter applies to both RAM 4A-4, Rev. 2 and RAM 4A-4, Rev. 3.

RAM 4A BOARD

THEORY OF OPERATION

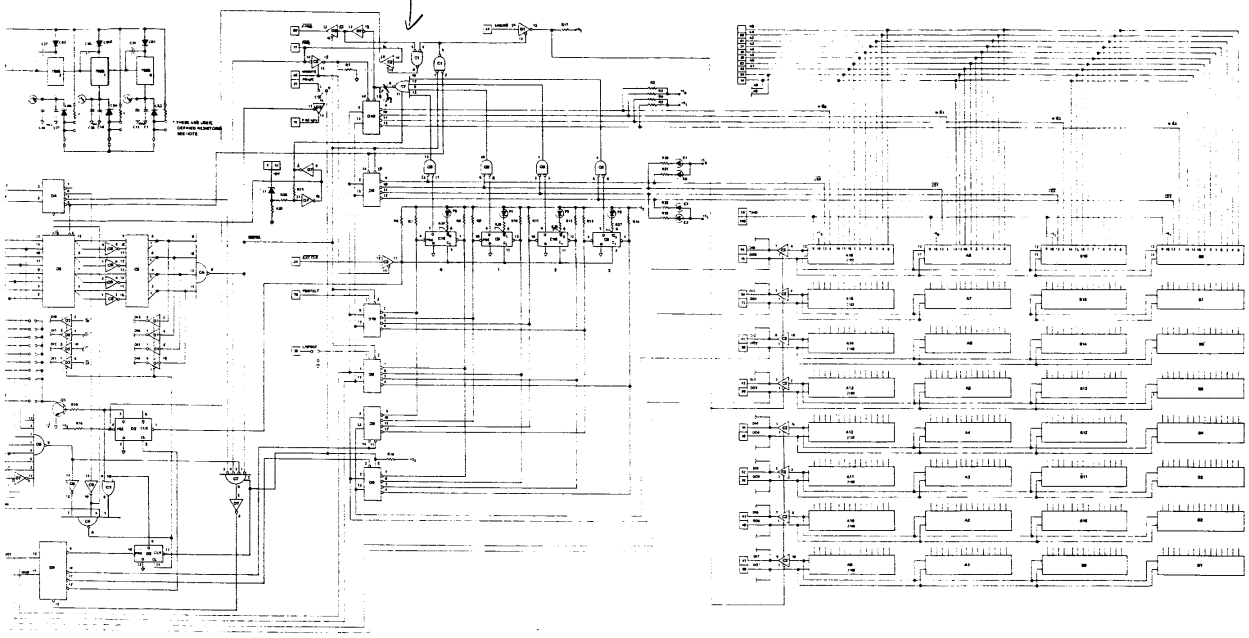
The memory circuits used on the IMSAI RAM 4A memory board are 2102-style integrated circuits housed in sixteen pin DIP packages. Their organization is 1024 words, each of which is one bit wide. Ten address inputs are used to select the desired word and there is a chip enable to select the chip. There is a read/write input. One input is provided for data in, and one output is provided for data out. To implement the storage of data words that are eight bits wide, eight of the above described chips are used to store 1024 words. Three more of these eight chip groups can be used to give the IMSAI RAM 4A memory board a maximum storage capacity of 4096 eight bit words.

Bits A9, A8, A7, A6, A5, A4, A3, A2, A1, and A0 of the address bus come onto the memory board and go directly to the appropriate address pins on each memory chips. Bits A11 and A10 are decoded by a section of the 74LS156 at location D8 to select the desired 1024 word block by assertion of the chip enable signal for only those eight memory chips comprising the desired 1024 word block.

Bits A15, A14, A13, and A12 of the address bus are used to give each memory board on the bus a unique address. These bits first go through (if the memory board is involved in the utilization of its memory function through a memory-read operation, or memory write operation) the 74LS157 data selector at location D5. The direct output, and the complement of the direct output (obtained through the 74LS04 inverters at location C6) of the four output pins of the 74LS157 at location D5 go to DIP jumper provision at location C5. Provision is made so that either the equivalant polarity, or its complement, of the above mentioned four address bits can be implemented through the correct use of jumpers at location C5. When the polarity of the above-mentioned four address bits are in such an arrangement that they satisfy the address requirements of a particular memory board the four input pins of a section of the 74LS20 at location C4 will be high. This effects the selection of an individual memory board. Thus, only one board should respond in this manner for each of the sixteen different polarity arrangements of these four address bits.

Each 1024 word block of memory has its own circuitry to implement the write-protect feature. This feature is manipulated in two ways. One is from the "PROTECT/UNPROTECT" switch on the front panel. The other is from program commands contained in software.

There are four flip/flops whose two states enable or prevent the changing of the contents of their respective 1024 word blocks when a memory write is received. Each of these four flip/flops is a section of a 74LS74 at location C10 and at location C9. Memory block 0 is controlled by half of C9, memory block 2 is controlled



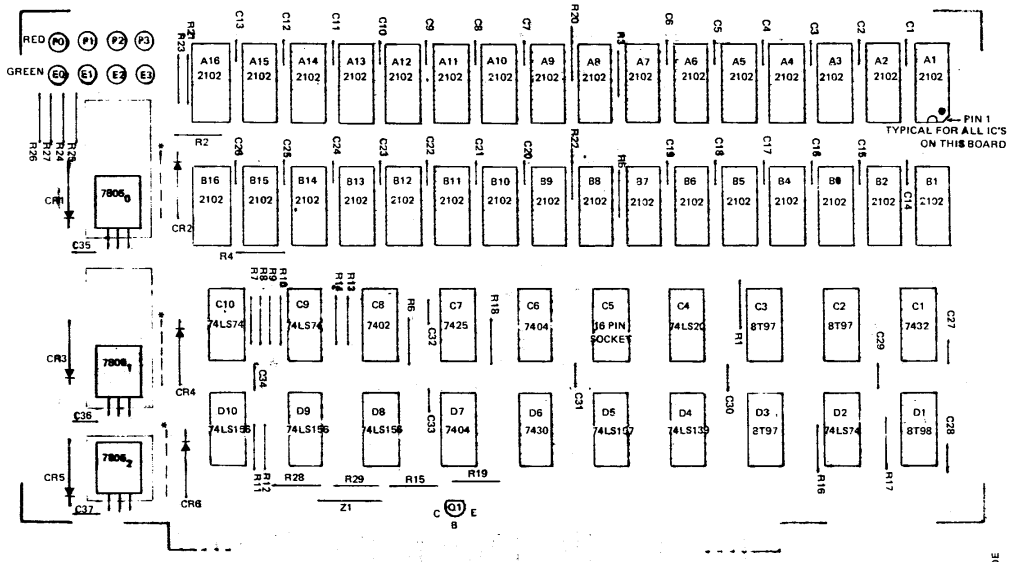
0 REV. 2
1 MOD & UPD.

A1 thru A16
B1 thru B16
C1
C2 C3
C4
C5
C6
C7
C8
C9 C10
D1
D2
D3
D4
D5
D6
D7
D8 D9 D10
C1 thru C34
C35 thru C37
CR1 thru CR6
Z1
Q1
R1 thru R18
R19 thru R28
R29
E0 thru E3
P0 thru P3

NOTE :
* THESE ARE USER DEFINED RESISTORS. REFER TO USERS GUIDE FOR EXPLANATION.

APPROVALS
DRAWN
CHECKED

LTR	DESCRIPTION
0	REV.2
1	MOD & UPDATE
2	REV.3



C5 is a 16 Pin Ju
All Capacitors ar
C35 thru C3
Diodes CR1 thru
Diode Z1 is 1N7
Transistor Q1 is
LED's E0 thru E
P0 thru P
Resistors are ¼ V
R1 thru R18 a
R19 thru R28
R29 is 100 Oh

NOT SUPPLIED *

NOTE: THESE ARE USER DEFINED RESISTORS
SEE USER GUIDE SECTION FOR EXPLANATION

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC. ANGLES		IMSAI SAN L
± ± ±		
APPROVALS	DATE	RAM4 ASSE
DRAWN RCU	2/77	
CHECKED		SCALE SI E
		DO NOT SCALE