4K RAM BOARD

DOCUMENTATION

CONTENTS

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"Creative Electronics"

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ALBUQUERQUE, NEW MEXICO 87108

THEORY of OPERATION

88-4MCD 4K DYNAMIC RAM BOARD OPERATION

The 4K RAM Board provides 4,096 words of Dynamic Random Access Memory for the ALTAIR 8800. Each individual board contains memory protect circuitry, and address selection circuitry for any one of 16 starting address locations in increments of 4K. The maximum access time is 300 nanoseconds; thus, there is no "wait" requirement unless Refresh is occurring at the time of access.

Refresh

This memory board is designed around a dynamic integrated circuit, TMS 4030 or C2107A IC's. These dynamic IC's require each row within the chip to be accessed every 2 milliseconds or less. This is accomplished by accessing one of the 64 rows every 64 clock pulses (32 microseconds).

The Ø2 clock is buffered through one gate of IC S and then inverted through one gate of IC A. It is then divided in half through flip-flop Ta, and divided again by 16 through a 4-bit counter (IC D). The final signal is fed to the clock input of flip-flop Ga. Thus, after 32 clock pulses Ga will toggle, and will toggle again after another 32 clock pulses. This will add one count to the 6-bit counter, IC's E & F, which sets up the refresh address at the inputs of IC O.

Ga is also used to trigger single-shot Ha. This partially enables IC K pin 11 and toggles flip-flop Gb, partially enabling IC K pin 3.

If the computer is in the run mode, a SYNC pulse, inverted through one gate of IC A, will occur within approximately 10 microseconds. This causes IC K pin 11 to go low for 500 nanoseconds and IC K pin 3 to go high for 500 nanoseconds. On the falling edge of this pulse, single-shot Ia is triggered. The pulse from IC Ia pin 13 disables the machine address and triggers IC Ib. The IC Ia pin 4 output is delayed less than 100 nanoseconds and fed to the chip-enable voltage level shift circuit (4 gates of IC Z, Q1, R1, R2, D1 & C1) and also clears flip-flop Gb.

The output of this circuit provides a 500 nanosecond, +12 volt pulse to the RAM IC's to accomplish the required access.

If the machine had been in a stop mode when the refresh pulse occured, there would have been no SYNC pulse. In this case refresh would have occured with the falling edge of the pulse from IC Ha, approximately 12 microseconds later.

The function of IC Ib is to disable the read-write single-shot, IC Hb, and to pull the Ready line active if the card is accessed during refresh. This puts the machine is a wait state until refresh has been accomplished. IC Hb is then triggered for a normal read or write.

Read

IC Hb is partially enabled by MEMR. When SYNC and Q1 occur, if refresh is not occuring keeping IC J pin 4 low, then IC K pin 8 goes low and pulls IC J pin 6 high. Approximately 90 nanoseconds later Q1 returns low, IC K pin 8 goes high and IC J pin 6 goes low triggering IC Hb. This pulls chip enable (CE) high for 500 nanoseconds.

After approximately 300 nanoseconds the data out of the RAM chips is valid. It is latched into the 8-bit latch (IC N) via the strobe input, IC N pin 11, by IC Hb pin 5.

The final requirement to place the data onto the bus is with the latch enable inputs, pins 1 & 13 of IC N. Pin 1 is pulled low by IC J pin 8 (card select) and pin 13 is pulled high by MEMR. This enables the latch outputs and presents the data to the bus.

Write

The write mode is identical to the read mode, except that the latch outputs are not enabled and the write inputs to the RAMS are activated.

The MWRITE signal partially enables the read-write single-shot, IC Hb, and is also gated with the output of Hb to IC L pins 9 & 10. When both signals are high (active) IC L pin 8 goes low. If memory is unprotected (IC M pin 6), IC M pin 4 goes high and IC A pin 4 goes low.

This pulls the write input of the memory chips to the low active write mode while at the same time chip enable is high (Hb pin 12) and the data (buffered and inverted through IC's R & Z) is present at the RAM data inputs.

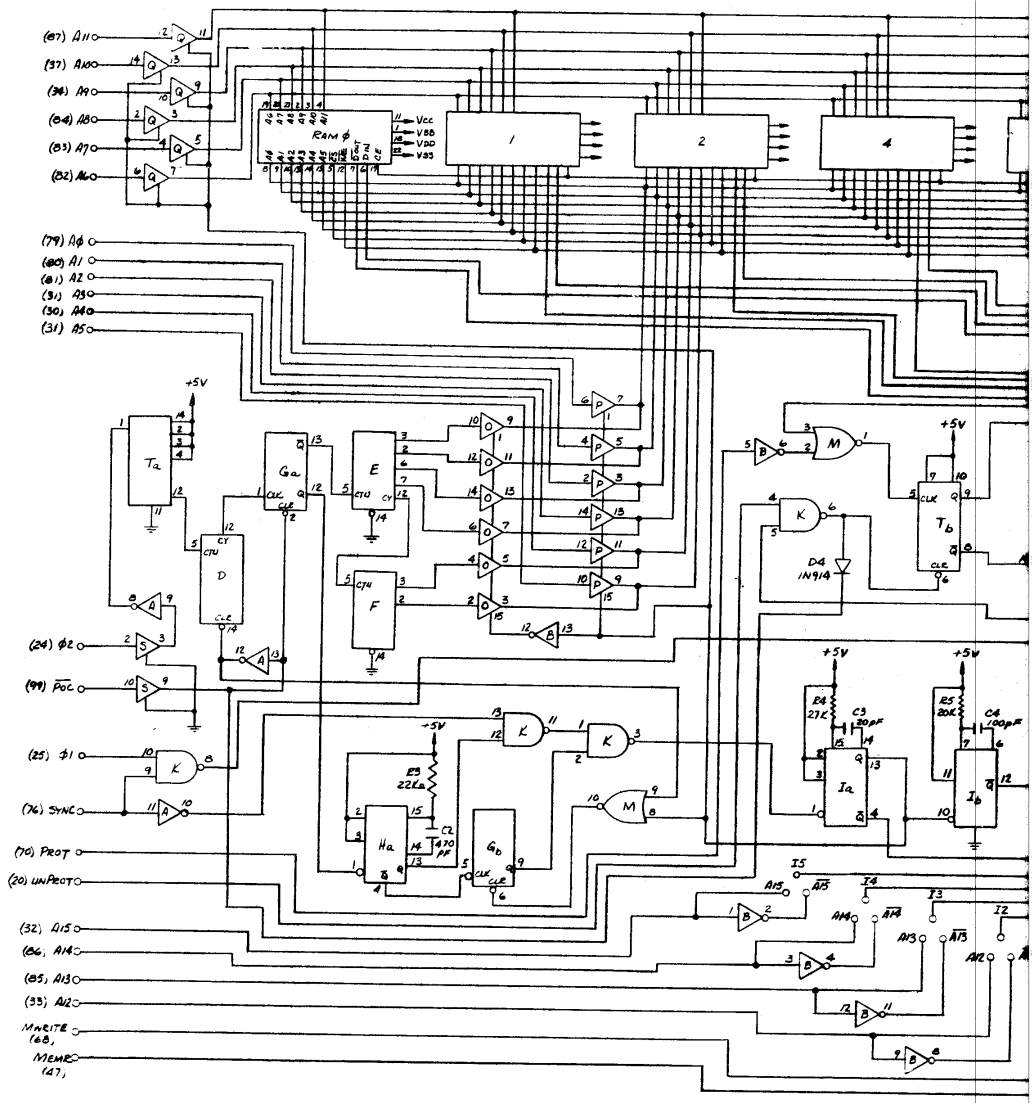
Protect

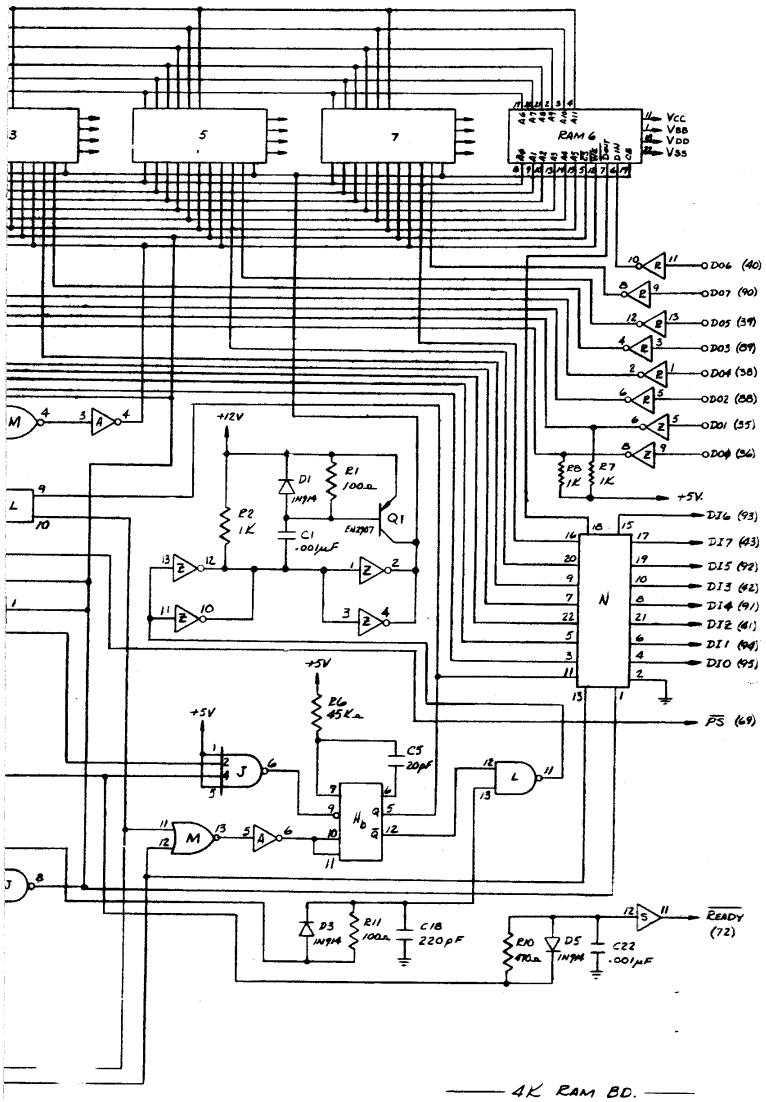
The entire 4,096 words of memory on the board can be protected via the front panel PROTECT switch.

When the card is selected (IC M pin 3) and the switch lifted to the PROTECT position (IC M pin 2), the output of IC M pin 1 toggles the flip-flop Tb. This pulls IC M pin 6 high to disable the write input to the RAMS, and pulls buffer IC S pins 13 & 14 low to light the PROTECT light on the front panel.

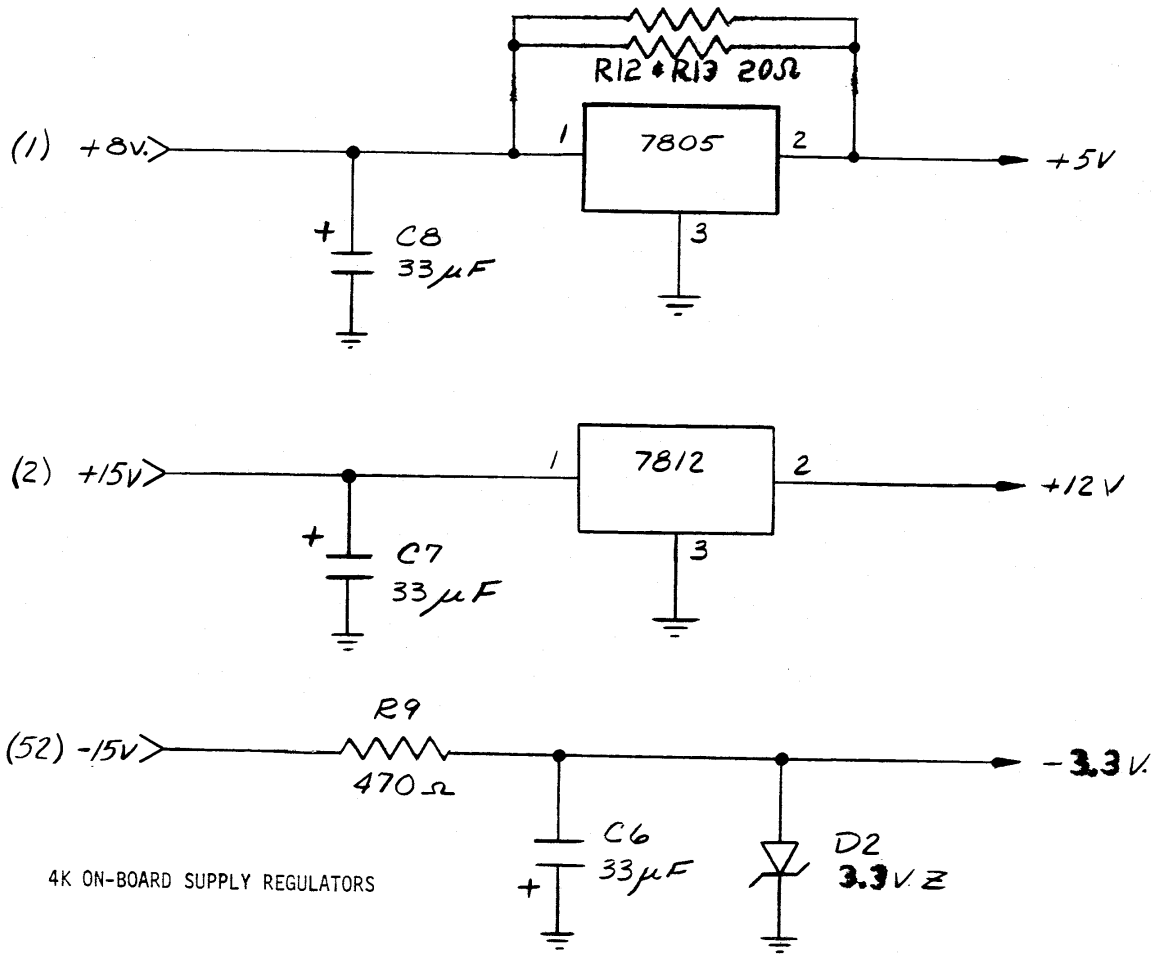
The memory will remain protected until power is turned off or the PROTECT switch is pushed to the UNPROTECT position.

When power is first applied to the unit the $\overline{\text{POC}}$ signal (Power On Clear) is pulled low for several milliseconds, insuring that the memory is unprotected.


(67) A11
(37) A10
(36) A9
(34) A8
(33) A7
(32) A6
(79) A0
(80) A1
(81) A2
(1) A3
(30) A4
(31) A5
Ram 0
Vcc
VSS
VDD
VBB
1
2
4
+5V
Ta
Ga
E
D
F
Tb
M
K
D4
1N914
(24) Φ2
(99) POC
(25) Φ1
(76) SYNC
(70) PROT
(20) UNPROT
(32) A15
(66) A14
(65) A13
(33) A12
MWRITE
(68)
MEMR
(47)
R3
22Ka
C2
470
PF
Ha
Gb
R4
27K
C3
20PF
R5
20K
C4
100PF
Ia
Ib
I5
I4
I3
I2
A15
A14
A13
A12


RAM 6
Vcc
VBB
VDD
Vss
DO6 (40)
DO7 (90)
DO5 (39)
DO3 (89)
DO4 (38)
DO2 (88)
DO1 (35)
DO0 (36)
+5V.
DI6 (93)
DI7 (43)
DI5 (92)
DI3 (42)
DI4 (91)
DI2 (41)
DI1 (90)
DI0 (95)
PS (69)
+12V
D1 IN914
R1 100Ω
R2 1K
C1 .001μF
Q1 2N2907
R8 1K
R7 1K
+5V
R6 45KΩ
C5 20pF
R11 100Ω
C18 220pF
D3 IN914
R10 470Ω
D5 IN914
C22 .001μF
READY (72)

4K RAM BD.



4K ON-BOARD SUPPLY REGULATORS

8800 ERRATA SHEET

August 8, 1975

DISPLAY/CONTROL BOARD CAPACITOR MODIFICATIONS

NOTE: THE FOLLOWING CAPACITOR VALUE SUBSTITUTIONS ARE CRITICAL IN THE OPERATION OF AN ALTAIR SYSTEM USING 4K DYNAMIC MEMORY BOARDS. THE NECESSARY CAPACITORS WILL BE INCLUDED WITH EACH ALTAIR KIT AND WITH EACH 4K MEMORY BOARD KIT, BUT THE SUBSTITUTIONS NEED BE PERFORMED ONLY ONCE. PERFORM THE SUBSTITUTIONS WHETHER YOU HAVE 4K BOARDS OR NOT.

THE FOLLOWING CAPACITORS ON THE DISPLAY/CONTROL BOARD ARE TO BE CHANGED TO THE VALUES INDICATED BELOW:

C7 should now be 0.01μf

C8 should now be 0.1μf

THESE SUBSTITUTIONS ARE TO IMPROVE THE OPERATION OF THE ALTAIR'S DEPOSIT CIRCUITRY.

4K DYNAMIC RAM BOARD

ASSEMBLY PROCEDURE

MITS INC.

4K DYNAMIC RAM BOARD ASSEMBLY

Integrated Circuit Installation

There is a total of 28 integrated circuits (IC's) to be installed on the 8800 4K RAM Board (88-4MCD). The eight memory IC's will be installed later in the assembly procedure. The other 20 IC's should be installed at this time, according to the following procedure.

( ) Referring to the component layout, remove the IC with the correct part number from its holder. If there are any bent pins, straighten these using needle-nose pliers. Ensure that you choose the IC with the correct part number.

( ) Orient the IC so that its notched end corresponds with the notch printed on the board, and pin 1 of the IC corresponds with the arrowhead printed on the board.

NOTE: If the IC does not have a notch on one end, refer to the IC Orientation Chart included in your manual for the identification of pin 1.

( ) When you have the correct orientation, start the pins on one side of the IC into their respective holes on the silk-screened side of the PC Board. DO NOT PUSH THE PINS IN ALL THE WAY. If you have difficulty getting the pins into the holes, use the tip of a small screwdriver to guide them.

( ) Start the pins on the other side of the IC into their respective holes in the same manner. When all of the pins have been started, set the IC into place by gently rocking it back and forth until it rests as close as possible to the board. Make sure that the IC is perfectly straight and as close to the board as possible; then tape it in place with a piece of masking tape.

( ) Turn the board over and solder each pin of the IC to the foil pattern on the back side of the board. Be sure to solder each pin and be careful not to leave any solder bridges.

( ) Turn the board over again and remove the piece of masking tape.

Use the same procedure to install each of the IC's. Be sure that you have the correct part number and the correct orientation as you install each one.

( ) IC's A, B & R are 74L04's

( ) IC D is a 74193

( ) IC's F & E are 74L193's

( ) IC's G & T are 7473's

( ) IC's H & I are AM26L123's

( ) IC J is a 7420

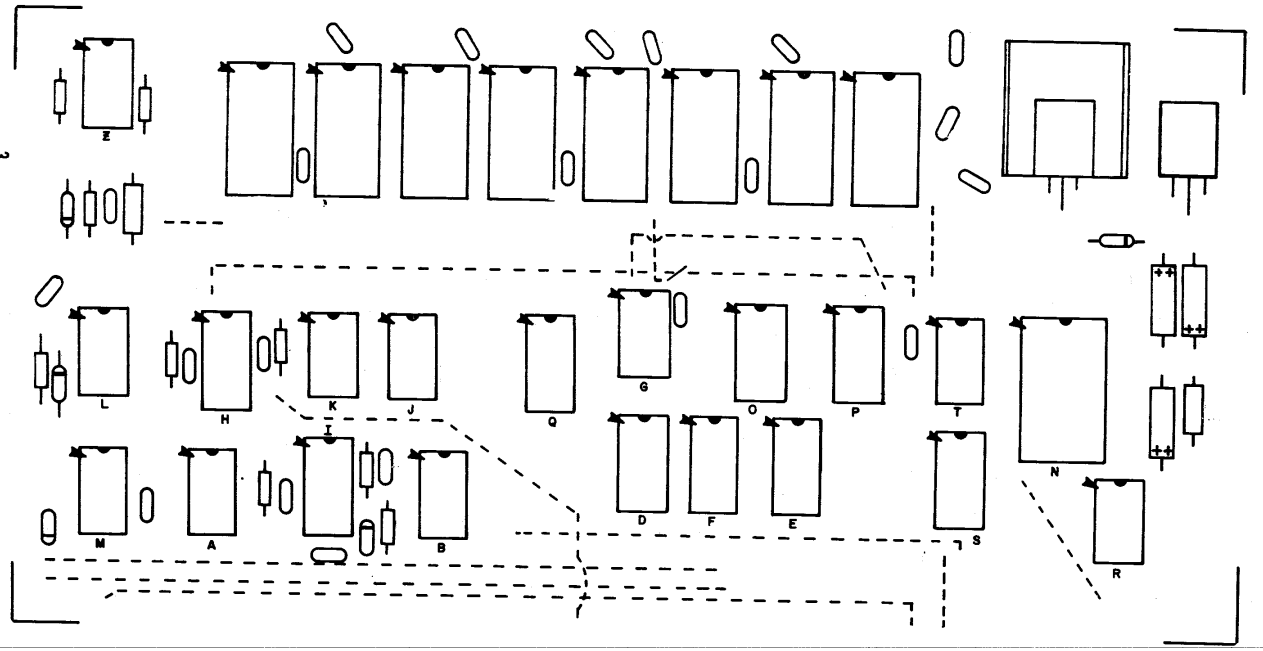
( ) IC M is a 74L02

( ) IC N is an 8212

( ) IC's O, P, Q & S are 8T97's

( ) IC's L & K are 7400's

( ) IC Z is a 7406



Resistor Installation

There are 11 resistors to be installed on the 8800 4K RAM Board.

NOTE: Resistors are color coded according to their value. The resistors in your kit will have four or possibly five bands of color. The fourth band in both cases will be gold or silver, indicating the tolerance. In the following instructions we will be concerned only with the three bands of color to one side of the gold or silver band. Be sure to match these three bands of color with those called for in the instructions as you install each resistor.

Using needle-nose pliers, bend the leads of the following resistors at right angles to match their respective holes on the PC board. (see component layout)

NOTE: All resistors on the 4K RAM Board may be either 1/4 or 1/2 Watt; except resistor R9, which must be 1/2 Watt.

( ) Install resistor R1 (100-ohm, brown-black-brown) into the correct holes on the silk-screened side of the PC board.

( ) Holding the resistor in place with one hand, turn the board over and bend the two leads slightly outward.

( ) Solder the leads to the foil pattern on the back side of the board; then clip off any excess lead lengths.

Referring to the component layout, install the remaining resistors in the same manner. Be sure you have the correct color-coding for each one as you install them.

NOTE: Save the component leads that you clip off for use later in the assembly procedure.

( ) R11 is 100-ohms, brown-black-brown

( ) R2, R7 & R8 are 1K-ohms, brown-black-red

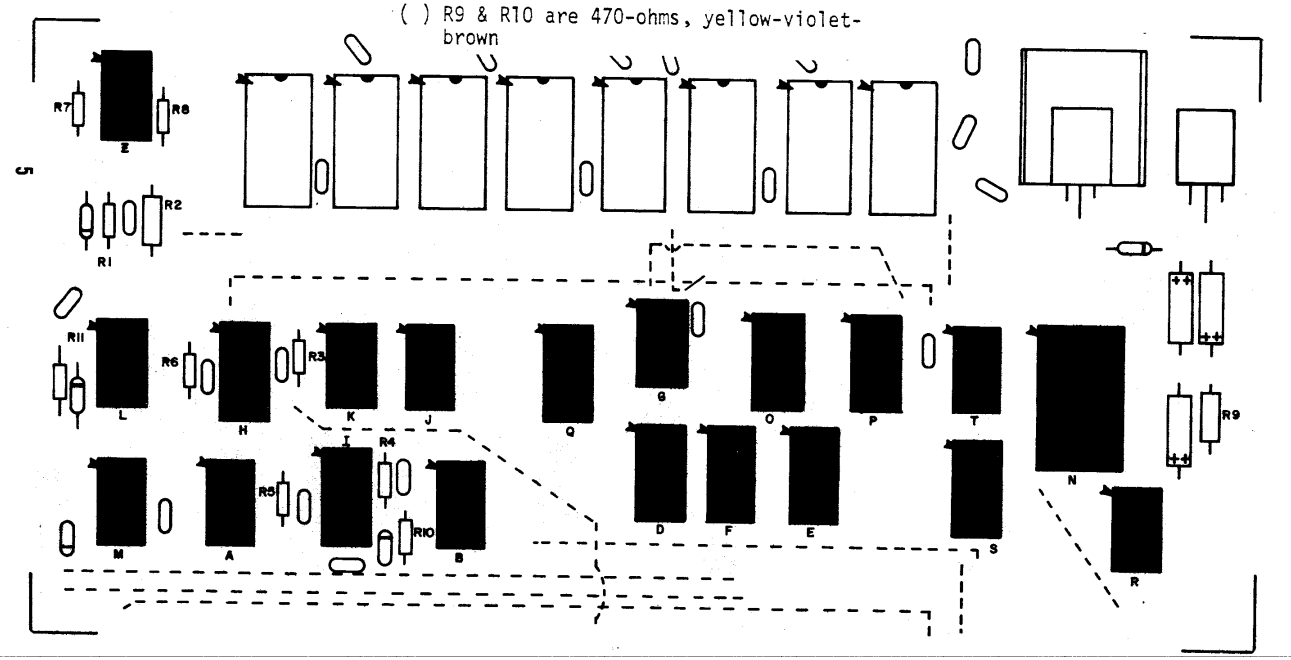
( ) R3 is 22K-ohms, red-red-orange

( ) R4 is 27K-ohms, red-violet-orange

( ) R5 is 20K-ohms, red-orange

( ) R6 is ~~43~~ 30K-ohms, yellow-orange-orange

( ) R9 & R10 are 470-ohms, yellow-violet-brown



Capacitor Installation

There are 21 ceramic disk capacitors and 3 electrolytic capacitors to be installed on the 8800 4K RAM Board.

Refer to the component layout and install the ceramic disk capacitors according to the following procedure.

( ) Choose the capacitor with the correct value as called for in the instructions. Straighten the two leads as necessary and bend them to fit their respective holes on the PC board.

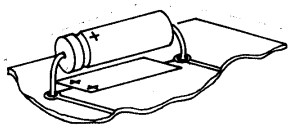
( ) Insert the capacitor into the correct holes from the silk-screened side of the board. Push the capacitor down until the ceramic insulation almost touches the foil pattern.

( ) Holding the capacitor in place, turn the board over and bend the two leads slightly outward.

( ) Solder the two leads to the foil pattern on the back side of the board; then clip off any excess lead lengths.

Install all of the ceramic disk capacitors in this manner. Be sure that you have the correct value capacitor as you install each one.

The three electrolytic capacitors for the 4K RAM Board have polarity requirements which must be noted before installation. Those contained in your kit may have one or possibly two of three types of polarity markings. To determine the correct orientation, look for the following: (see drawing above right)



ELECTROLYTIC CAPACITOR

One type will have plus (+) signs on the positive end; another will have a band or a groove around the positive side in addition to the plus signs. The third type will have an arrow on it; in the tip of the arrow there is a negative (-) sign and the capacitor must be oriented so the arrow points to the negative polarity side.

Referring to the component layout, install the electrolytic capacitors on the board.

( ) Bend the two leads of the capacitor with the correct value at right angles to match their respective holes on the board. Insert the capacitor into the holes on the silk-screened side of the board. Be sure to align the positive polarity side with the "+" signs printed on the board.

( ) Holding the capacitor in place, turn the board over and bend the two leads slightly outward. Solder the leads to the foil pattern and clip off any excess lead lengths.

( ) Install the remaining electrolytic capacitors in the same manner.

( ) C1 & C22 are .001uf

( ) C2 is 470pf

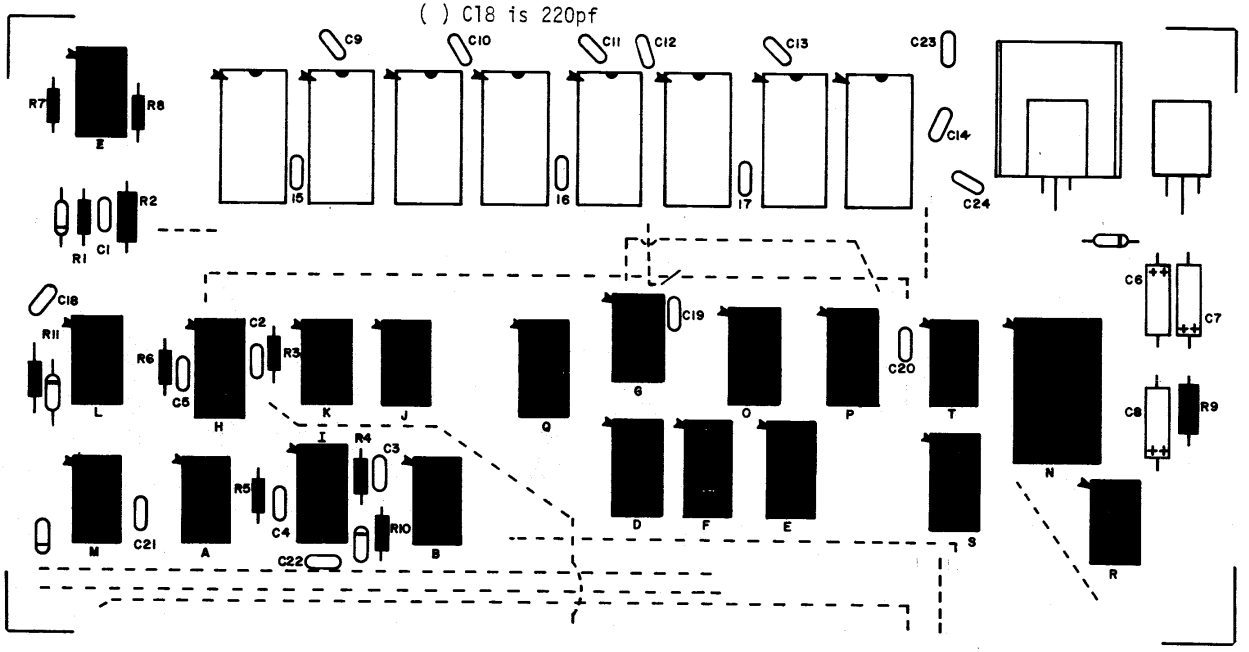
( ) C3 & C5 are 20pf

( ) C4 is 100pf

( ) C6, C7 & C8 are 35uf

( ) C9 through C17, C19 through C21, and C23 & C24 are .1uf

( ) C18 is 220pf

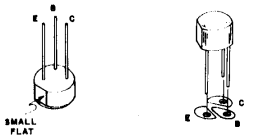


Transistor Installation

There is 1 PNP, EN2907 transistor to be installed on the 8800 4K RAM Board.

NOTE: When installing this transistor, ensure that you check the part number before soldering it into place. Some transistors are identical in physical appearance but differ in electrical characteristics. If the part number on the transistor does not match the number called for in the instructions, it may be that you have substitutions. In this case refer to the Transistor Identification Chart included with your manual.

( ) This transistor is rounded and has a flat edge near one of the leads. The lead nearest this flat edge is called the emitter. The hole for the emitter is marked with an "E" on the board, next to the transistor Q1 designation. If the emitter lead is placed into this hole, the other two leads should fit into their holes with little or no bending and should not cross over each other. (see drawing below)



( ) Orient Q1 so that the lead nearest the flat edge aligns with the correct hole on the board. Insert the transistor into the holes from the silk-screened side of the board.

( ) Holding the transistor in place, turn the board over and bend the three leads slightly outward.

( ) Solder the leads to the foil pattern on the back side of the board; then clip off any excess lead lengths.

Diode Installation

There are four 1N914 diodes and one 3.3v (1N746A) zener diode to be installed on the 8800 4K RAM Board.

NOTE: Diodes are marked with a band on one end indicating the cathode end. The diode must be oriented so that the end with the band is towards the band printed on the board when being installed.

( ) Referring to the component layout, bend the leads of diode D1 (1N914) at right angles to match the correct holes on the board.

( ) Insert the diode into the correct holes from the silk-screened side of the board. Turn the board over and bend the two leads slightly outward.

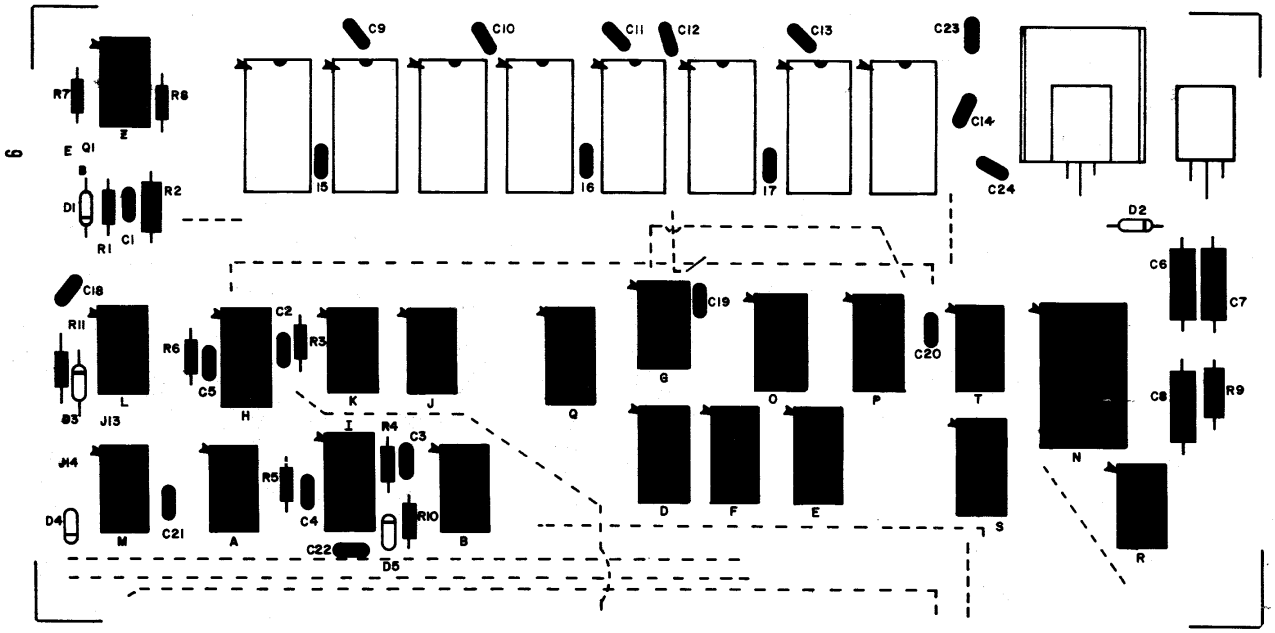
( ) Solder the leads to the foil pattern on the back side of the board; then clip off any excess lead lengths.

Install zener diode D2 and the remaining 1N914 diodes, D3, D4 & D5, in the same manner. Be sure that the band on the diode is aligned with the band printed on the board as you install them. Failure to orient these diodes correctly may result in permanent damage to your unit.

( ) Q1 is an EN2907

( ) D1, D3, D4 & D5 are 1N914's

( ) D2 is a 1N746A



PC Jumper Wire Connections

There are 17 hardwire jumper connections to be made on the 8800 4K RAM Board.

These jumpers are indicated on the PC board in two manners. The first twelve are indicated by the two pads to be connected having the same designation and shown connected by a broken line printed on the board. The remaining five are indicated simply by the two pads to be connected having the same designation.

Cut the wire for each jumper to the correct length for each connection allowing an extra 1/2 inch. Strip 1/4 inch of insulation from both ends of each wire and tin them by applying a thin coat of solder to the uninsulated portion.

NOTE: It is very important for the operational performance of this board to keep the length of these jumper wires as short as possible. Any excess wire lengths may create "noise" and influence critical timing operations.

Make each of the following connections by inserting the wires from the silkscreened side of the board and soldering them to the foil pattern on the back side. Be sure to clip off any excess lead lengths as you install each jumper.

NOTE: Jumpers J1, J7, J8 & J12 should be made using the heavier guage wire included with your kit.

( ) Connect J1 to J1

( ) Connect J2 to J2

( ) Connect J3 to J3

( ) Connect J4 to J4

( ) Connect J5 to J5

( ) Connect J6 to J6

( ) Connect J7 to J7

( ) Connect J8 to J8

( ) Connect J9 to J9

( ) Connect J10 to J10

( ) Connect J11 to J11

( ) Connect J12 to J12

( ) Connect J13 to J13

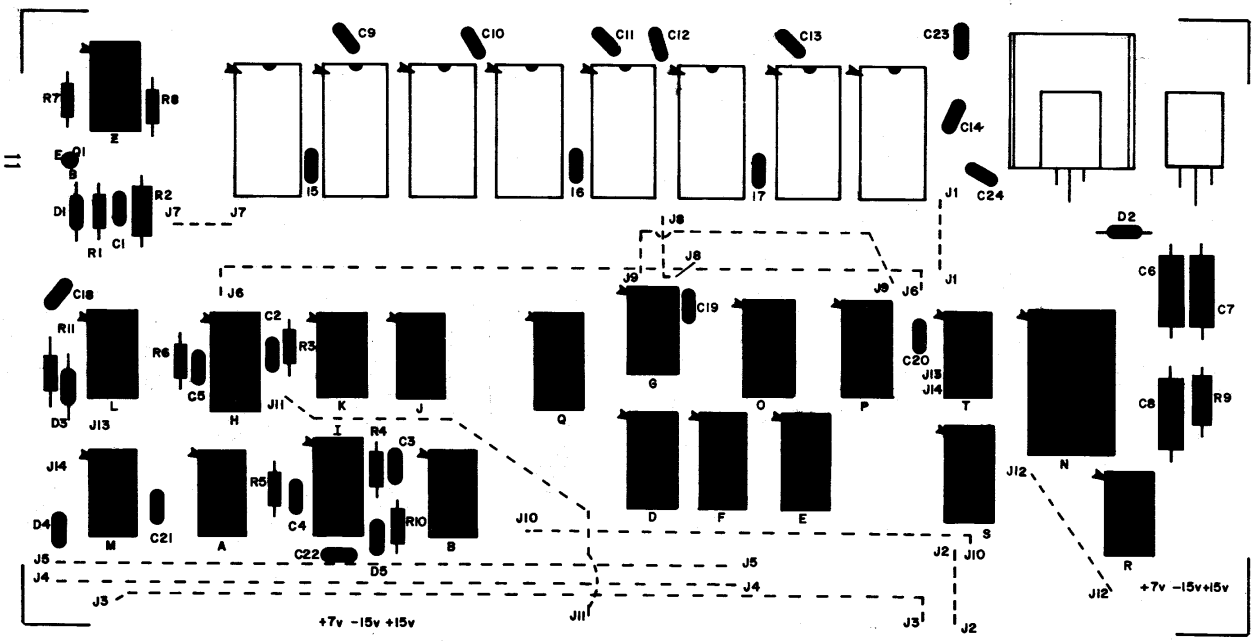
( ) Connect J14 to J14

( ) Connect +7v to +7v

( ) Connect -15v to -15v

( ) Connect +15v to +15v

( ) Install all 17 jumpers as per the instructions.



Voltage Regulator Installation

There is one 7805 5-volt regulator and one 7812 12-volt regulator to be installed on the 8800 4K RAM Board.

( ) Set the 7805 (VR5) in place on the board and align the mounting holes. (see drawing)

( ) Use a pencil to mark the point on each of the three leads where they line up with their respective holes on the board.

( ) Use needle-nose pliers to bend each of the three leads at a right angle on the points where you made the pencil marks.

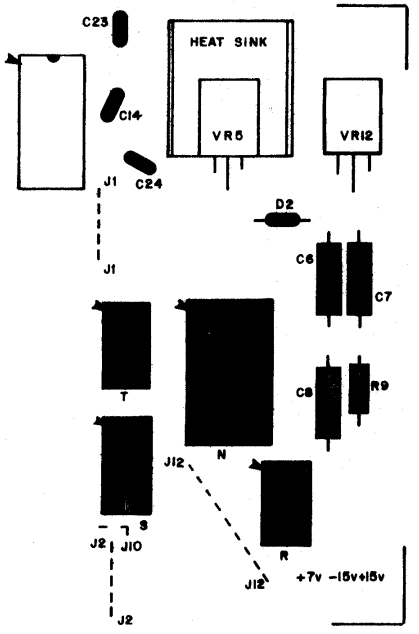
NOTE: Use heat-sink grease when installing these components. Apply the grease to all surfaces which come in contact with each other.

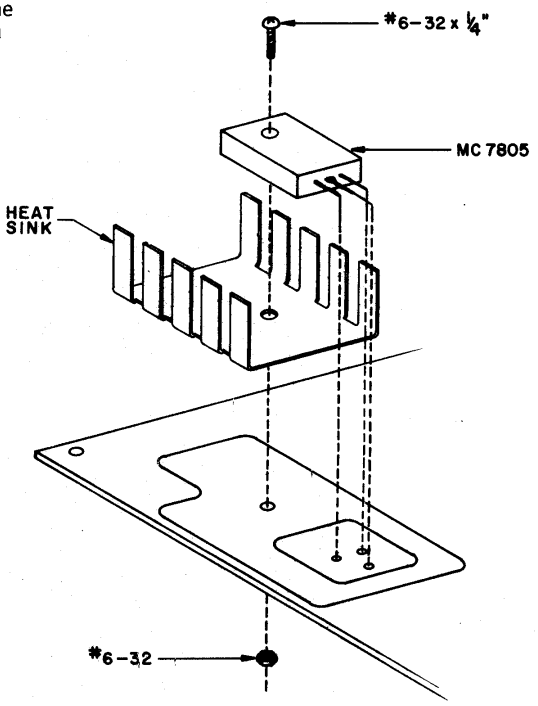
( ) Referring to the drawing, set the regulator and heat sink in place on the silk-screened side of the board. Secure them as shown, holding the regulator in place as you tighten the nut to keep from twisting the leads.

( ) Turn the board over and solder the three leads to the foil pattern on the back side of the board. Be sure not to leave any solder bridges.

( ) Clip off any excess lead lengths.

( ) Install the 7812 (VR12) in the same manner; except there is no heat sink to be installed with this regulator.





MOS Integrated Circuit Installation

There are eight MOS Integrated Circuits (IC's) to be installed on the 8800 4K RAM Board.

These IC's are very sensitive to static electricity and transient voltages. In order to prevent damage to these components review the information contained in the MOS IC SPECIAL HANDLING PRECAUTIONS included with your manual.

( ) Referring to the component layout, remove the IC with the correct part number from its holder. If there are any bent pins, straighten these using needle-nose pliers. Ensure that you choose the IC with the correct part number.

( ) Orient the IC so that its notched end corresponds with the notch printed on the board, and pin 1 of the IC corresponds with the arrowhead printed on the board.

NOTE: If the IC does not have a notch on one end, refer to the IC Orientation Chart included in your manual for the identification of pin 1.

( ) When you have the correct orientation, start the pins on one side of the IC into their respective holes on the silk-screened side of the PC board. DO NOT PUSH THE PINS IN ALL THE WAY. If you have difficulty getting the pins into the holes, use the tip of a small screwdriver to guide them.

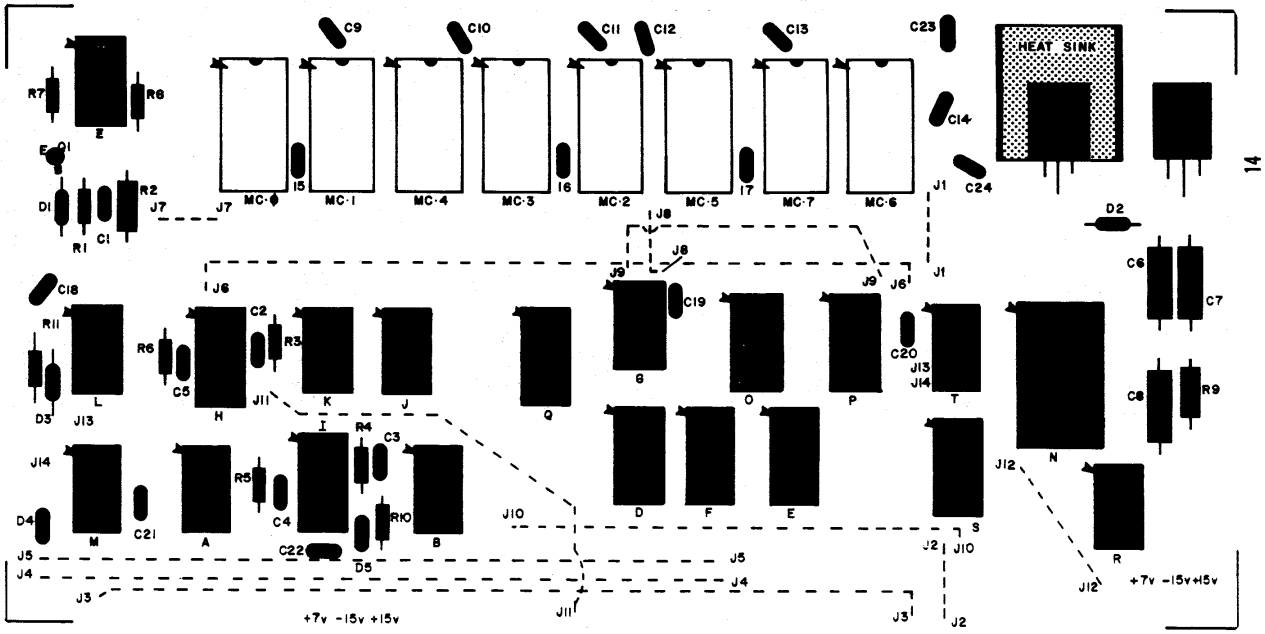
( ) Start the pins on the other side of the IC into their respective holes in the same manner. When all of the pins have been started, set the IC into place by gently rocking it back and forth until it rests as close as possible to the board. Make sure that the IC is perfectly straight and as close to the board as possible; then tape it in place with a piece of masking tape.

( ) Turn the board over and solder each pin of the IC to the foil pattern on the back side of the board. Be sure to solder each pin and be careful not to leave any solder bridges.

( ) Turn the board over again and remove the piece of masking tape.

Use the same procedure to install each of the IC's. Be sure that you have the correct part number and the correct orientation as you install each one.

( ) IC's MC0 through MC7 are TMS 4030's or C2107A's



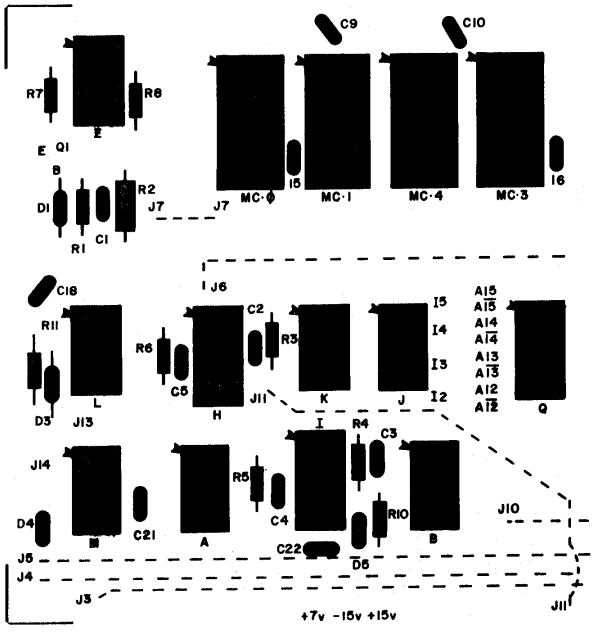
Address Hardwire Connections

There are four hardwire connections to be made on the 8800 4K RAM Board which set the starting address for the particular board being wired.

The address choosen for each memory board must be correlated with the rest of the system in which it is to be used. Refer to the MEMORY ADDRESS SELECTION section of your manual for the necessary information to determine these connections.

These four connections are to be made using the component leads saved from earlier in the assembly procedure. Bend the leads as necessary to fit the correct holes on the board, and insert them from the silk-screened side. Solder the leads to the foil pattern on the back side of the board; then clip off any excess lead lengths.

Be careful not to leave any solder bridges.



The board should be installed with the same orientation as the other boards in your 8800.

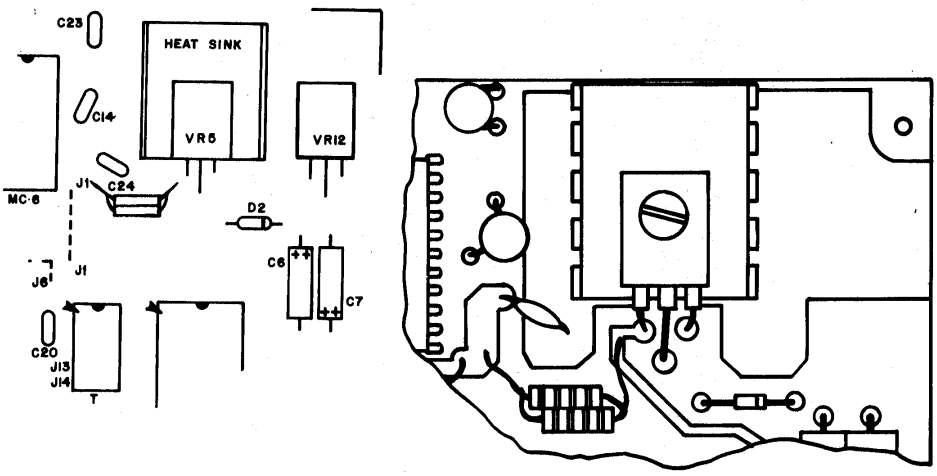
4K RAM BOARD POWER SUPPLY
**** MODIFICATION ****

THE FOLLOWING MODIFICATION MUST BE PERFORMED ON THE 5 VOLT SUPPLY REGULATION CIRCUITRY.

( ) Solder two 20-ohm resistors (red-black-black) together. Make the connection so that the two are as close as possible to each other. (see drawing below)

( ) Referring to the drawing, place a piece of electrical tape over the area on the board where the resistors will rest.

( ) Solder the resistors in place directly to the PC lands. One side will go to the 7805 lead closest to the IC labeled MC-6. The other side goes to the land connecting one side of C24 and the top pad for jumper J1. (see drawing and component layout below)



MEMORY ADDRESS SELECTION

There are several hardwire connections to be made on the 8800 memory boards for selecting the starting address for each board.

The starting address for each individual board is entirely optional within a few limitations. With only a single memory board in your system there is no problem, as long as the starting address selected in noted and taken into account when programming.

When more than one memory board is in the system, the sequence of starting addresses becomes critical. This is especially true when combining 1K and 4K boards in the same system. The important aspect in this case is to be sure that the individual blocks of memory on each board follow each other sequentially. There should be no gaps between the last address of one board and the starting address of the next.

The best example of this situation would be a system containing a 1K board with only 256 words of static memory together with a full 4K dynamic memory board. As may be noted from the "MEMORY ADDRESS SELECTION CHART", the starting address of the 1K boards may be selected with minimum increments of 1024 words. For the 4K board the minimum increment is 4096 words.

NOTE: Those addresses marked with an asterisk (*) in the chart are the possible address selections for the 4K boards, I1 & I0 being dropped for this board. Any address listed may be selected for the 1K boards.

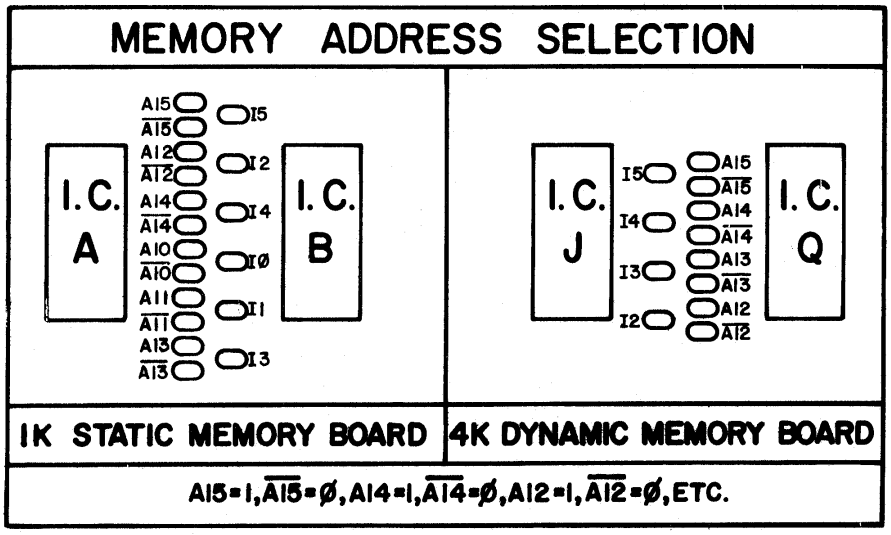
As may be seen from studying the chart, in the example above if the 1K board is placed at an address "before" the 4K board there will be a gap of 3840 words of memory between the boards. Even with the 1K board expanded to its full 1024 words, there would still be a gap of 3072 words of memory.

In this example the 4K board address must be placed "before" the 1K board address in order to keep all possible addresses sequential. (i.e.--place the 4K board at octal address 0 and the 1K board at octal address 10 000)

The same would hold true for two 1K boards, one fully expanded and the other with only 256 words of memory. The full board must be placed first and the second board must be placed so that it follows immediately in sequence.

The chart below illustrates the address selection pads for both the 1K and the 4K memory boards. The "I" prefixed pads correspond to the "I" prefixed headings on the "MEMORY ADDRESS SELECTION CHART". The "A" prefixed pads correspond to the 1's and 0's on the "MEMORY ADDRESS SELECTION CHART" as indicated at the bottom of the chart below. The last number of the pad should always correspond in each connection. (i.e.--pad I5 must go to either A15 or $\overline{A15}$, pad I1 must go to either A11 or $\overline{A11}$)

PROM MEMORY CARD (88-PMC) The 2K PROM Board uses exactly the same addressing format as the 1K and 4K memory boards. The only difference is that five jumpers are used (I1 through I5), and the memory increments in 2K blocks. All of the information in this section applies to the PROM board just as with the other memory boards. The possible addresses for the PROM board are marked " † " on the MEMORY ADDRESS SELECTION CHART.



MEMORY ADDRESS SELECTION CHART

ADDRESS LINES						ADDRESS SELECTED		
I5	I4	I3	I2	I1	I0	DECIMAL ADDRESS	OCTAL ADDRESS	
0	0	0	0	0	0	0	0	* †
0	0	0	0	0	1	1,024	2 000	
0	0	0	0	1	0	2,048	4 000	†
0	0	0	0	1	1	3,072	6 000	
0	0	0	1	0	0	4,096	10 000	* †
0	0	0	1	0	1	5,120	12 000	
0	0	0	1	1	0	6,144	14 000	†
0	0	0	1	1	1	7,168	16 000	
0	0	1	0	0	0	8,192	20 000	* †
0	0	1	0	0	1	9,216	22 000	
0	0	1	0	1	0	10,240	24 000	†
0	0	1	0	1	1	11,264	26 000	
0	0	1	1	0	0	12,288	30 000	* †
0	0	1	1	0	1	13,312	32 000	
0	0	1	1	1	0	14,336	34 000	†
0	0	1	1	1	1	15,360	36 000	
0	1	0	0	0	0	16,384	40 000	* †
0	1	0	0	0	1	17,408	42 000	
0	1	0	0	1	0	18,432	44 000	†
0	1	0	0	1	1	19,456	46 000	
0	1	0	1	0	0	20,480	50 000	* †
0	1	0	1	0	1	21,504	52 000	

ADDRESS LINES						ADDRESS SELECTED	
I5	I4	I3	I2	I1	I0	DECIMAL ADDRESS	OCTAL ADDRESS
0	1	0	1	1	0	22,528	54 000 †
0	1	0	1	1	1	23,552	56 000
0	1	1	0	0	0	24,576	60 000 * †
0	1	1	0	0	1	25,600	62 000
0	1	1	0	1	0	26,624	64 000 †
0	1	1	0	1	1	27,648	66 000
0	1	1	1	0	0	28,672	70 000 * †
0	1	1	1	0	1	29,696	72 000
0	1	1	1	1	0	30,720	74 000 †
0	1	1	1	1	1	31,744	76 000
1	0	0	0	0	0	32,768	100 000 * †
1	0	0	0	0	1	33,792	102 000
1	0	0	0	1	0	34,816	104 000 †
1	0	0	0	1	1	35,840	106 000
1	0	0	1	0	0	36,864	110 000 * †
1	0	0	1	0	1	37,888	112 000
1	0	0	1	1	0	38,912	114 000 †
1	0	0	1	1	1	39,936	116 000
1	0	1	0	0	0	40,960	120 000 * †
1	0	1	0	0	1	41,984	122 000
1	0	1	0	1	0	43,008	124 000 †
1	0	1	0	1	1	44,032	126 000
1	0	1	1	0	0	45,056	130 000 * †
1	0	1	1	0	1	46,080	132 000

ADDRESS LINES						ADDRESS SELECTED		
I5	I4	I3	I2	I1	I0	DECIMAL ADDRESS	OCTAL ADDRESS	
1	0	1	1	1	0	47,104	134 000	†
1	0	1	1	1	1	48,128	136 000	
1	1	0	0	0	0	49,152	140 000	* †
1	1	0	0	0	1	50,176	142 000	
1	1	0	0	1	0	51,200	144 000	†
1	1	0	0	1	1	52,224	146 000	
1	1	0	1	0	0	53,248	150 000	* †
1	1	0	1	0	1	54,272	152 000	
1	1	0	1	1	0	55,296	154 000	†
1	1	0	1	1	1	56,320	156 000	
1	1	1	0	0	0	57,344	160 000	* †
1	1	1	0	0	1	58,368	162 000	
1	1	1	0	1	0	59,392	164 000	†
1	1	1	0	1	1	60,416	166 000	
1	1	1	1	0	0	61,440	170 000	* †
1	1	1	1	0	1	62,464	172 000	
1	1	1	1	1	0	63,488	174 000	†
1	1	1	1	1	1	64,512	176 000	
Highest Directly Addressable Memory Location ⟶						65,535	177 777	

*4K Dynamic Memory Board Selections

† PROM MEMORY CARD SELECTIONS

MOS LSI

TMS 4060 JL, NL; TMS 4060-1 JL, NL; TMS 4060-2 JL, NL
4096-BIT DYNAMIC RANDOM-ACCESS MEMORIES

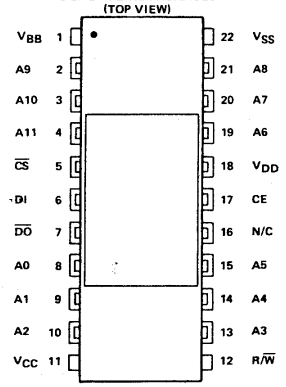
BULLETIN NO. DL-S 7512241, FEBRUARY 1975

- 4096 x 1 Organization
- 3 Performance Ranges:

	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY WRITE CYCLE (MIN)
TMS 4060	300 ns	470 ns	710 ns
TMS 4060-1	250 ns	430 ns	640 ns
TMS 4060-2	200 ns	400 ns	580 ns

- Full TTL Compatibility on All Inputs (No Pull-up Resistors Needed)
- Low Power Dissipation
  - 400 mW Operating (Typical)
  - 0.2 mW Standby (Typical)
- Single Low-Capacitance Clock
- N-Channel Silicon-Gate Technology
- 22-Pin 400-Mil Dual-in-Line Package

22-PIN CERAMIC AND PLASTIC DUAL-IN-LINE PACKAGES
(TOP VIEW)



3

description

The TMS 4060 series is composed of high-speed dynamic 4096-bit MOS random-access memories, organized as 4096 one-bit words. N-channel silicon-gate technology is employed to optimize the speed/power/density trade-off. Three performance options are offered: 300 ns access for the TMS 4060, 250 ns access for the TMS 4060-1, and 200 ns for TMS 4060-2. These options allow the system designer to more closely match the memory performance to the capability of the arithmetic processor.

All inputs except the chip enable are fully TTL-compatible and require no pull-up resistors. The low capacitance of the address and control inputs precludes the need for specialized drivers. When driven by a Series 74 device, the guaranteed dc input noise immunity is 200 mV. The TTL-compatible buffer is guaranteed to drive two Series 74 TTL gates. The TMS 4060 series uses only one clock (chip enable) to simplify system design. The low-capacitance chip-enable input requires a positive voltage swing (12 volts), which can be driven by a variety of widely available drivers.

The typical power dissipation of these RAM's is 400 mW active and 0.3 mW standby. To retain data only 6 mW average power is required, which includes the power consumed to refresh the contents of the memory.

The TMS 4060 series is offered in both 22-pin ceramic (JL suffix) and plastic (NL suffix) dual-in-line packages. The series is guaranteed for operation from 0°C to 70°C. These packages are designed for insertion in mounting-hole rows on 0.400-mil centers.

operation

chip select ($\overline{CS}$)

The chip-select terminal, which can be driven from standard TTL circuits without an external pull-up resistor, affects the data-in, data-out and read/write inputs. The data input and data output terminals are enabled when chip select is low. Therefore, the read, write, and read, modify write operations are performed only when chip select is low. If the chip is to be selected for a given cycle, the chip-select input must be low on or before the rising edge of the chip enable. If the chip is not to be selected for a given cycle, chip select must be held high as long as chip enable is high. A register for the chip-select input is provided on the chip to reduce overhead and simplify system design.

chip enable (CE)

A single external clock input is required. All read, write, and read, modify write operations take place when the chip enable input is high. When the chip enable is low, the memory is in the low-power standby mode. No read/write operations can take place because the chip is automatically precharging.

operation (continued)

mode select (R/$\overline{W}$)

The read or write mode is selected through the read/write (R/$\overline{W}$) input. A logic high on the R/$\overline{W}$ input selects the read mode and a logic low selects the write mode. The read/write terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected.

address (A0–A11)

All addresses must be stable on or before the rising edge of the chip-enable pulse. All address inputs can be driven from standard TTL circuits without pull-up resistors. Address registers are provided on chip to reduce overhead and simplify system design.

data-in (DI)

Data is written during a write or read, modify write cycle while the chip enable is high. The data-in terminal can be driven from standard TTL circuits without a pull-up resistor. There is no register on the data-in terminal.

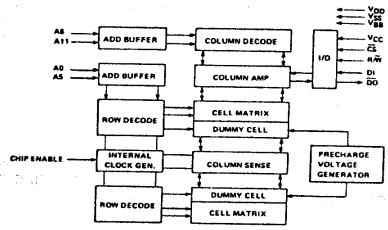
data-out ($\overline{DO}$)

The three-state output buffer provides direct TTL compatibility with a fan-out of two Series 74 TTL gates. The output is in the high-impedance (floating) state when the chip enable is low. It remains in the high-impedance state if the chip-select input is high when chip enable goes high and provided that chip select remains high as long as chip enable is high. If the chip select is set up low prior to the rise of chip enable and held low an interval after that rise, the output will be enabled as long as chip enable stays high regardless of subsequent changes in the level of chip select. A data-valid mode is always preceded by a low output state. Data-out is inverted from data-in.

refresh

Refresh must be performed every two milliseconds by cycling through the 64 addresses of the lower-order-address inputs, A0 through A5 (pins 8, 9, 10, 13, 14, 15), or by addressing every row within any 2-millisecond period. Addressing any row refreshes all 64 bits in that row. The chip does not need to be selected during the refresh. If the chip is refreshed during a write mode, then chip select must be high. The column addresses (A6 through A11) can be indeterminate during refresh.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note)	−0.3 to 20 V
Supply voltage, V_{DD} (see Note)	−0.3 to 20 V
Supply voltage, V_{SS} (see Note)	−0.3 to 20 V
All input voltages (see Note)	−0.3 to 20 V
Chip-enable voltage (see Note)	−0.3 to 20 V
Output voltage (operating, with respect to V_{SS})	−2 to 7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 150°C

NOTE: Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to V_{SS}.

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recommended operating conditions (see Note)

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
Supply voltage, V_{BB}	−4.5	−5	−5.5	V
High-level input voltage, V_{IH} (all inputs except chip enable)	2.2		5.25	V
High-level chip enable input voltage, $V_{IH(CE)}$	V_{DD} −0.6		V_{DD} +1.0	V
Low-level input voltage, V_{IL} (all inputs except chip enable) (see Note)	−0.6		0.6	V
Low-level chip enable input voltage, $V_{IL(CE)}$ (see Note)	−1		0.6	V
Refresh time, $t_{refresh}$			2	ms
Operating free-air temperature, T_A	0		70	°C

NOTE: The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_O = −2 mA		2.4		V_{CC}	V
V_{OL}	Low-level output voltage	I_O = 3.2 mA		V_{SS}		0.4	V
I_I	Input current (all inputs except chip enable)	V_I = 0 to 5.25 V				10	μA
$I_{I(CE)}$	Chip enable input current	V_I = 0 to 13.2 V				2	μA
I_{OZ}	High-impedance-state (off-state) output current	V_O = 0 to 5.25 V				10	μA
I_{CC}	Supply current from V_{CC}	2 Series 74 TTL loads				1	mA
I_{DD}	Supply current from V_{DD}	$V_{IH(CE)}$ = 12.6 V			30	60	mA
I_{DD}	Supply current from V_{DD}, standby	$V_{IL(CE)}$ = 0.6 V			20	200	μA
$I_{DD(av)}$	Average supply current from V_{DD} during read or write cycle	Minimum cycle time	TMS 4060		32		mA
			TMS 4060-1		35		
			TMS 4060-2		38		
$I_{DD(av)}$	Average supply current from V_{DD} during read, modify write cycle		TMS 4060		32		mA
			TMS 4060-1		35		
			TMS 4060-2		38		
I_{BB}	Supply current from V_{BB}	V_{BB} = −5.5 V, V_{DD} = 12.6 V,	V_{CC} = 5.25 V, V_{SS} = 0 V		−5	−100	μA

†All typical values are at T_A = 25°C.

capacitance at V_{DD} = 12 V, V_{SS} = 0 V, V_{BB} = −5 V, V_{CC} = 5 V, $V_{I(CE)}$ = 0 V, V_I = 0 V, f = 1 MHz, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$C_{i(ad)}$	Input capacitance address inputs			5	7	pF
$C_{i(CE)}$	Input capacitance clock input	$V_{I(CE)}$ = 10.8 V		18	22	pF
		$V_{I(CE)}$ = −1.0 V		23	27	
$C_{i(\overline{CS})}$	Input capacitance chip select input			4	6	pF
$C_{i(data)}$	Input capacitance data input			4	6	pF
$C_{i(R/\overline{W})}$	Input capacitance read/write input			5	7	pF
C_o	Output capacitance			5	7	pF

†All typical values are at T_A = 25°C.

read cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4060		TMS 4060-1		TMS 4060-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time	470		430		400		ns
$t_{w(CEH)}$	Pulse width, chip enable high	300	4000	260	4000	230	4000	ns
$t_{w(CEL)}$	Pulse width, chip enable low	130		130		130		ns
$t_{r(CE)}$	Chip-enable rise time		40		40		40	ns
$t_{f(CE)}$	Chip-enable fall time		40		40		40	ns
$t_{su(ad)}$	Address setup time	0↑		0↑		0↑		ns
$t_{su(\overline{CS})}$	Chip-select setup time	0↑		0↑		0↑		ns
$t_{su(rd)}$	Read setup time	0↑		0↑		0↑		ns
$t_{h(ad)}$	Address hold time	150↑		150↑		150↑		ns
$t_{h(\overline{CS})}$	Chip-select hold time	150↑		150↑		150↑		ns
$t_{h(rd)}$	Read hold time	40↓		40↓		40↓		ns

↑↓ The arrow indicates the edge of the chip enable pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

3

read cycle switching characteristics over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4060		TMS 4060-1		TMS 4060-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(CE)}$	Access time from chip enable†		280		230		180	ns
$t_{a(ad)}$	Access time from address†		300		250		200	ns
t_{PHZ} or t_{PLZ}	Output disable time from high or low level‡	30		30		30		ns
t_{PZL}	Output enable time to low level‡		250		200		150	ns

†Test conditions: C_L = 50 pF, $t_{r(CE)}$ = 20 ns, Load = 1 Series 74 TTL gate.
‡Test conditions: C_L = 50 pF, Load = 1 Series 74 TTL gate.

write cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4060		TMS 4060-1		TMS 4060-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(wr)}$	Write cycle time	470		430		400		ns
$t_{w(CEH)}$	Pulse width, chip enable high	300	4000	260	4000	230	4000	ns
$t_{w(CEL)}$	Pulse width, chip enable low	130		130		130		ns
$t_{w(wr)}$	Write pulse width	200		190		180		ns
$t_{r(CE)}$	Chip-enable rise time		40		40		40	ns
$t_{f(CE)}$	Chip-enable fall time		40		40		40	ns
$t_{su(ad)}$	Address setup time	0↑		0↑		0↑		ns
$t_{su(\overline{CS})}$	Chip-select setup time	0↑		0↑		0↑		ns
$t_{su(da\text{-}wr)}$	Data-to-write setup time*	0		0		0		ns
$t_{su(wr)}$	Write-pulse setup time	240↓		220↓		210↓		ns
$t_{h(ad)}$	Address hold time	150↑		150↑		150↑		ns
$t_{h(\overline{CS})}$	Chip-select hold time	150↑		150↑		150↑		ns
$t_{h(da)}$	Data hold time	40↓		40↓		40↓		ns

↑↓ The arrow indicates the edge of the chip enable pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.
*If $R/\overline{W}$ is low before CE goes high then DI must be valid when CE goes high.

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read cycle timing

CHIP ENABL

ADDRESS, A

CHIP SELEC

READ/WRIT

DATA OUT

NOTE: For the chip-enabl
2.2 V (high). Out

write cycle timing

CHIP ENA

ADDRES

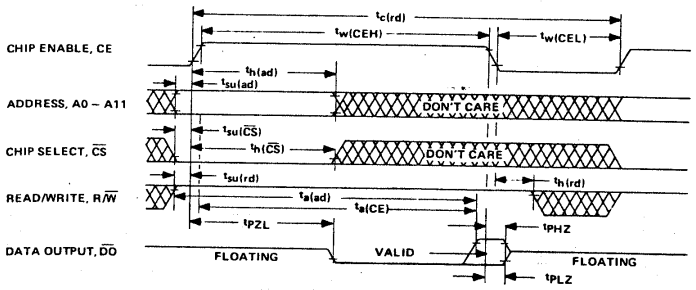
CHIP SEL

READ/W

DATA IN

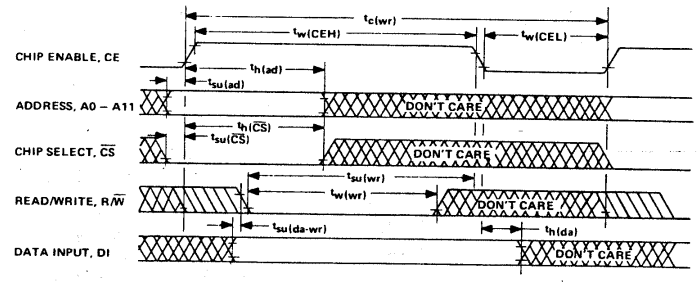
NOTE: For the chip-enab
2.2 V (high). Out
mitted to change

read cycle timing



NOTE: For the chip-enable input, high and low timing points are 90% and 10% of $V_{IH(CE)}$. Other input timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high).

write cycle timing



NOTE: For the chip-enable input, high and low timing points are 90% and 10% of $V_{IH(CE)}$. Other input timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high). During the time from the rise of CE to the fall of R/$\overline{W}$, R/$\overline{W}$ is permitted to change from high to low only.

read, modify write cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4060		TMS 4060-1		TMS 4060-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(RMW)}$	Read, modify write cycle time*	710		640		580		ns
$t_{w(CEH)}$	Pulse width, chip enable high*	540	4000	470	4000	410	4000	ns
$t_{w(CEL)}$	Pulse width, chip enable low	130		130		130		ns
$t_{w(wr)}$	Write-pulse width	200		190		180		ns
$t_{r(CE)}$	Chip-enable rise time		40		40		40	ns
$t_{f(CE)}$	Chip-enable fall time		40		40		40	ns
$t_{su(ad)}$	Address setup time	0↑		0↑		0↑		ns
$t_{su(\overline{CS})}$	Chip-select setup time	0↑		0↑		0↑		ns
$t_{su(da\text{-}wr)}$	Data-to-write setup time	0		0		0		ns
$t_{su(rd)}$	Read pulse setup time	0↑		0↑		0↑		ns
$t_{su(wr)}$	Write pulse setup time	240↓		220↓		210↓		ns
$t_{h(ad)}$	Address hold time	150↑		150↑		150↑		ns
$t_{h(\overline{CS})}$	Chip-select hold time	150↑		150↑		150↑		ns
$t_{h(rd)}$	Read hold time	280↑		230↑		180↑		ns
$t_{h(da)}$	Data hold time	40↓		40↓		40↓		ns

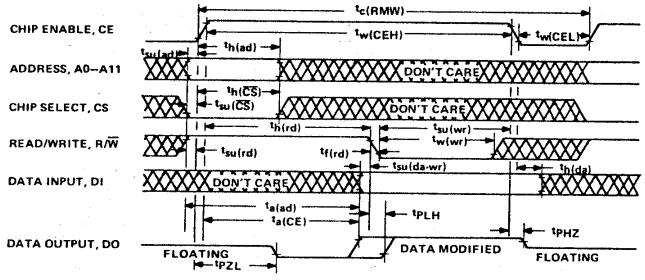
↑↓ The arrow indicates the edge of the chip-enable pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.
*Test conditions: $t_{f(rd)}$ = 20 ns.

read, modify write cycle switching characteristics over recommended supply voltage range, T_A = 0°C to 70°C

PARAMETER		TMS 4060		TMS 4060-1		TMS 4060-2		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(CE)}$	Access time from chip enable†		280		230		180	ns
$t_{a(ad)}$	Access time from address†		300		250		200	ns
t_{PLH}	Propagation delay time, low-to-high level output from write pulse‡	30		30		30		ns
t_{PHZ}	Output disable time from high level‡	30		30		30		ns
t_{PZL}	Output enable time to low level‡		250		200		150	ns

†Test conditions: C_L = 50 pF, $t_{r(CE)}$ = 20 ns, Load = 1 Series 74 TTL gate.
‡Test conditions: C_L = 50 pF, Load = 1 Series 74 TTL gate.

read, modify write cycle timing

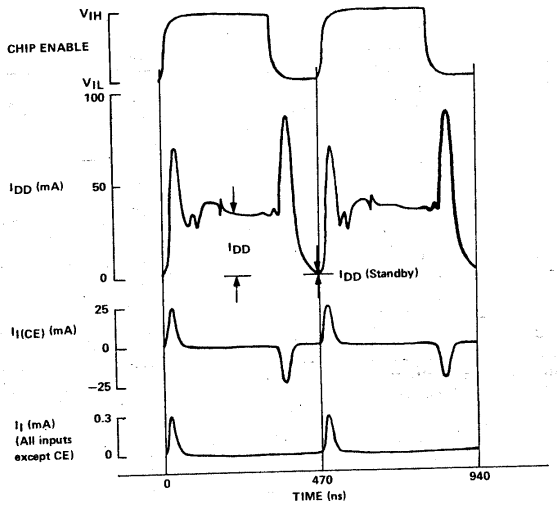


NOTE: For the chip enable input, high and low timing points are 90% and 10% of $V_{IH(CE)}$. Other input timing points are 0.6 V (low) and 2.2 V (high). Output timing points are 0.4 V (low) and 2.4 V (high).

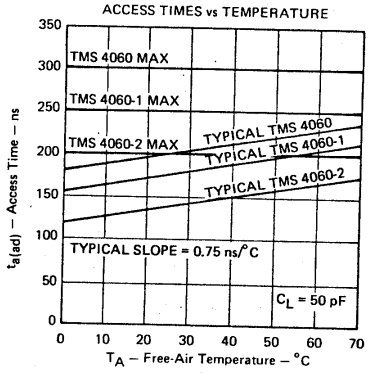
timing diagram conventions

TIMING DIAGRAM SYMBOL	MEANING: INPUT FORCING FUNCTIONS	MEANING: OUTPUT RESPONSE FUNCTIONS
	Must be steady high or low	Will be steady high or low
	High-to-low changes permitted	Will be changing from high to low sometime during designated interval
	Low-to-high changes permitted	Will be changing from low to high sometime during designated interval
	Don't care	State unknown or changing
	(Does not apply)	Center line is high-impedance off-state

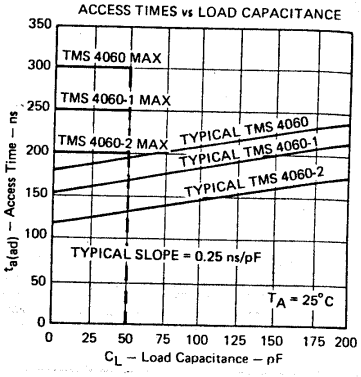
TYPICAL WAVEFORMS



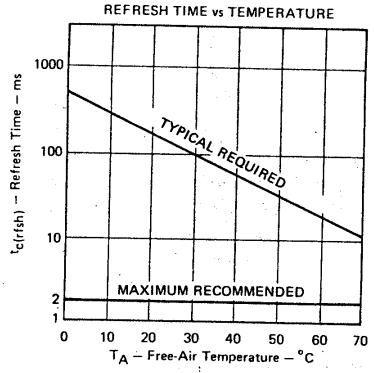
ACCESS TIMES vs TEMPERATURE



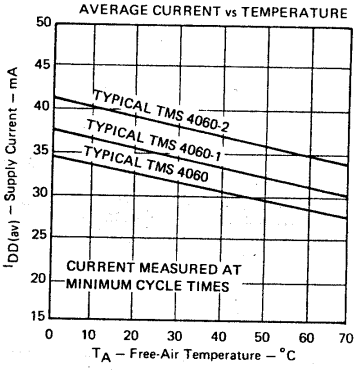
ACCESS TIMES vs LOAD CAPACITANCE



REFRESH TIME vs TEMPERATURE



AVERAGE CURRENT vs TEMPERATURE



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