88-4PIO

1 PORT

PARTS LIST

BAG 1

1	6820	101097
1	74L00	101080
1	74L02	101072
4	74L04	101073
1	74L20	101039
1	7473	101027
1	7805	101074
3	8T97	101040

BAG 2

1	100 Pin Conn	101864
2	Card Guides	101714
1	40 Pin Sockets	102106
1	24 Pin Sockets	102105
1	Flat Cable Assy	103036
1	25DBP Connector	102111
1	Connector Cover	101739
5	2½" Wire (yellow)	103001

BAG 3

1	1K½w 5%	101928
1	33uf 16V	100326
13	.luf 10V	100348

BAG 4

1	#6 x ½" Screw	100918
2	#4 x 3/8"Screw	100908
1	#6 - 32 Nut	100933
2	#4 - 40 Nut	100932
1	#6 Lock Washer	100942
2	#4 Lock Washer	100941
1	Heat Sink (Large)	101870
4	#6-32 x 3/8"	100925

MISC:

1	4PIO PC Board	100184
1	4PIO Manual	101522

88-4 PARALLEL INPUT/OUTPUT BOARD OPERATION

The 88-4PIO board is based on a peripheral interface integrated circuit, the 6820. The chip contains all control and data registers, thus most 88-4PIO options are software selectable. These options include data direction (each data line can act as input or output) and interrupt/control structure modification. The 88-4PIO board can be expanded to four "PORTS" (four 6820 ICs), making it one of the most powerful and versatile interface boards available.

BACKGROUND THEORY

NOTE: See block diagram on page 3.

The ALTAIR 8800 allows for up to 256 addresses reserved for Input/Output devices. The "IN" and "OUT" instructions to the central processing unit (CPU) distinguish I/O addresses from memory addresses, thus enabling the CPU to maintain full memory capability during I/O operations.

"IN" and "OUT" instructions work as follows: Each instruction contains two bytes and requires three machine cycles to execute. During machine cycles 1 and 2 (M1, M2), bytes 1 and 2 of the instruction are fetched from memory by the CPU. Byte 1 is the instruction code ("IN" = 333, "OUT" = 323), and byte 2 is the device address (0-377).

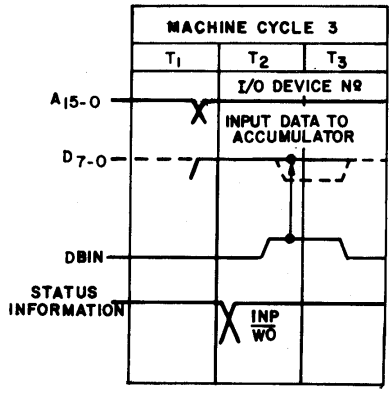
During machine cycle 3 (M3), data is transferred as follows: During the first clock period (T1) of M3, the I/O device address (byte 2 of the instruction) is placed on the "address" buss. Only 8 bits are used for I/O device addresses so that the address appears on both the lower lines (A0-A7) and the upper lines (A8-A15). The status signals of T2 distinguish device address operations from memory operations. During T2, the status information is latched and sent to the system buss. The status signal for the "IN" instruction is "SINP" and the status signal for the "OUT" instruction is "SOUT". Except for the I/O status signal, T3 of M3 appears identical to a memory operation.

Data is strobed into the accumulator with PDBIN for "IN" operations. The accumulator is placed on the data buss and strobed out with $\overline{\text{PWR}}$ for "OUT" operations. The device and interface are responsible for assuring that data is on the buss when the CPU requires it and that the device receives data during $\overline{\text{PWR}}$ in an "OUT" operation.

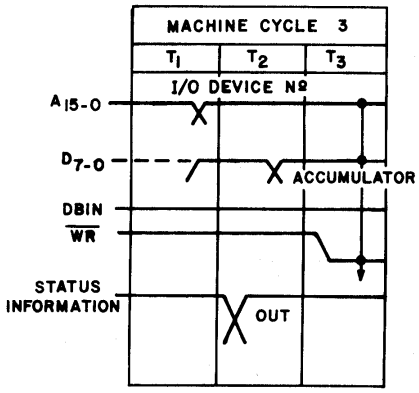
TIMING DIAGRAMS

88-4PIO BOARD

INPUT INSTRUCTION



OUTPUT INSTRUCTION



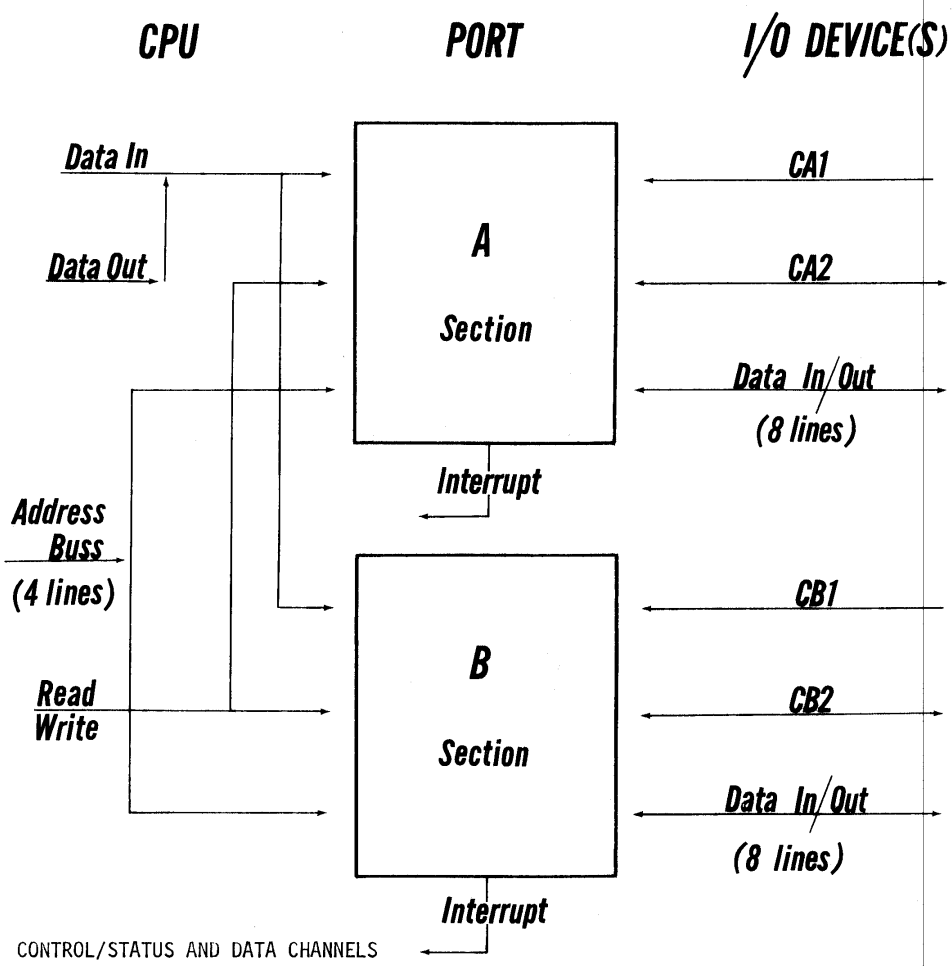
PORT SELECTION

Each 4-PIO board requires 16 addresses, four for each port. The four jumpers on the 88-4PIO board represent address lines A4-A7 and their complements $\overline{A4}$-$\overline{A7}$. The address lines cause one of a possible 16 4-PIO boards to be selected. Page 13 of the 88-4PIO assembly procedure shows how to connect the jumpers for a particular group of addresses.

Address lines A2 and A3 enable selection of one of the four ports. Each port contains two sections, A and B. Sections A and B each contain two channels, control/status channel and data channel. Address lines A0 and A1 enable the selection of port section, A or B, and the selection of control/status channel or data channel. If the address selection jumpers are wired for 000-017, the port, section and channel addresses would appear as follows:

ADD		PORT	IC LETTER	SECTION	CHANNEL
Octal	Decimal				
0	0	0	J	A	C
1	1				D
2	2			B	C
3	3				D
4	4	1	K	A	C
5	5				D
6	6			B	C
7	7				D
10	8	2	L	A	C
11	9				D
12	10			B	C
13	11				D
14	12	3	M	A	C
15	13				D
16	14			B	C
17	15				D
					C=Control D=Data

The simplified block diagram on the following page illustrates the address-register operation of the 88-4PIO.



CONTROL/STATUS AND DATA CHANNELS

Each port section, A and B, contains three registers, eight data lines, two control lines and an interrupt request output. The control/status register, designed as follows, is a read/write register, meaning that it can be input from and output to.

Bit #	7	6	5	4	3	2	1	0
Function	Interrupt Request		C2 Control			DDR Control	C1 Control	

Bit 7 and 6 are unaffected during write. Bit 7 is an interrupt status bit which relates the activity of the external control line, C1. C1 is an input control line from the I/O device. C1 affects status bit 7 and the interrupt request output to the system buss, $\overline{IRQ}$. Control bits 1 and 0 define the operation of C1 as follows:

CONTROL BITS 1	0	C1 INPUT	STATUS BIT 7	$\overline{IRQ}$ OUTPUT
0	1	Active low	Set high when C1 is active	Disabled -- remains high
0	1	Active low	Set high when C1 is active	Goes low when bit 7 goes high
1	0	Active high	Set high when C1 is active	Disabled -- remains high
1	1	Active high	Set high when C1 is active	Goes low when bit 7 goes high

Bit 7 and $\overline{IRQ}$ are reset (bit 7 goes low, $\overline{IRQ}$ goes high) when the data register is read by the CPU.

The C2 control line can function as either input or output for the I/O device. The mode of operation for C2 is determined by control bits 5, 4 and 3 as shown by the following table. This table shows C2 functioning as input (control bit 5 low):

CONTROL BITS 5	4	3	C2	STATUS BIT 6	$\overline{IRQ}$
0	0	0	Active low	Set high when C2 is active	Disabled -- remains high
0	0	1	Active low	Set high when C2 is active	Goes low when bit 7 is high
0	1	0	Active high	Set high when C2 is active	Disabled -- remains high
0	1	1	Active high	Set high when C2 is active	Goes low when bit 7 is high

Sections A and B operate identically when C2 functions as input. As output, however, C2 functions uniquely for sections A and B. C2 (noted as CA2) functions as output in Section A as follows (control bit 5 high):

A SECTION CONTROL BITS			CA2	
5	4	3	CLEARED	SET
1	0	0	Low after E pulse, following read of A data channel	High when CA1 is active
1	0	1	Low after a read of A data channel	High following next E pulse
1	1	0	Always low when bit 3 is low	
1	1	1		Always high when bit 3 is high

NOTE: The E pulse is a strobe pulse into the port that occurs during every machine cycle and partially enables the port to read or write.

C2 (noted as CB2) functions as output in Section B as follows (control bit 5 high):

B SECTION CONTROL BITS			CB2	
5	4	3	CLEARED	SET
1	0	0	Low when E pulse goes high, following a write of B data channel	High when CB1 is active
1	0	1	Low when E pulse goes high, following a write of B data channel	High when next E pulse goes high
1	1	0	Always low when bit 3 is low	
1	1	1		Always high when bit 3 is high

To write into a control register, set each accumulator bit according to the preceding chart; execute an "OUT" instruction, with Byte 2 of the instruction equal to the control channel address. Also, data lines must be entered as input or output. All ports are reset when power is first applied, thereby resetting the data lines and the C2 line for both sections as inputs.

Data channel address permits access to either the data register or the data direction register (DDR). The status of bit 2 in the control register determines whether data register or DDR is accessed. If bit 2 is logic 0, DDR is accessed. If bit 2 is logic 1, data register is accessed. Writing logic 0 into a bit of the DDR causes the corresponding data line to act as an input; writing logic 1 into a bit of the DDR causes the corresponding data line to act as an output.

The machine language routine on the next page illustrates the initialization procedure for a port which interfaces a parallel input/output device. The 88-4PIO board is addressed at locations 20-37 octal or 16-31 decimal. In this example, Port 0 and addresses 20-23 are used. The addresses function as follows: 20, A control; 21, A data; 22, B control; and 23, B data. The A section of the port functions as input and B section, as output.

LOCATION	INSTRUCTION	CODE	DESCRIPTION
0	MVIA	076	Set bit 2 of both control registers to "0" in order to write to the DDRs.
1	<B2>	000	
2	OUT	323	
3	<B2>	020	
4	OUT	323	
5	<B2>	022	
6	OUT	323	Write all "0"s to DDR of A Section to enable A data lines to act as inputs
7	<B2>	021	
10	MVIA	076	Write "1"s into DDR of B Section to enable B data lines to act as outputs
11	<B2>	377	
12	OUT	323	
13	<B2>	023	
14	MVI	076	Set A control register:*
15	<B2>	045	
16	OUT	323	
17	<B2>	020	Set B control register:*
20	MVI	076	
21	<B2>	054	
22	OUT	323	
23	<B2>	022	

7	6	5	4	3	2	1	0
		1	0	0	1	0	1

7	6	5	4	3	2	1	0
		1	0	1	1	0	0

* See description of C1 and C2 for above settings.

This initialization procedure causes the following communication between the I/O device and the CPU.

INPUT

1. If the I/O device has valid data, a strobe signal from the I/O device pulls input CA1 low; bit 7 of the A control register goes high; $\overline{IRQA}$ goes low; and CA2 goes high. CA2 operates as a "busy" signal back to the I/O device.

2. If interrupts are used, an interrupt is generated and Step 3 is entered. If interrupt is not used, the CPU periodically inputs the A control register in order to interpret the status of bit 7. When bit 7 is high, Step 3 will be entered. Refer to page 12 for further explanation of the 88-4PIO board interrupt capabilities.

3. Data is input to the accumulator which, in turn, resets bit 7, $\overline{IRQA}$ and CA2. The transition of CA2 tells the I/O device that new data may be entered.

OUTPUT

1. CB1 is pulled low by the I/O device when it is ready to receive new data.

2. If interrupts are implemented, an interrupt is generated and Step 3 is entered. If interrupt is not used, the CPU periodically inputs the B control register in order to interpret the status of bit 7. When bit 7 is high, Step 3 will be entered.

3. Data is output to the I/O device and thereby latched into the port outputs. CB2 goes low when the next E pulse goes high. CB2 returns to a high position when E pulse (enable) goes high again. CB2 can be used to strobe data into the I/O device. CB2 pulse width is, approximately, 1.5 microseconds - 3.5 microseconds, depending on the instructions executed.

88-4PIO BOARD ELECTRICAL THEORY

Address lines A7-A4 are inverted/buffered through IC D and fed to pads $\overline{A7}$-$\overline{A4}$ and E pins 2, 4, 6 and 8 are the complements of $\overline{A7}$-$\overline{A4}$. If the incoming address matches selected address (jumpers 7-4), N pin 6 goes low and F pin 6 and G pin 1 go high. If an "IN" or "OUT" instruction is executed, either SINP or SOUT forces G pin 3 and $\overline{CS2}$ low, thereby partially selecting the ports (ICs J, K, L and M). Address lines A3 and A2 complete selection of one of the four ports via inputs CS0 and CS1 (high active) according to the following chart:

A3	A2	PORT (IC)
0	0	J
0	1	K
1	0	L
1	1	M

Address lines A1 and A0 select the port section and a register within that section via inputs RS0 and RS1 according to the chart below:

A1	A0	SECTION	REGISTER
0	0	A	Control
0	1	A	Data
1	0	B	Control
1	1	B	Data

The incoming 8-bit address, therefore, selects a 4-PIO board, a port, a section and a register. To read or write a register, E pulse (enable) must be present. PDBIN and $\overline{\text{PWR}}$ are ored together to generate one E pulse/machine cycle. The E pulse ensures that data is read and written at the correct time.

F pin 6 enables G pins 9 and 12. The instruction "OUT" causes two operations: 1) SOUT forces G pin 13 high and G pin 11 low, enabling data to enter the port (A pin 1 and B pin 1); 2) SOUT pulls R/W (read/write) low to cause a write. Note that ICs A, B, and C are tri-state drivers and are enabled by pins 1 and 15 (for illustration see 8T97 layout of CPU schematic). The ports use a bidirectional data buss to communicate with the CPU.

The instruction "IN" causes the following operations: 1) SINP forces G pin 8 low, enabling the port data drivers (A15, B15 and C1) and clocks flip-flop IC0; 2) IC0 pin 13 goes low, enabling C pin 13 to pull PRDY low; 3) at this point, the CPU rests in a "wait state" until PWAIT goes high, thereby clearing the flip-flop. The wait state lasts for 500 nanoseconds and is generated in order to allow address set-up time for the ports. The wait state occurs only during an input operation.

$\overline{\text{POC}}$ (power on clear) is ored to PWAIT. This connection ensures that IC0 is initially reset. The connection also ensures that the IC0 is gated to RST input which is, in turn, gated to the ports. This resets the internal registers of the ports when power is applied.

The data and control lines to the external world are all TTL compatible, requiring one TTL load as input and driving one TTL load as output. One TTL load is defined as 1.6 ma at .8 volts, maximum, for a logic low and 40 microamps at 2.0 volts, minimum (up to 5.5 volts, max.), for a logic high. The B section data and control lines, when used as outputs, will also drive at least 1 milliamp at 1.5 volts to directly drive the base of switching transistors.

The 88-4PIO board uses a single +5 volt supply derived from the unregulated voltage in VR1, a +5 volt regulator.

INTERRUPT

Communication between the I/O device and the CPU may be handled with software. The CPU's user program periodically tests the status of the I/O device, and when a ready bit is detected, the I/O device is serviced.

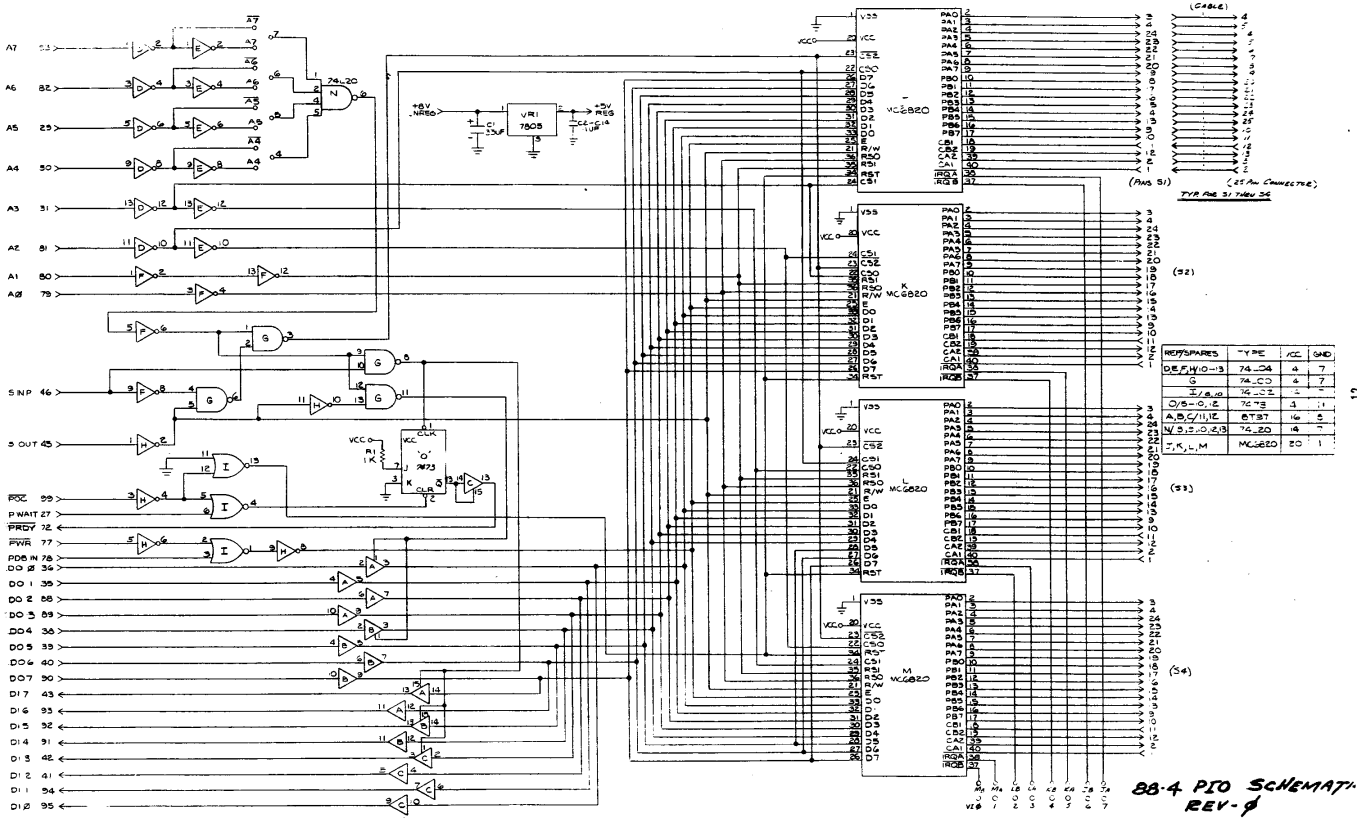
However, in some applications, the CPU may have a tremendous amount of work to do in a relatively short period of time. In this kind of environment, it is most efficient for the I/O device itself to signal the CPU when it is ready to be serviced.

Communication from the I/O device to the CPU may be accomplished via one of two optional methods. The 88-VI board, which provides eight levels of vectored interrupt, may be implemented. The optional 88-VI board is practical if several I/O devices of different priority need to be serviced under interrupt control.

The second interrupt option provides a single level of interrupt and is enabled by the 88-4PIO board itself. To enable single level interrupt, jumper the particular port interrupt request line(s) (JA, JB, KA, KB, etc.) to the pad marked $\overline{\text{PINT}}$, located at the bottom of the 88-4PIO board. Note, any number of interrupt request lines on the 88-4PIO board can be jumpered to $\overline{\text{PINT}}$.

The CPU's user program enables interrupt within the port and within the CPU via the Enable Interrupt (EI) instruction. The user program also allocates space in memory for the stack.

During interrupt, the interrupt request line goes low, thereby 1) causing the CPU to finish execution of its current instruction, 2) pushing the program counter onto the stack, and 3) jumping to location 70 (octal). The I/O device service routine must begin at location 70. The return instruction (RET) may be used to return the CPU to its main program after interrupt is complete.



88-4 PIO SCHEMATIC REV-Ø

4PIO

88-4PIO BOARD

Assembly Procedure

88-4 PARALLEL I/O BOARD ASSEMBLY

SOCKET INSTALLATION

The 88-4 Parallel Input/Output board (88-4PIO) may be configured for 1, 2, 3 or 4 I/O ports. Each port requires one 40-pin IC socket and one 24-pin connector cable socket.

The 40-pin IC sockets will be placed in positions J, K, L, M, and the 24-pin connector cable sockets will be placed in positions S1-S4, as noted by the component layout on page 5. The 40-pin IC sockets and the 24-pin connector cable sockets must be placed in positions parallel to each other. Depending upon the configuration of your board, install the sockets in the positions indicated below.

	40-pin	24-pin
1 port	J	S1
2 ports	J, K	S1, S2
3 ports	J, K, L	S1, S2, S3
4 ports	J, K, L, M	S1, S2, S3, S4

Referring to the parts chart on page 4, the component layout on page 5, and the illustration on this page, use the following procedure to install each socket.

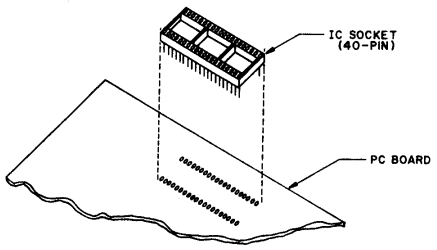
1. Be certain that the socket pins are straight. If any of the pins are bent, CAREFULLY straighten them with the tip of a small screwdriver.

2. Set the socket into place and secure it with a piece of masking tape.

3. Turn the board over and solder each pin to the foil pattern of the back of the board. Be sure that EACH pin is soldered, and be careful not to leave any solder bridges.

4. Turn the board over again, and remove the masking tape.

5. After each socket is installed, check the corresponding socket off of the parts list on page 4.



IC INSTALLATION

There are 15 integrated circuits to be installed on the 88-4PIO board. From one to four of the ICs have been provided with sockets (J, K, L, M) and must not be installed at this time. The remaining ICs (A, B, C, D, E, F, G, H, I, O, N) are to be soldered directly to the board.

NOTE: The four ICs provided with sockets are extremely static-sensitive. Do not install these ICs (J, K, L, M) until after the entire board is assembled. Before installation, be certain to refer to the "MOS IC Special Handling Procedures" (page 5 of the ALTAIR 8800 Assembly Manual.) Failure to carefully follow the instructions of the "MOS IC Special Handling Procedures" may result in permanent damage to static-sensitive ICs.

To prepare ICs for installation:

Referring to the component layout on page 5, remove the IC with the correct part number from its holder. If there are any bent pins, straighten them with a needle-nose pliers. Ensure that you choose the IC with the correct part number as you install each one.

All ICs are damaged easily and should be handled carefully. Always try to hold the IC by the ends, touching the pins as little as possible.

All ICs must be oriented so that the notched end is toward the end with the arrowhead printed on the 88-4PIO board. Pin 1 of the IC should correspond with the pad marked with the arrowhead. If the IC does not have a notch on one end, refer to the IC Orientation Chart included with your manual for the identification of Pin 1.

Install the ICs according to the following procedure:

1. After the IC is correctly oriented, start the pins on one side of the IC into their respective holes on the silk-screened side of the PC board. DO NOT PUSH THE PINS IN ALL THE WAY. If you have difficulty getting the pins into the holes, use the tip of a small screwdriver to guide them.

2. Start the pins on the other side of the IC into their holes in the same manner. When all of the pins have been started, set the IC into place by gently rocking it back and forth until it rests as closely as possible to the board. After you are certain that the IC is perfectly straight and as close to the board as possible, tape it in place with a piece of masking tape.

3. Turn the board over and solder each pin to the foil pattern on the back side of the board. Be sure to solder EACH pin, and be careful not to leave any solder bridges.

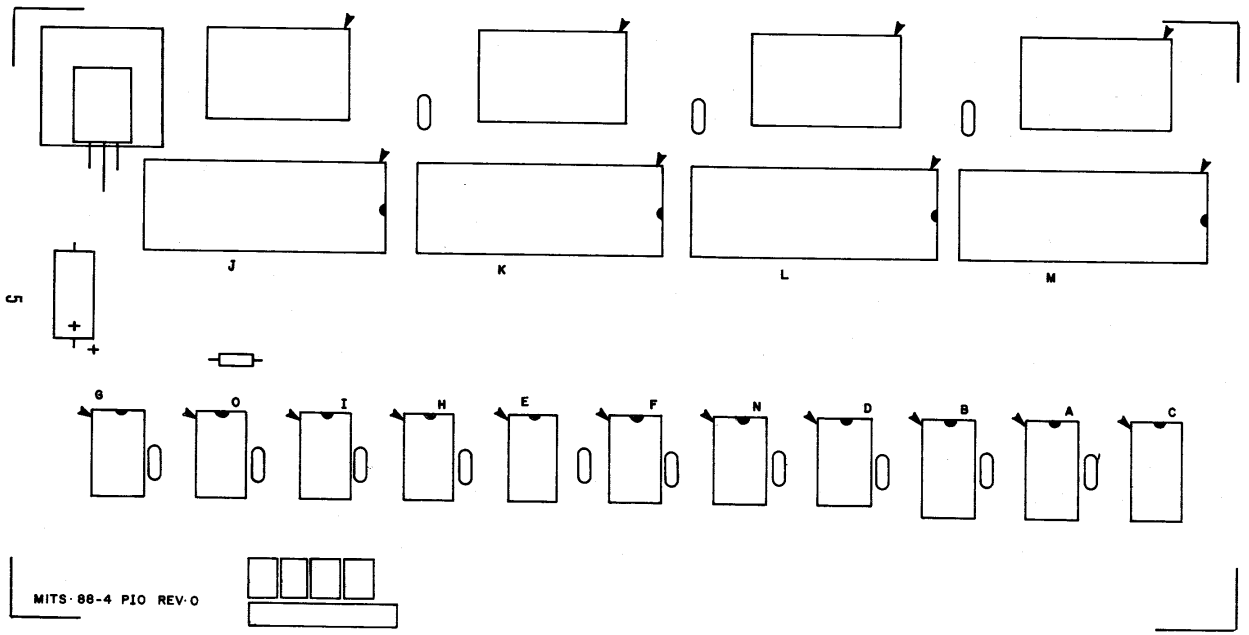
4. Turn the board over again, and remove the piece of masking tape.

5. After each IC is installed, check the corresponding IC off of the parts list provided on page 4.

ICS AND SOCKETS

Silk Screen Designation	Parts	Number
( ) A ( ) B ( ) C	ICs	8T97
( ) D ( ) E ( ) F ( ) H	ICs	74L04
( ) G	IC	74L00
( ) I	IC	74L02
( ) J ( ) K ( ) L ( ) M*	40-pin IC Sockets	
( ) N	IC	74L20
( ) O	IC	7473
( ) S1 ( ) S2 ( ) S3 ( ) S4**	24-pin Sockets	

* Parts K, L, M are optional.
** Parts S2, S3, S4 are optional.


J
K
L
M
G
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I
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E
F
N
D
B
A
C
MITS-88-4 PIO REV-0

RESISTOR AND CAPACITOR INSTALLATION

One resistor and 14 capacitors must be installed on the 88-4PIO board. The resistor is color-coded, brown-black-red-gold and is either 1/4 or 1/2 Watt. It is labeled R1 on the component layout (page 9). The capacitors are labeled C1-C14. C-1 is an electrolytic capacitor with a capacitance of 30 µf or greater. C2-C14 are ceramic disk capacitors with a capacitance of .1 µf or greater.

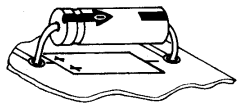
Refer to the component layout (page 9), and install the resistor according to the following procedure.

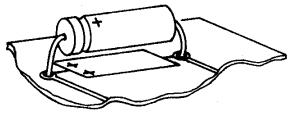
1. Using needle-nose pliers, bend the leads of the resistor at right angles to match their respective holes on the 88-4PIO board.
2. Insert the resistor into the correct holes from the silk-screened side of the board. Push the resistor down until it almost touches the foil pattern.
3. Holding the resistor in place, turn the board over and bend the leads slightly outward.
4. Solder the two leads to the foil pattern on the back side of the board; then clip off any excess lead lengths.
5. After making sure that there are no solder bridges, check the resistor off of the parts list provided on page 8.

There is one electrolytic capacitor to be installed on the 88-4PIO board. The polarity requirements of the electrolytic capacitor must be noted before it is installed.

The polarity markings of the electrolytic capacitor for the 88-4PIO board may appear as one of three types. Note the following illustrations.

ELECTROLYTIC CAPACITOR





If the marking is the arrow type, orient the capacitor so that the arrow points to the negative polarity side. If the marking is one of the other two types, orient the capacitor so that the positive signs match the positive polarity side. Polarity is designated on the silk screened side of the board.

Referring to the component layout on page 9, install the electrolytic capacitor (C-1) according to the following procedure:

1. Bend the two leads of the capacitor at right angles to match their respective holes on the board. Insert the capacitor into the holes on the silk-screened side of the board. Be sure to point the arrow of the capacitor in the opposite direction of the positive signs "+ +" printed on the board.

2. Holding the capacitor in place, turn the board over and bend the two leads slightly outward. Solder the two leads to the foil pattern, and clip off any excess lead lengths.

3. After making sure that there are no solder bridges, check the electrolytic capacitor (C-1) off of the parts list on page 8.

Use the following procedure to install each of the 14 ceramic disk capacitors (C2-C14).

1. Using needle-nose pliers, straighten the two leads as necessary to fit their respective holes on the 88-4PIO board.

2. Insert the capacitor into the correct holes from the silk-screened side of the board. Push the capacitor down until the ceramic insulation almost touches the foil pattern.

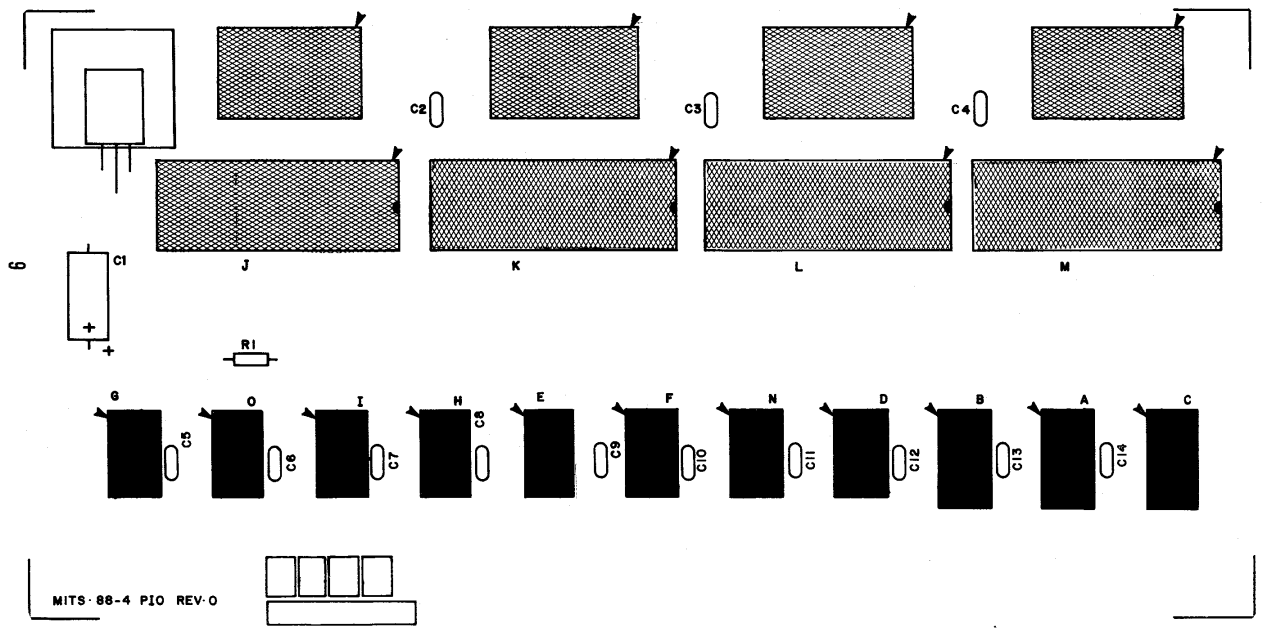
3. Holding the capacitor in place, turn the board over and bend the two leads slightly outward. Solder the leads to the foil pattern and clip off any excess lead lengths.

4. Be sure that there are no solder bridges, and check each ceramic disk capacitor off of the parts list on page 8 after it is installed.

RESISTOR AND CAPACITORS

Silk Screen Designation	Part	Value
( ) R1	Resistor (brown-black-red-gold)	1/4 or 1/2 W
( ) C1	Electrolytic Capacitor	30 µf or greater
( ) C2 ( ) C3 ( ) C4	Ceramic Disk Capacitor	1 µf or greater
( ) C5 ( ) C6 ( ) C7		
( ) C8 ( ) C9 ( ) C10		
( ) C11 ( ) C12 ( ) C13		
( ) C14		

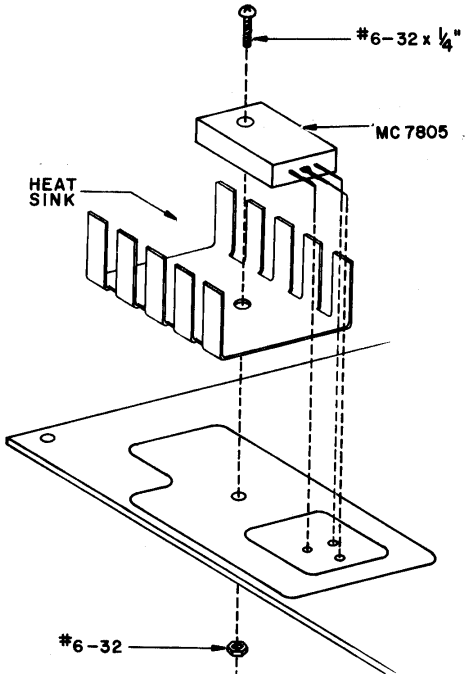
Screened blocks designate partially-installed components.



VOLTAGE REGULATOR INSTALLATION

There is one 5-volt regulator to be installed on the 88-4PIO board.

1. Set the voltage regulator in place on the board and align the mounting holes. (See drawing below.)



2. Use a pencil to mark the point on each of the three leads where they line up with their respective holes on the board.

3. Using needle-nose pliers, bend each of the three leads at a right angle on the points where you made the pencil marks.

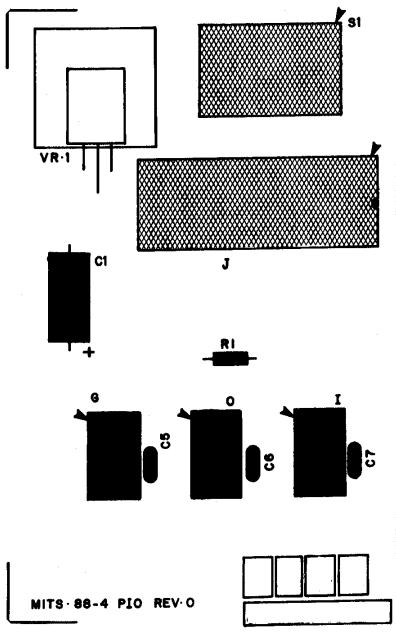
NOTE: Use heat-sink grease when installing this component. Apply the grease to all surfaces which come in contact with each other.

4. Referring to the preceding drawing, set the regulator and heat sink in place on the silk-screened side of the board. Secure the regulator and heat sink as shown by the drawing, holding the regulator in place as you tighten the nut.

5. Turn the board over and solder the three leads to the foil pattern on the back side of the board. Be sure not to leave any solder bridges.

6. Clip off any excess lead lengths, and place a checkmark in the blank provided below.

( ) VR1



HARDWIRE CONNECTIONS

There are four address selection jumpers and from one to eight optional interrupt jumpers to be connected on the 88-4PIO board. The connections for the address selection and the interrupt jumpers must be made with the insulated wire included in the kit.

Referring to the component layout on page 12 and the Address Selection Chart on page 13, connect the address selection jumpers as follows:

1. Choose the address selection you want to use according to the Address Selection chart. Be sure that the octal address group that you choose is not used by any other I/O board. Refer to the Theory of Operations in the front on this manual for further explanation of address selection.

2. Connect pads 4-7 to pads A4 or $\overline{A4}$-A7 or $\overline{A7}$ according to the pattern indicated by the Address Selection Chart to obtain the octal address you have chosen. Example: In order to implement octal address 000-017, it is necessary to connect pads 7 to $\overline{A7}$, 6 to $\overline{A6}$, 5 to $\overline{A5}$ and 4 to $\overline{A4}$.

3. Bend the leads to fit the corresponding holes. Insert the leads into the correct holes from the silk-screened side of the board.

4. Turn the board over and solder the leads to the foil pattern on the back side of the board.

The 88-4PIO board is designed to provide the capability for interrupt at eight levels via the 88-Vector Interrupt, at one level via the interrupt request line provided on the 88-4PIO board, or no interrupt at all. Any one of these three options may be implemented.

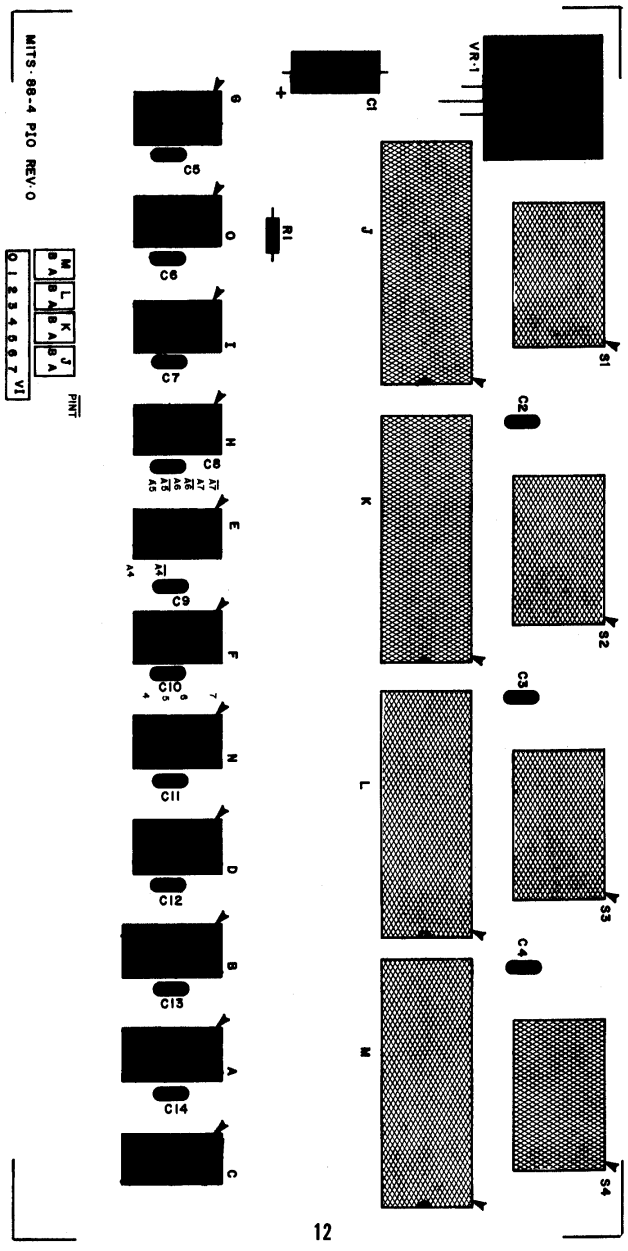
NOTE: The processor is capable of handling only one interrupt system. If the single level interrupt request line of the 88-4PIO board is implemented, no other board can be hardwire connected to the processor for interrupt. Refer to the Theory of Operation section for further explanation of interrupt functions.

If you choose to implement the single interrupt system, connect the jumper wires as follows:

1. Choose which interrupt request lines (JA, JB, KA, KB, LA, LB, MA, MB) you want to use.

2. Connect the chosen interrupt request line or lines with the pad marked $\overline{PINT}$. Using the component leads saved earlier in the assembly procedure, bend the leads as necessary and insert them into the correct holes from the silk-screened side of the board. All interrupt request leads must be inserted in the hole marked $\overline{PINT}$.

3. Turn the board over and solder the leads to the foil pattern on the back side of the board. Clip off any excess lengths.


MITS-88-4 PIO REV.0
VR-1
C1
R1
C2
C3
C4
S1
S2
S3
S4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
PINT

I/O ADDRESS SELECTION CHART

Address Octal	Connections 7	6	5	4
000-017	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$
020-037	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	A4
040-057	$\overline{A7}$	$\overline{A6}$	A5	$\overline{A4}$
060-077	$\overline{A7}$	$\overline{A6}$	A5	A4
100-117	$\overline{A7}$	A6	$\overline{A5}$	$\overline{A4}$
120-137	$\overline{A7}$	A6	$\overline{A5}$	A4
140-157	$\overline{A7}$	A6	A5	$\overline{A4}$
160-177	$\overline{A7}$	A6	A5	A4
200-217	A7	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$
220-237	A7	$\overline{A6}$	$\overline{A5}$	A4
240-257	A7	$\overline{A6}$	A5	$\overline{A4}$
260-277	A7	$\overline{A6}$	A5	A4
300-317	A7	A6	$\overline{A5}$	$\overline{A4}$
320-337	A7	A6	$\overline{A5}$	A4
340-357	A7	A6	A5	$\overline{A4}$
360-377	A7	A6	A5	A4

40-PIN IC INSTALLATION

The 40-pin IC(s) can be installed now.

1. Review the "MOS IC Special Handling Procedures" on page 5 of the ALTAIR 8800 Assembly Manual. Note, failure to carefully follow the instructions of the "MOS Special Handling Procedures" may result in permanent damage to static-sensitive ICs.

2. Insert the 6820 IC(s) into the socket(s) on the 88-4PIO board. Handle the IC(s) carefully, and use as little pressure as possible when inserting the IC(s).

INTERCONNECTIONS AND BOARD INSTALLATION

Install the 24-pin connector cable(s) as follows:

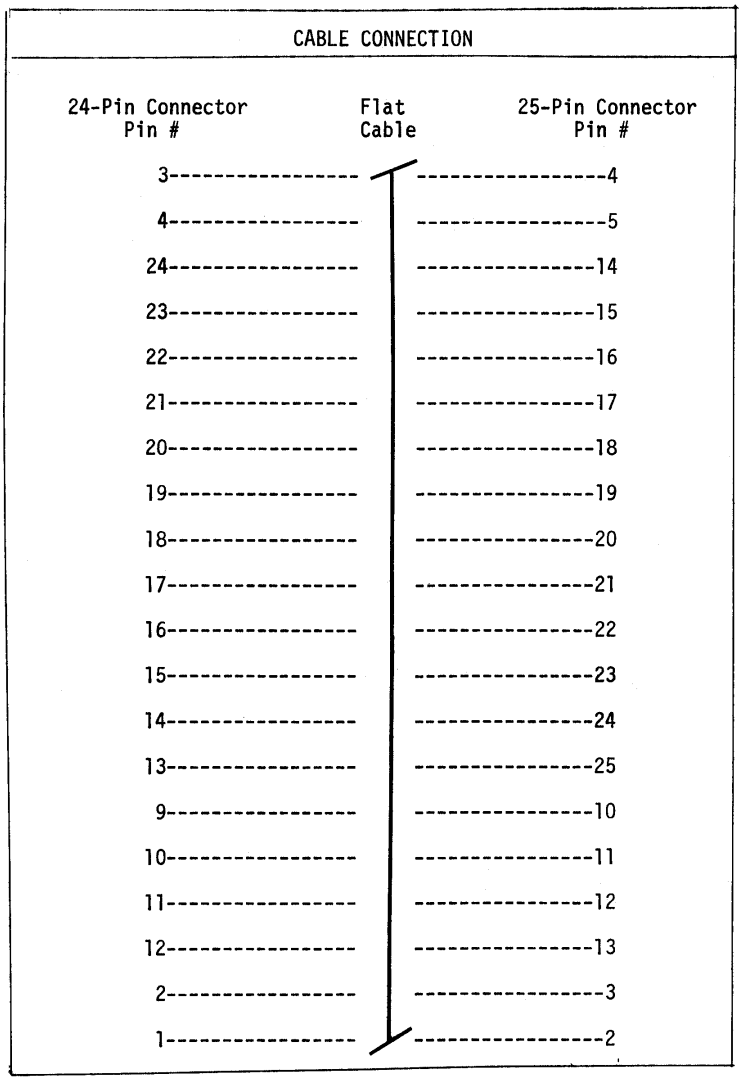
1. Insert the 24-pin connector(s) into the socket(s) on the 88-4PIO board. Be sure that the cable(s) extend across the top edge of the board.

2. Press the 88-4PIO board into any available edge connector in the ALTAIR 8800, with the silk-screened side of the board facing toward the chassis.

3. Straighten the connector cable(s) and place the 25-pin connector into the appropriate hole(s) on the back panel.

4. Attach the 25-pin connector with the screws provided. Before screwing the 25-pin connector(s) to the back panel of the ALTAIR 8800, be sure that the cables are not twisted.

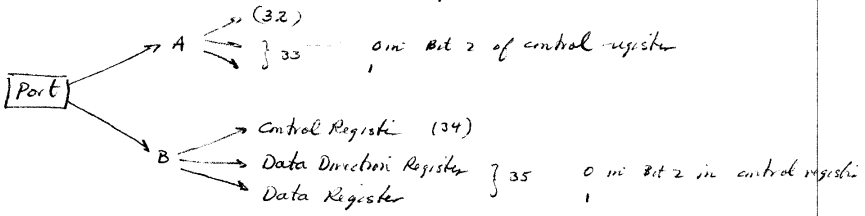
CABLE CONNECTION



Initialising 4P10

Ports 40-57 (4 ports actually) (June 76 issue of Computer note)

Note 40 octal = 32 decimal



Data Direction Register Initialisation (will do one port only)

- Out 32, 000
- Out 34, 000

will now select DDR

1 in DDR ⇒ output
0 in DDR ⇒ input

Set A = input, B = output

- Out 33, 000
- Out 35, 255

A Section control

- Out 32, 38 100110 enable data register

replace with 44 decimal

CA1 low active
disable interrupts
If CA1 = 1 then status Bit 7 set high and input device is ready
Makes CA2 as output to act as busy signal - goes high after CA1 because A data channel
CA1 high ⇒ keyboard may now send

B Section Control

- Out 34, 38 100110

CB2 is output busy signal
CB2 low tells printer that data is available
CB1 low means printer is ready for new data

Echo (after initialization)

- If 128 AND Inp(32) = 0 then loop (If Bit 7 Low, loop)
- S = Inp(33) (Data in)
- If 128 AND Inp(34) = 0 then loop (If Bit 7 Low, loop)
- Out (35)
- Clear flag on B input Input (35)

Test routine

Initialize

```
Out  32,0
Out  34,0
Out  33,0
Out  35,255
Out  32, 38
Out  34, 38
```

- 44 gives pulse on pin 13 of DB-25

Square wave output

```
10  Out 35,0
20  Out 35,255
30  GO TO 10
```

} can be replaced by strobe above

pulse duration is down 1.7 usec.