

ALTAIR 88-DIAGNOSTIC CARD USER'S GUIDE

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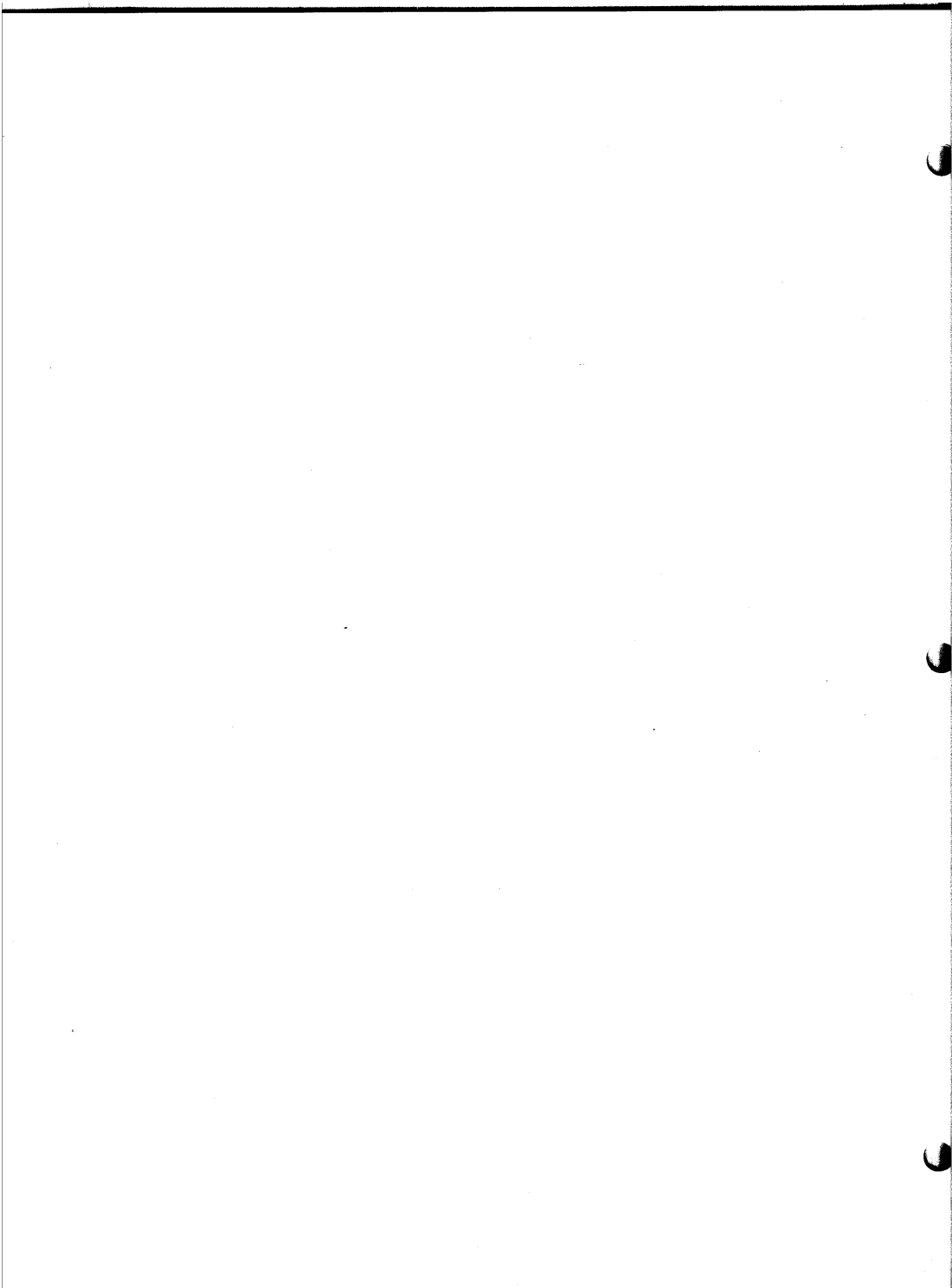


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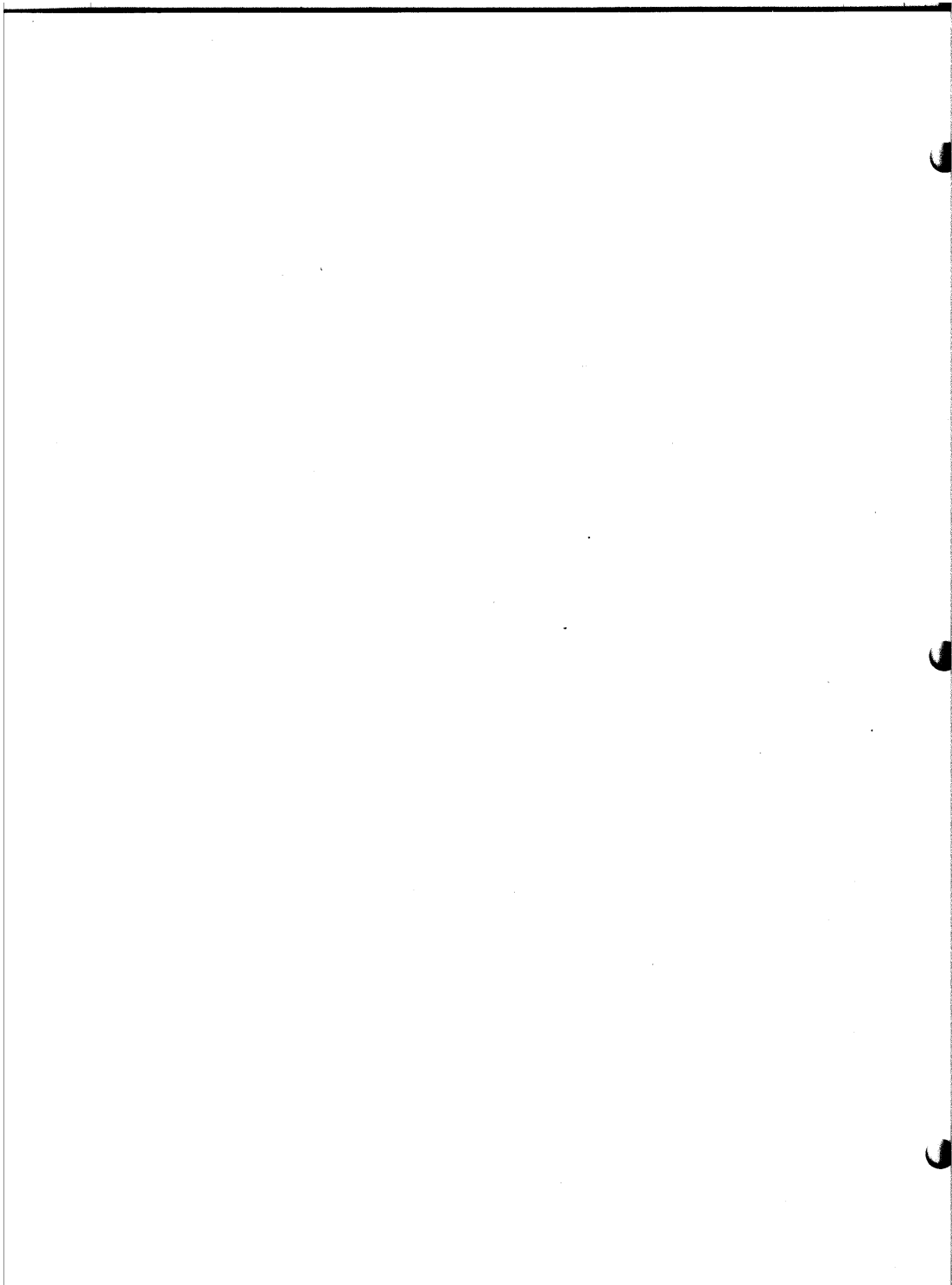
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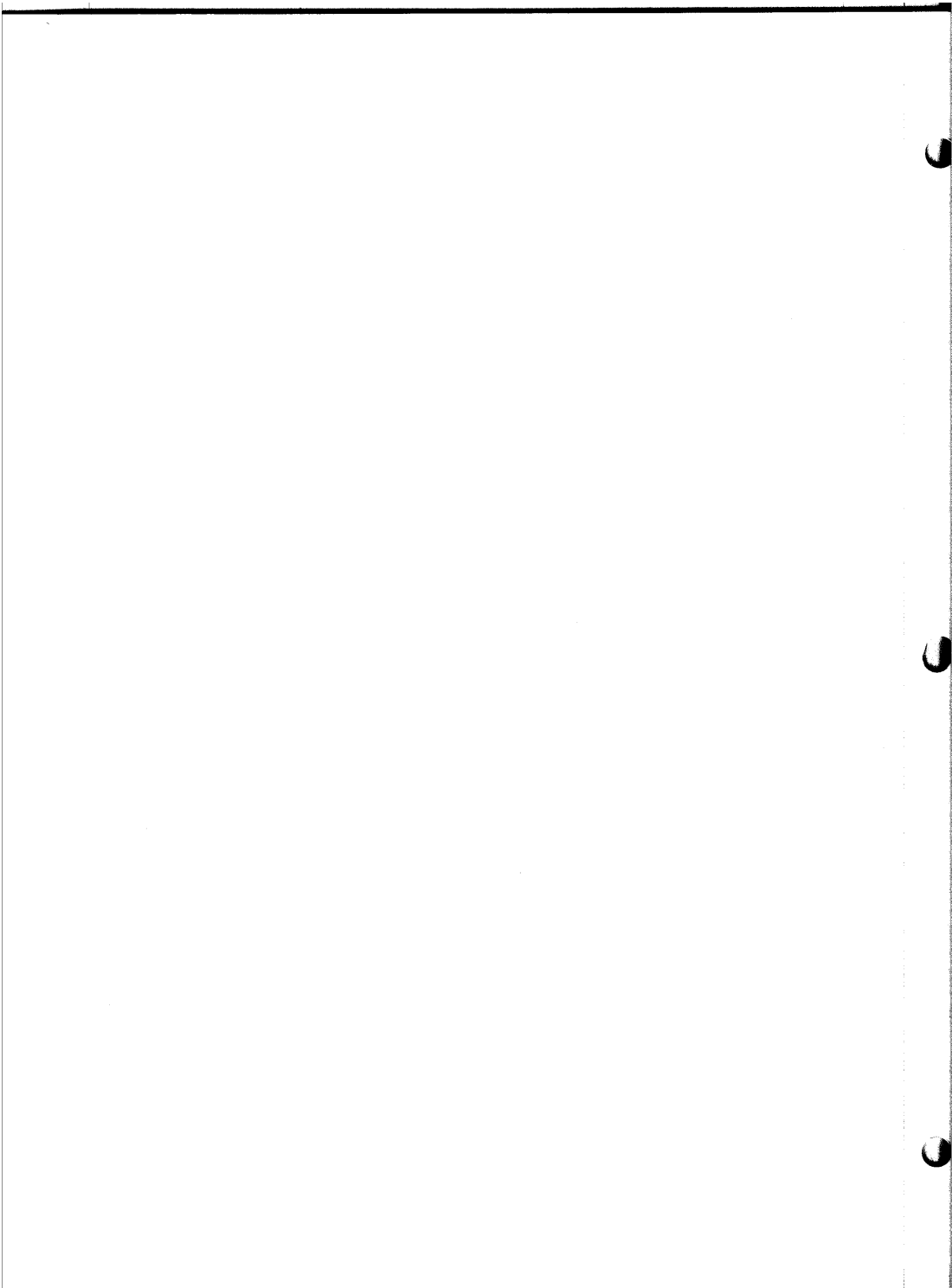
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SECTION I
88-DC
INTRODUCTION

88-DC
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1. INTRODUCTION

1-1. Description

The Altair™ 88-DC Diagnostic Card provides a precise, effective method of troubleshooting for the Altair 8800 computer. The card offers three main functions using the following devices:

- 1) An Eight-Bit-to-Octal Decoder/Display that allows the user to examine the data on any of the lines on the Altair bus;
- 2) A Digital Voltmeter, switch-selectable between bus (+8v, +18v, -18v) and External Input (+9.99v full scale range) that can be used to measure the on-card regulator voltages;
- 3) An Output Jack for oscilloscope display referencing of data and control signals. The Synchronization is selectable from the Data Out and Data In lines and 16 control signals to provide a stable oscilloscope display.

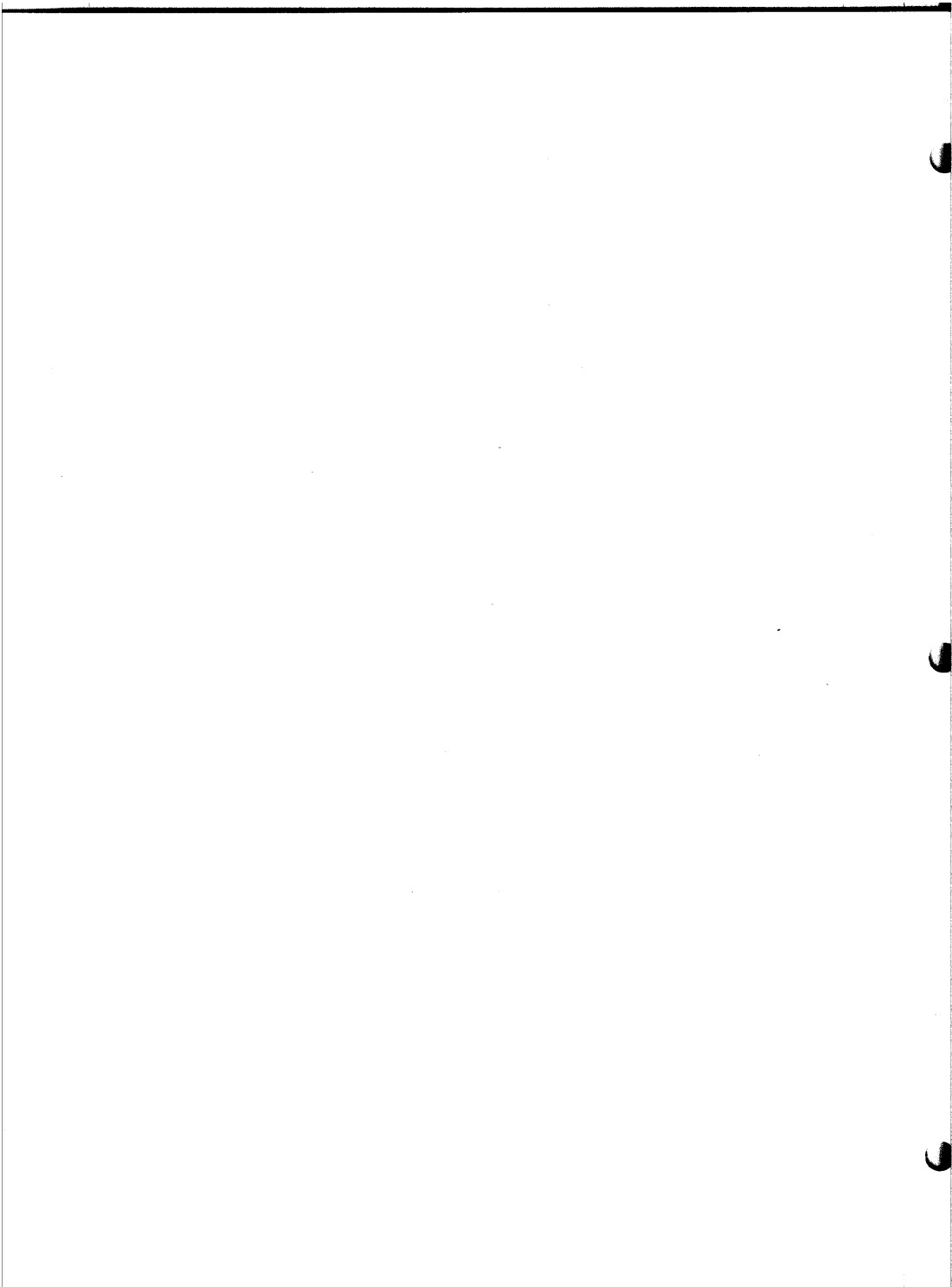
Any combination of data, address and control lines can be selected (except where redundancy of DIP switches causes the computer to become inoperative--see Paragraph 2-3) to display up to eight signals on a single channel oscilloscope.

Troubleshooting of individual boards with critical timing relationships is possible through the 10-pin right angle connector which acts as an external input. (Assembly of a special user-supplied cable is required to meet individual needs.)

1-2. Scope and Arrangement

The 88-DC User's Guide is divided into two main parts:

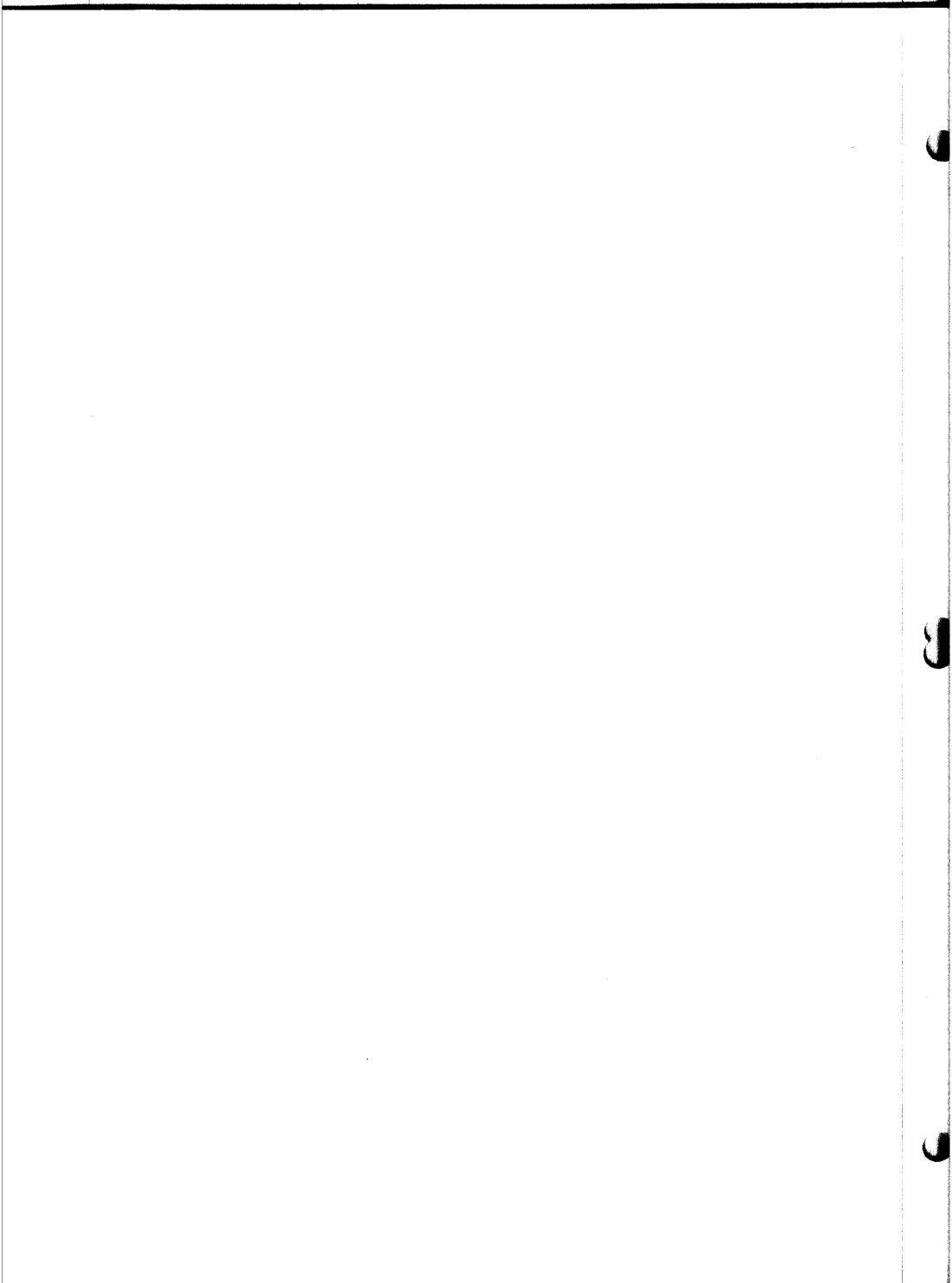
- 1) a brief theory of operation section, complete with schematics, designed to give the user a basic understanding of the card's circuit operation;
- 2) directions for system integration.



SECTION II
88-DC
THEORY OF OPERATION

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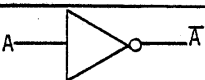
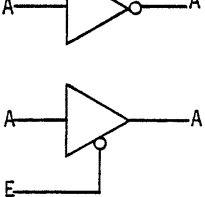
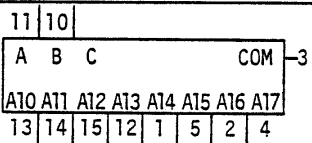
2. THEORY OF OPERATION

2-1. General Contents

Section II contains a description of the circuitry operation of the 88-DC card, with references to the schematics, Figures 2-1 and 2-2. The logic symbols used in these figures are explained in Table 2-A, which presents the functional name, symbolic representation and a brief description of each logic circuit.

The active state of the inputs and outputs of the circuits is graphically displayed by the presence or absence of small circles. A circle at the input of a circuit indicates that the input is an active LOW; i.e. a LOW signal will enable the input. A circle at the output of a circuit indicates that the output is an active LOW; i.e. the output is LOW in the actuated state. Conversely, the absence of a circle indicates that the input or output is active HIGH.

Table 2-A. Symbol Definitions

Name	Logic Symbol	Description
NAND gate	 $Y = \overline{AB \dots N}$	<p>The NAND gate performs one of the fundamental logic functions. All of the inputs have to be enabled (HIGH) to produce the desired (LOW) output. The output is HIGH if any of the inputs are LOW.</p>
Inverter		<p>The inverter is a device whose output is the opposite state of the input.</p>
Non-Inverting Bus Driver		<p>The non-inverting bus driver is a device whose output is the same state as the input. Data is enabled through the device by applying a (LOW) signal to the E input.</p>
Eight-Channel Analog Multiplexer (MUX)		<p>This eight-channel multiplexer has three binary control inputs (A, B and C) which select one of eight channels (A10-A17) to be turned on and connected to the output (COM).</p>

Name	Logic Symbol	Description
Digital Multi-plexer		<p>The digital multiplexer contains full on-chip decoding to select one of eight data sources. The chip has a strobe input which must be at a low logic level to enable these devices. A HIGH level at the strobe forces the W output HIGH, and the Y output (as applicable) LOW.</p>
Analog Multi-plexer	<p style="text-align: center;">TOP VIEW</p>	<p>The Analog multiplexer has three binary control inputs (A, B and C) and an inhibit input. The three binary signals select one of eight channels to be turned "ON" and connect the input to the output.</p>

2-2. Power Supply (Figure 2-1)

The +5v regulated DC voltage, which supplies V_{CC} for most of the ICs, is provided by a 3 amp voltage regulator, VR1 (zone D7). Current is input to VR1 from pins 1 and 51 (the unregulated +8v bus).

The -5v regulated DC voltage is supplied to IC D (zone B2) from regulator Q1 (zone D8). IC D draws approximately 3mA of current.

2-3. Digital Voltmeter (Figure 2-1)

The DVM section of the card allows voltages to be tested and numerically displayed on LEDs 1, 2 and 3 (zones B5 through B3). Voltage levels are converted to a 3-digit number by means of a CMOS A/D Converter, IC D (zone B2). IC D utilizes the "quantized feedback" conversion technique which provides auto-zero and auto-polarity functions to eliminate the need for additional external circuitry. The auto-zero feature also regulates drift automatically. The circuit is made functionally complete by the addition of C_{AZ} (C2), C_{INT} (C3), C_{OSC} (C6), V_{REF} (D2) and ± 5 volt supplies (VR1 and Q1).

Switch S1 has four switch selectable inputs (+8v, ± 18 v and EXT) which are calibrated by the adjustment of the corresponding trim pots: R1 for +8v, R2 for +18v, R3 for -18v and R4 for EXT. The Binary Coded Decimal (BCD) output of IC D is sent to IC E (zone B2) which is a BCD-to-7-segment decoder. The output then goes through resistor pack RP1 which contains seven 68 ohm resistors, and to the anodes (A-G) of the LED displays.

The Digit Strobe outputs of IC D (pins 7, 8 and 9) are switched by Q3, Q4 and Q5 (zones B4, B4 and B3, respectively). The "Sign/Over-Range" output (indicating polarity or excessive voltage) on pin 5 goes to Q2 (zone B6). D1 is turned on if it receives a positive input from Q2 and off if a negative input is received. D1 and LEDs 1, 2 and 3 flash in an over-range condition.

The reference voltage (V_{REF}) to pin 2 of IC D is furnished by D2 (zone A1), a 2v zener diode. C2, the auto-zero capacitor (C_{AZ}) has an optimum value of .1mf over the full sampling range. C3, the integrator capacitor (C_{INT}) and C6, the oscillator capacitor (C_{OSC}) determine the sampling rate (approximately 5 samples/second). The C_{OSC} frequency is approximately 30KHz.

The input impedance of IC D is >1000 megohms. Power consumption is 25 milliwatts, typical, and the accuracy is better than 1%. The External Input range of the digital voltmeter is $\pm 9.99\text{v}$ with 10mv resolution. Resolution on the +8v position is also 10mv, and resolution on the $\pm 18\text{v}$ positions is 100mv. Decimal point placing is determined by S1 (zone A6).

2-4. Multiplexed Oscilloscope Display Circuit (Figure 2-2)

Timing relationships between several signals can be visually checked with the Multiplexed Oscilloscope Display Circuit. Eight signals, selected by a combination of S3, S4 (16 control lines, zones C5 and C6); S9, S10 (A0-A16, zones C6 and C7); S11 (D01-D07, zone C7); and C12 (DI0-DI7, zone C8), can be displayed on a single channel of an oscilloscope. Oscilloscope sync is switch selectable from S5, S6 (16 control signals, zone B2), S7 (D00-D07, zone B3), and S8 (DI0-DI7, zone B3).

The display on the oscilloscope coincides with the silkscreening under the switches. For example:

If the D00-D07 lines are selected for display, they are shown in numerical order (from top to bottom) on the CRT.

If PWAIT, PDBIN, PSYNC, 02, PRDY, 01, MWRITE and SMEMR are selected for display, they appear in the same order on the CRT (from top to bottom).

NOTE

Redundancy of switch selection will cause the computer to become inoperative. For example, if the #2 position of switch S3 (PDBIN) is selected, the #2 position of the other nine switches cannot be selected at the same time.

The display operation is accomplished by applying the eight selected signals to the digital MUX, IC L (zone D6). The MUX Select Inputs (pins 9, 10 and 11 of ICs L and K, zones D6 and C6) are incremented by the 3-bit output from IC J (zone C5) which receives an input frequency of 1953Hz from IC A (zone C4). This frequency is derived through divider IC A (zone C4) from 01 of the system clock.

The 3-bit output of IC J causes IC L to select one of its eight applied signals and increment by one on each count. IC K is simultaneously incremented in the same manner and selects one of eight DC voltage levels. The digital output of IC L (pins 9, 10 and 11, zone D5) and the DC level output of IC K (pins 9, 10 and 11, zone C6) are summed, providing a different DC reference level for each trace and vertically separating the traces from each other on the oscilloscope screen.

The DC level output of IC K goes through Q6 (zone B3) and R14 (zone D4) to the summing point. R14 adjusts the magnitude of DC offset which varies trace separation. The scope's Variable Vertical Sensitivity Control may be used to adjust the overall display amplitude. The hex inverter, IC B (zone C4), is used for signal shaping and inversion where necessary.

The External Sync for the oscilloscope is provided by selecting the desired signal(s) from S5, S6 (16 control signals, zone B2), S7 (D00-D07, zone B3) or S8 (DI0-DI7, zone B3). For example, Sync selection can be used to select a pulse (e.g. the system clock) or a combination of pulses (e.g. an octal word) to reference the signal display. The selected sync signals go to IC C (an 8-input NAND gate, zone A3), then to the BNC connector.

2-5. Octal Display Circuit (Figures 2-1, 2-2 and 2-3)

The Octal Display Circuit provides a simple method for checking short programs by displaying the information being transmitted on the data bus on LEDs 3, 4 and 5. The circuit is switch selectable between the D0 and DI lines via section 1 of switch S2 (Figure 2-2, zone D2).

NOTE

When used with the 8800a computer, the circuit can monitor only the D0 lines.

LED #4 is connected to IC F (Figure 2-1, zone D2) and displays the numbers 0, 1 and 2 only. LEDs #5 and #6 are connected to ICs G and H, respectively, and display the numbers 0 through 7 (the largest octal number being 377). ICs F, G and H are BCD-to-7-segment decoders. Outputs A through G are sent through resistor packs RP1 through RP4 which each contain seven 220 ohm resistors. The signals are then sent to the anodes of the 7-segment displays of LEDs 3, 4 and 5.

In order to conserve power when the circuit is not in use, section 2 of switch S2 disables display decoder ICs F, G and H.

Figure 2-3 is an example of a scope display showing 303_8 . Note that D0, D1, D6 and D7 are HIGH. The narrow lines are switching pulses that may be disregarded.

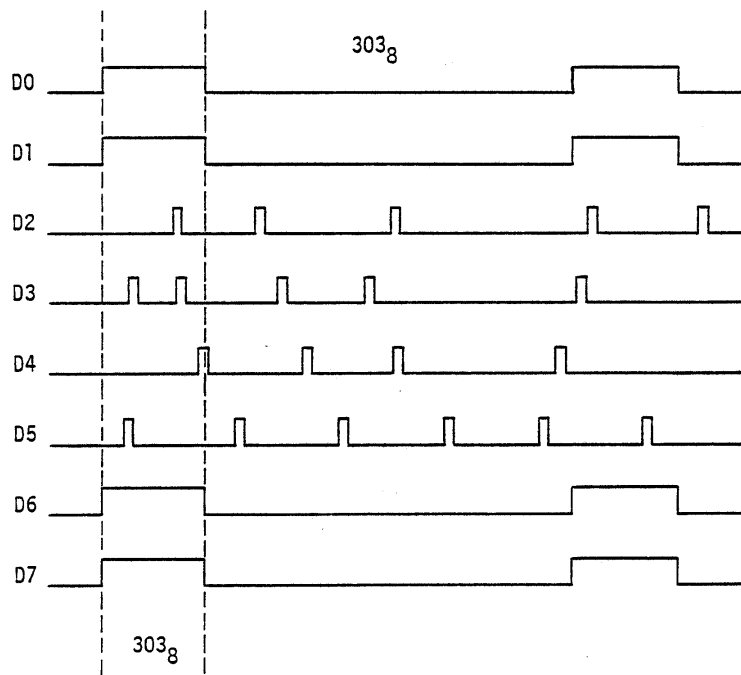
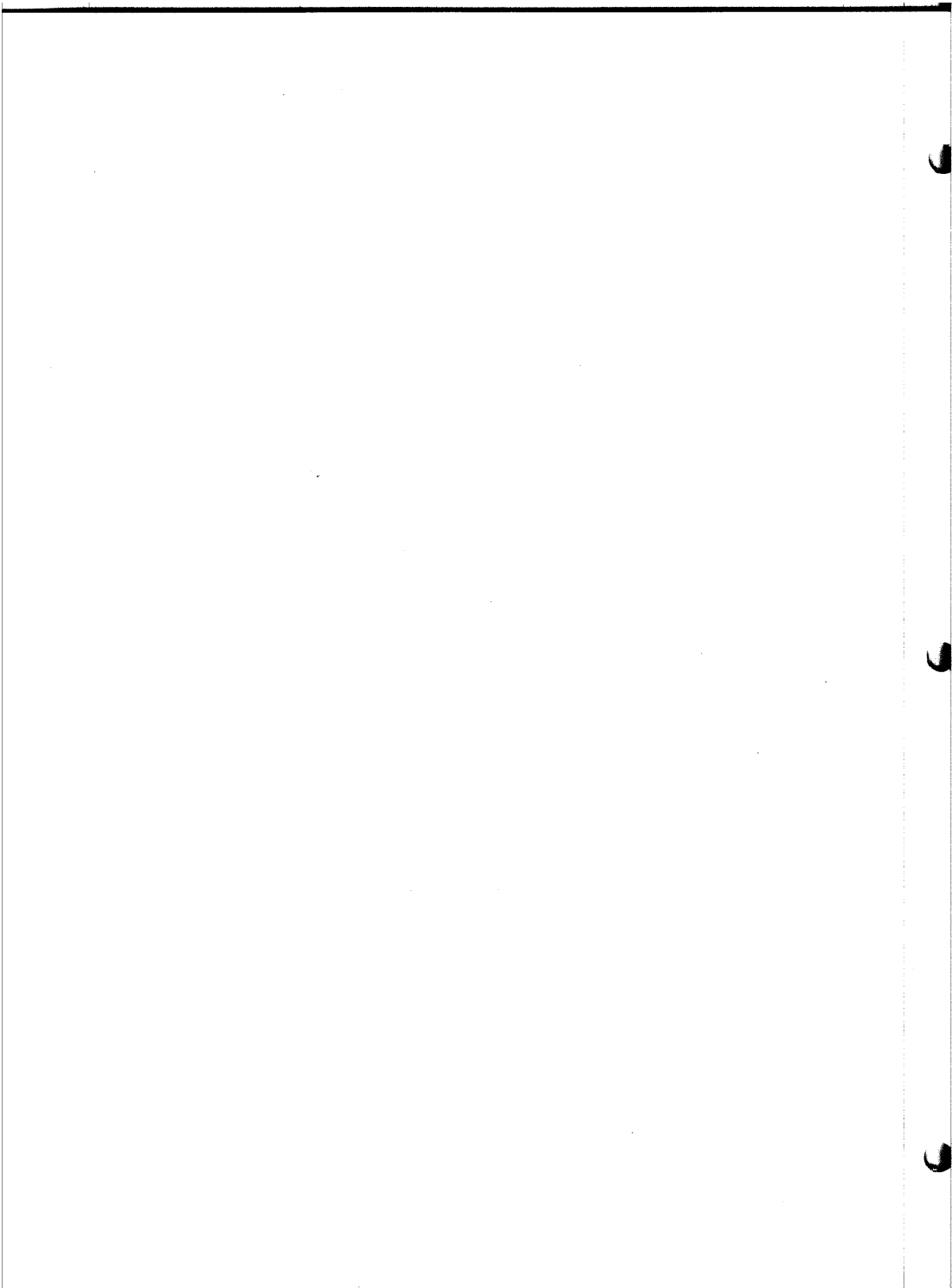
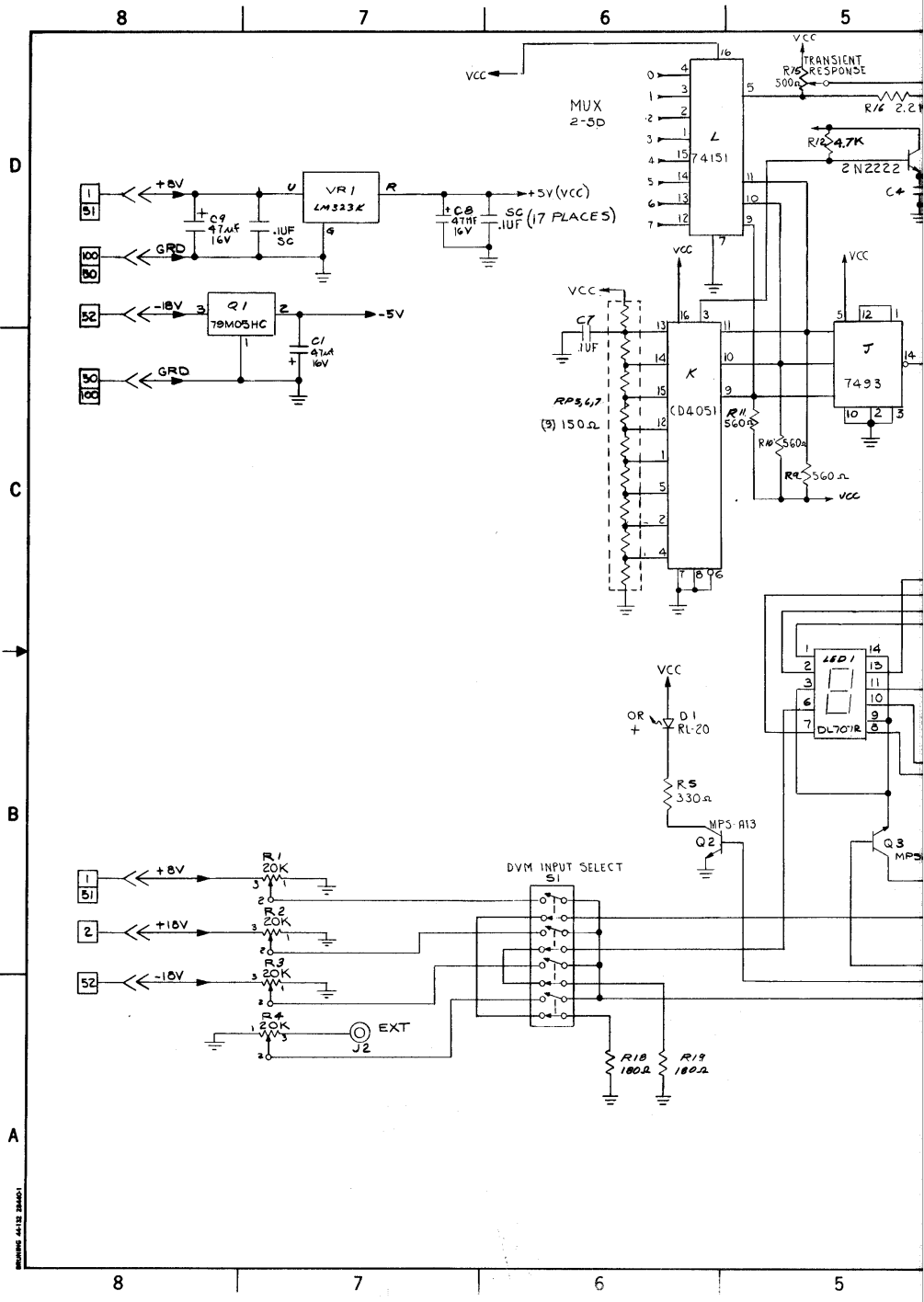
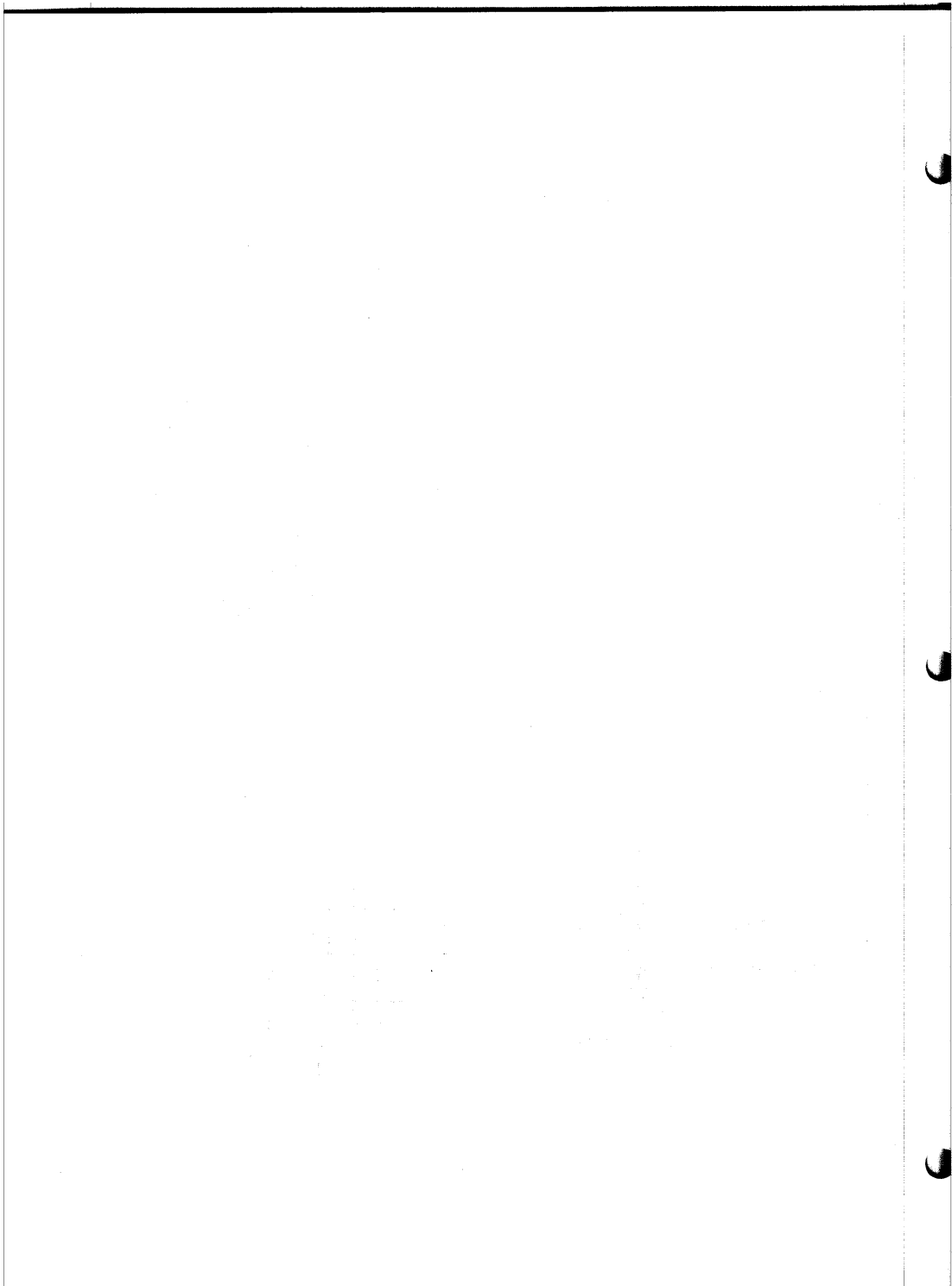


Figure 2-3. 303_8 Oscilloscope Display







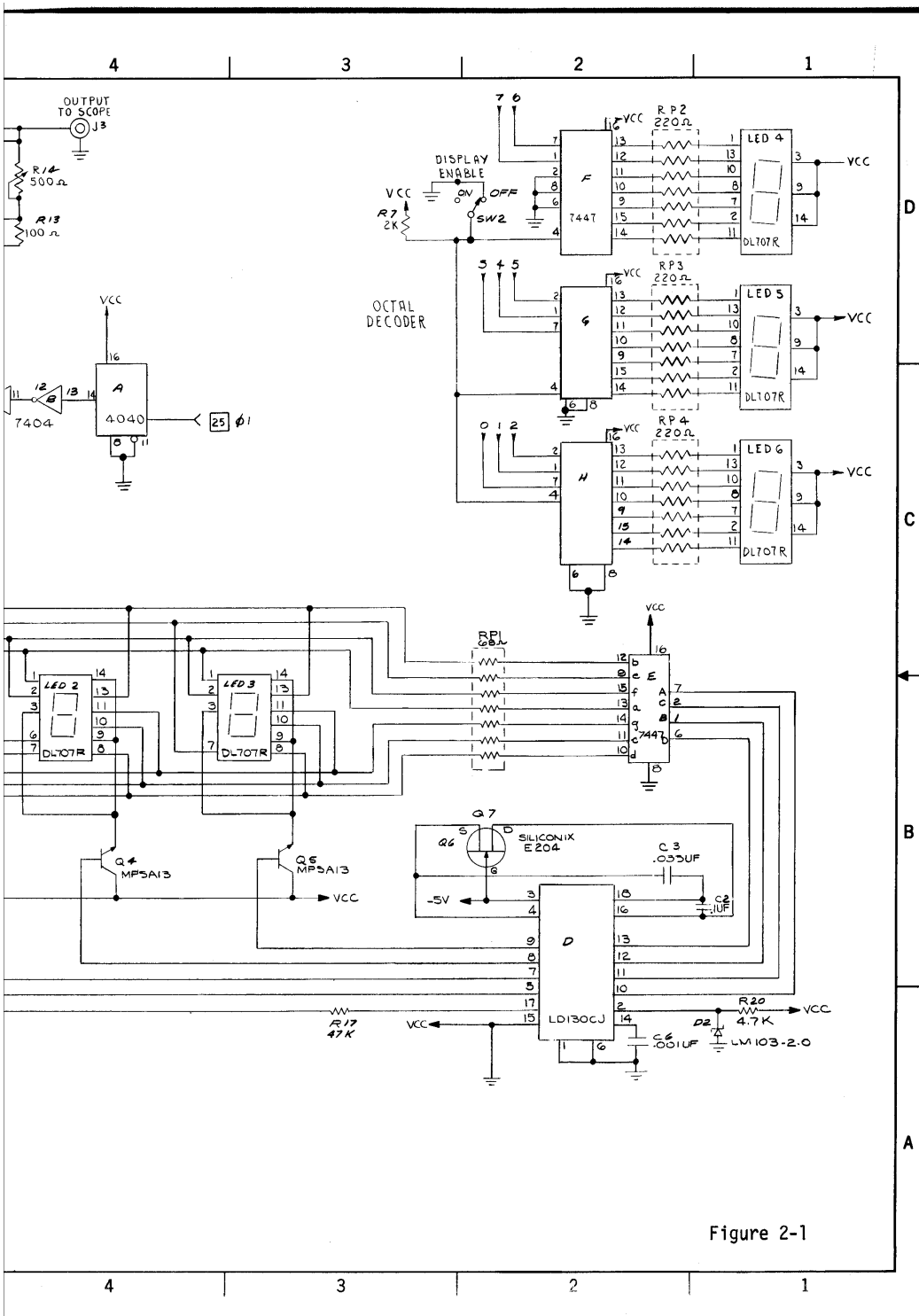
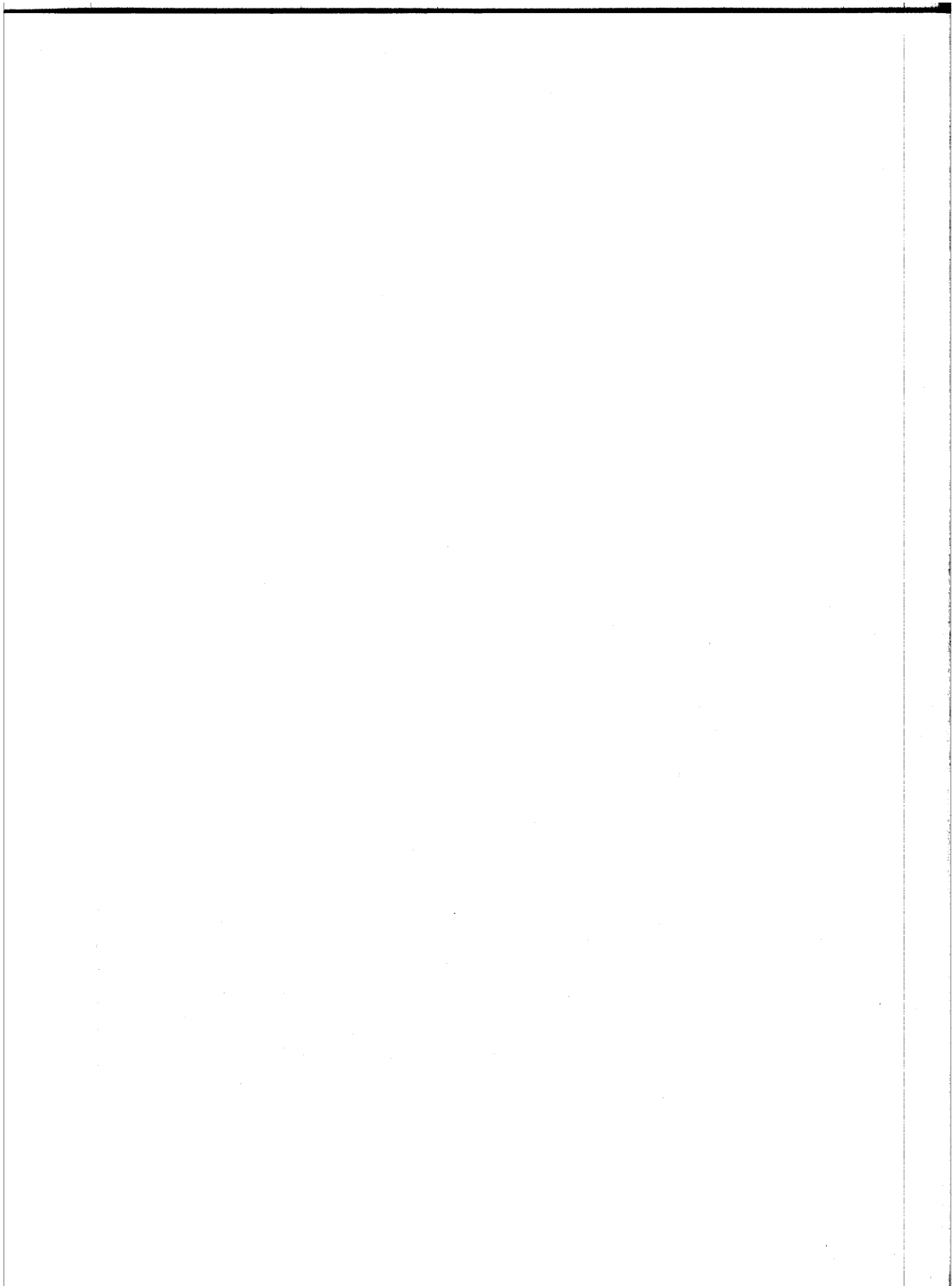
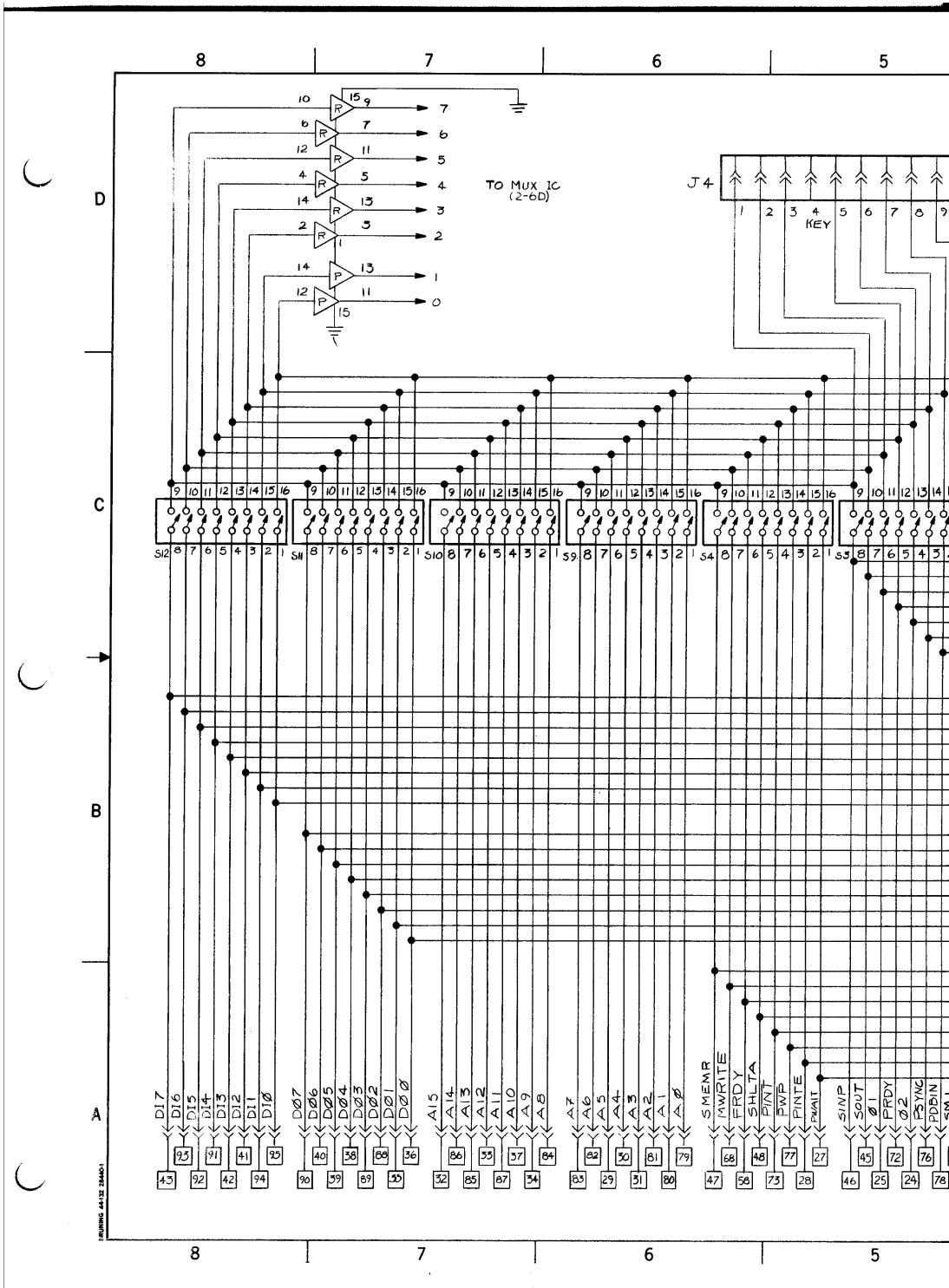
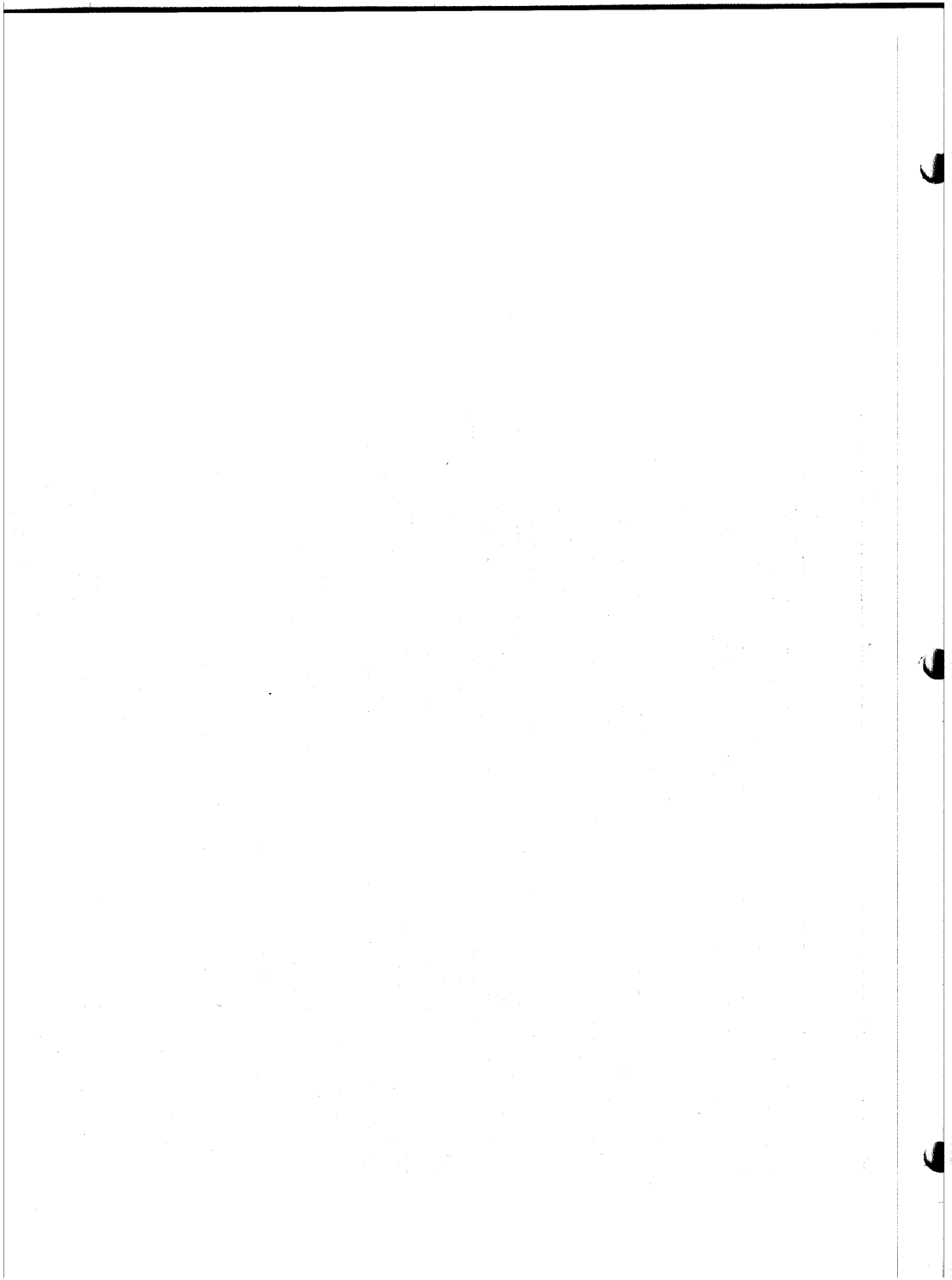


Figure 2-1







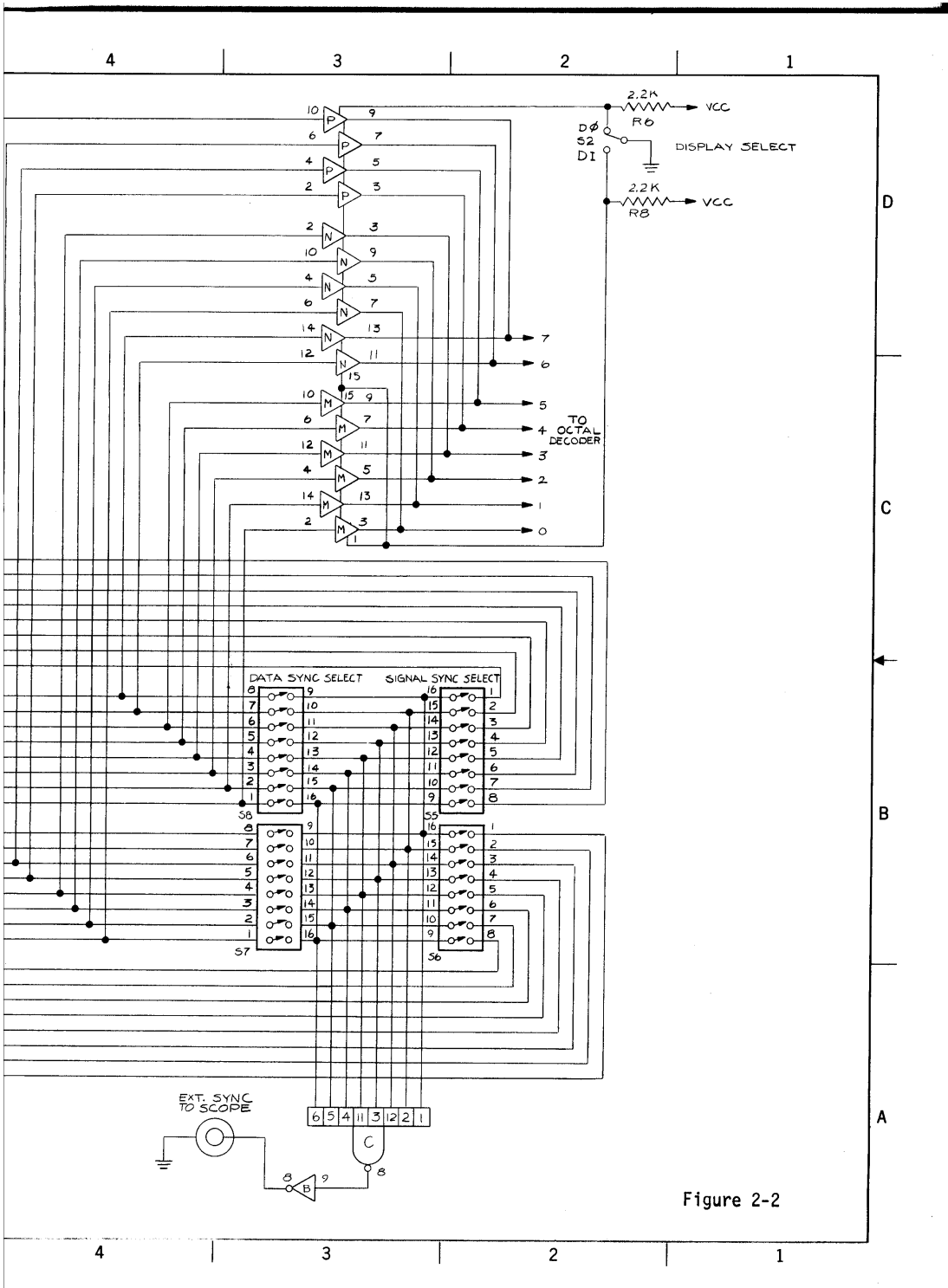
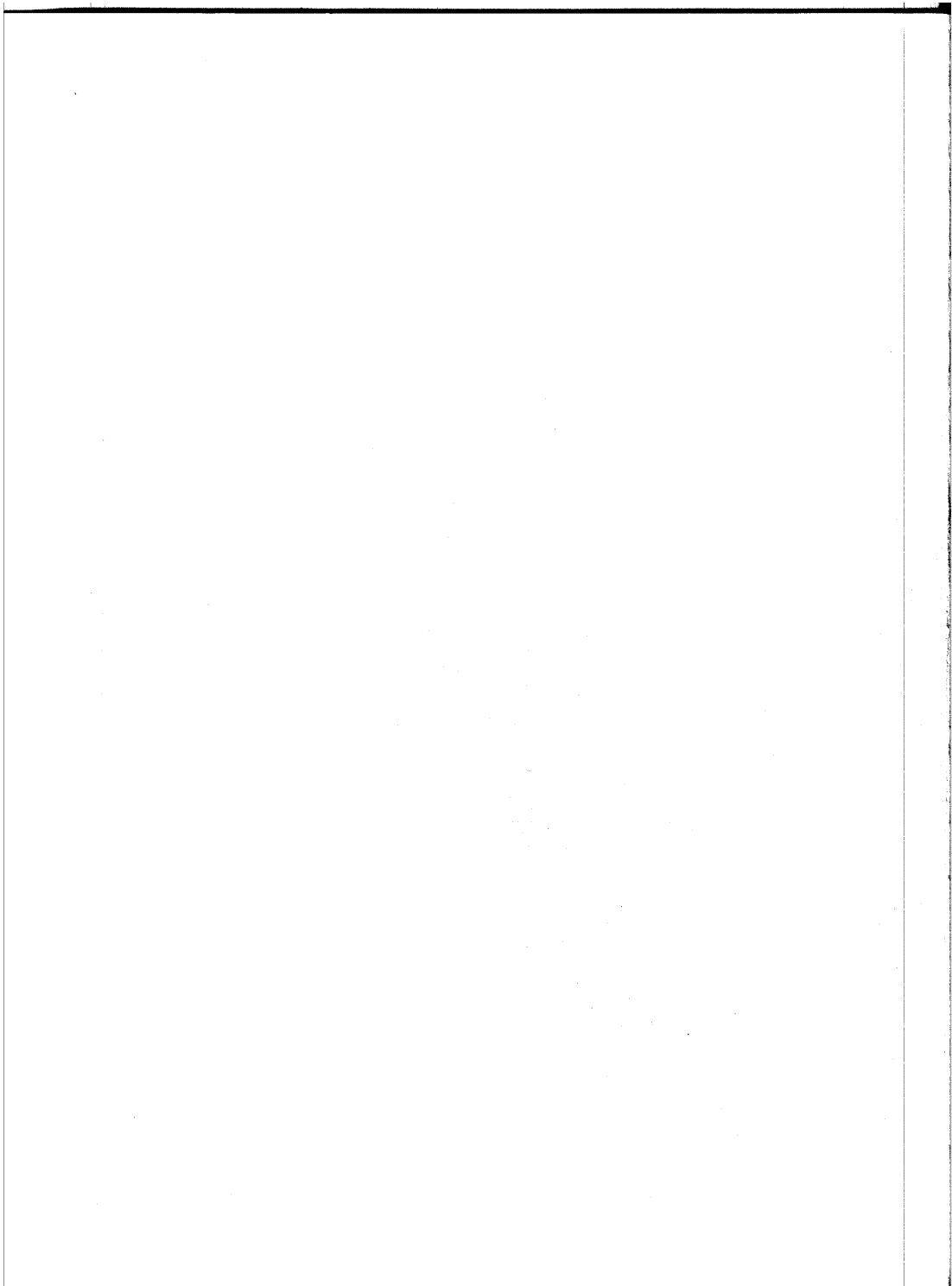


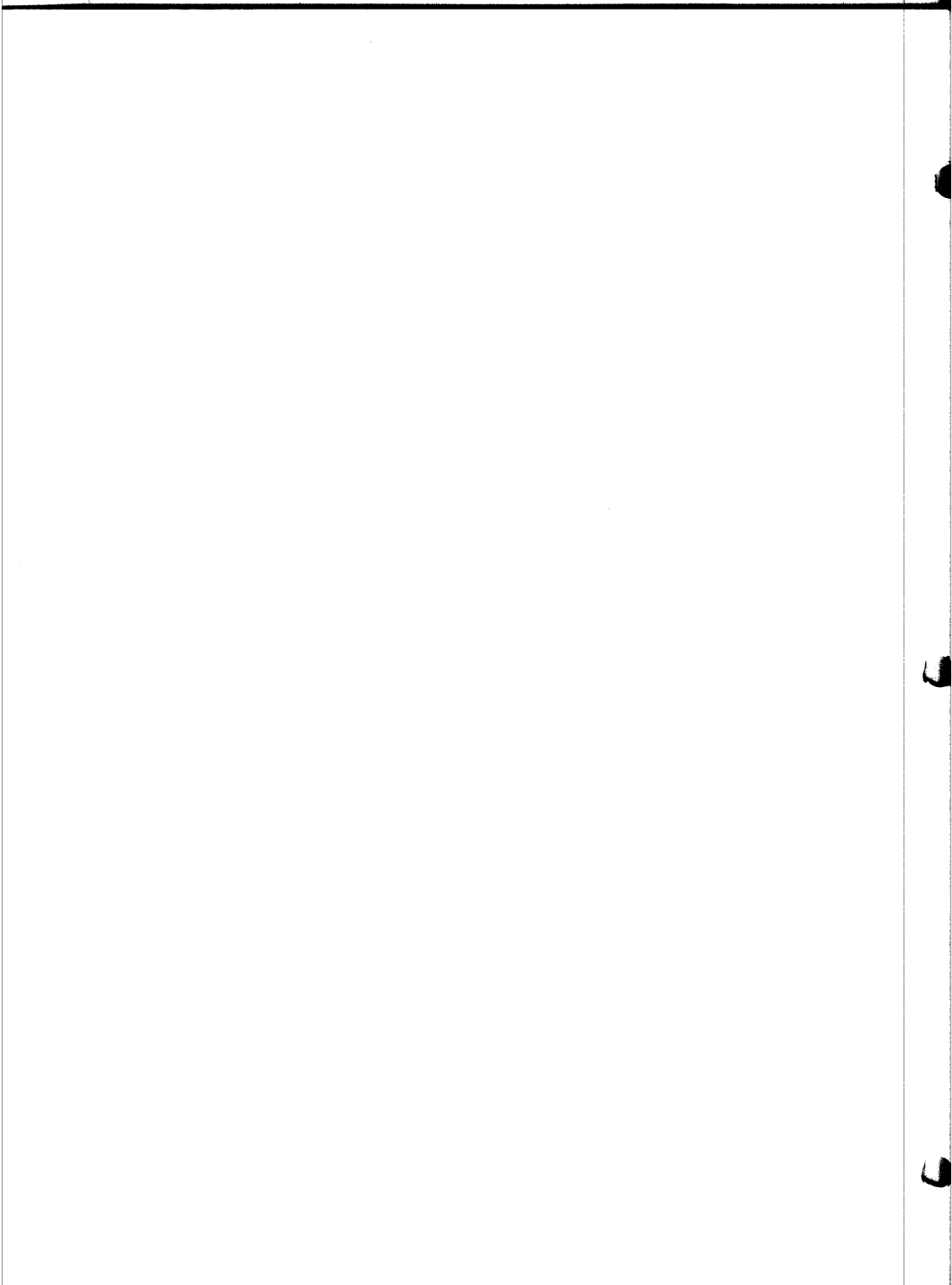
Figure 2-2



SECTION III
88-DC
SYSTEM INTEGRATION

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3. SYSTEM INTEGRATION

3-1. Normal Mode of Operation With Oscilloscope (Figure 3-1)

To connect the sync output, attach one end of a BNC-BNC cable to the "sync output" socket on the 88-DC card and the other end to the "external sync" socket on the oscilloscope.

To connect the data output, attach one end of a BNC-BNC cable to the "data output" socket on the 88-DC card and the other end to the "vertical amplifier" socket on the oscilloscope.

3-2. External Input Mode of Operation With Oscilloscope (Figure 3-2)

To use the external input portion of the board, the user must construct a special cable. One end of the cable must have a 10-pin female socket to plug into the 10-pin male connector on the 88-DC card. The other end (which connects to the problem board) may have "E-Z clips" or "DIP clips" for termination. Sync is selected from the desired signals by means of an oscilloscope probe. A BNC-BNC cable should also be used to connect the 88-DC card's "data output" socket to the oscilloscope's "vertical amplifier" socket. All of the 88-DC card's switches should be turned off while testing in this mode.

Figure 3-1. Normal Mode of Operation

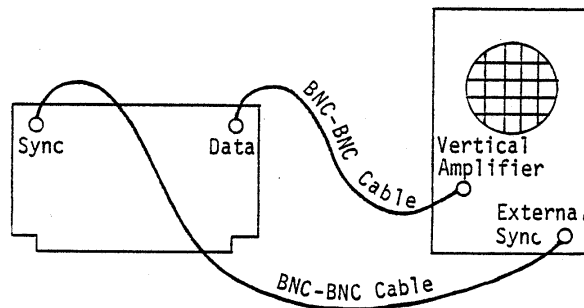


Figure 3-2. External Input Mode of Operation

