PARALLEL I/O BOARD

DOCUMENTATION

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THEORY of OPERATION

PARALLEL I/O BOARD OPERATION

The Parallel I/O Board is designed to interface any 8-bit parallel device to the ALTAIR 8800. The board can be jumpered for any one of 128 addresses and has full hardware interrupt capability. An 8-bit latch for both the input word and the output word act as buffers between the ALTAIR and the external device.

Card Select

The board is selected from the bus by address lines A1 through A7 and the inversion of these lines, $\overline{A1}$ through $\overline{A7}$. When these seven address bits appear at the inputs of IC C as all logic ones (all inputs high), pin 8 of IC C will go low and enable pins 8 & 11 of IC D.

Channel Select

The P I/O Board has both a control channel and a data channel, either of which is selected by the state of address line A0. If the incoming address is an even number (A0 is low), IC D pin 10 will go high and select the control channel.

Control Channel

The control channel is used to test the status of the external device and to operate the interrupt enable/disable circuitry.

The data latches (OUT port IC G & IN port IC H) each contain an internal flip-flop that can be set by their "STB" input. The "STB" inputs may be pulsed high by the "handshake" lines to the external devices, "SBO" for the output device and "SBI" for the input device. These two signals are for the purpose of informing the CPU that the external device has sent or is ready to recieve data. When the "STB" input to these latches is pulsed high, the "$\overline{INT}$" output goes low signifing a ready condition for the particular device.

The "$\overline{INT}$" signals from both latches, G & H, are also buffered and sent to the external devices for additional "handshake" capability on lines "BO" and "BIN".

The control channel line is gated together with the "SINP" line at IC N, pins 9 & 10. When an "IN" instruction is followed by the even address of the board pin 8 of IC N goes low and partially enables IC O at pins 2 & 5, and enables two of the gates of IC L.

Rev Ø

PARALLEL I/O BOARD ERRATA SHEET

PLEASE MAKE THE FOLLOWING CHANGES ON THE PARALLEL I/O BOARD.

CUT THE LAND THAT CONNECTS IC N PIN 11 TO IC E PINS 1, 4, 9 and 12. CUT THIS LAND CLOSE TO PIN 11 OF IC N.

CONNECT IC N PIN 11 TO IC N PIN 5 AND CONNECT IC N PIN 4 TO +5V (at IC N pin 14).

CONNECT IC N PIN 6 TO THE CUT LAND THAT CONNECTS IC E PINS 1, 4, 9 and 12.

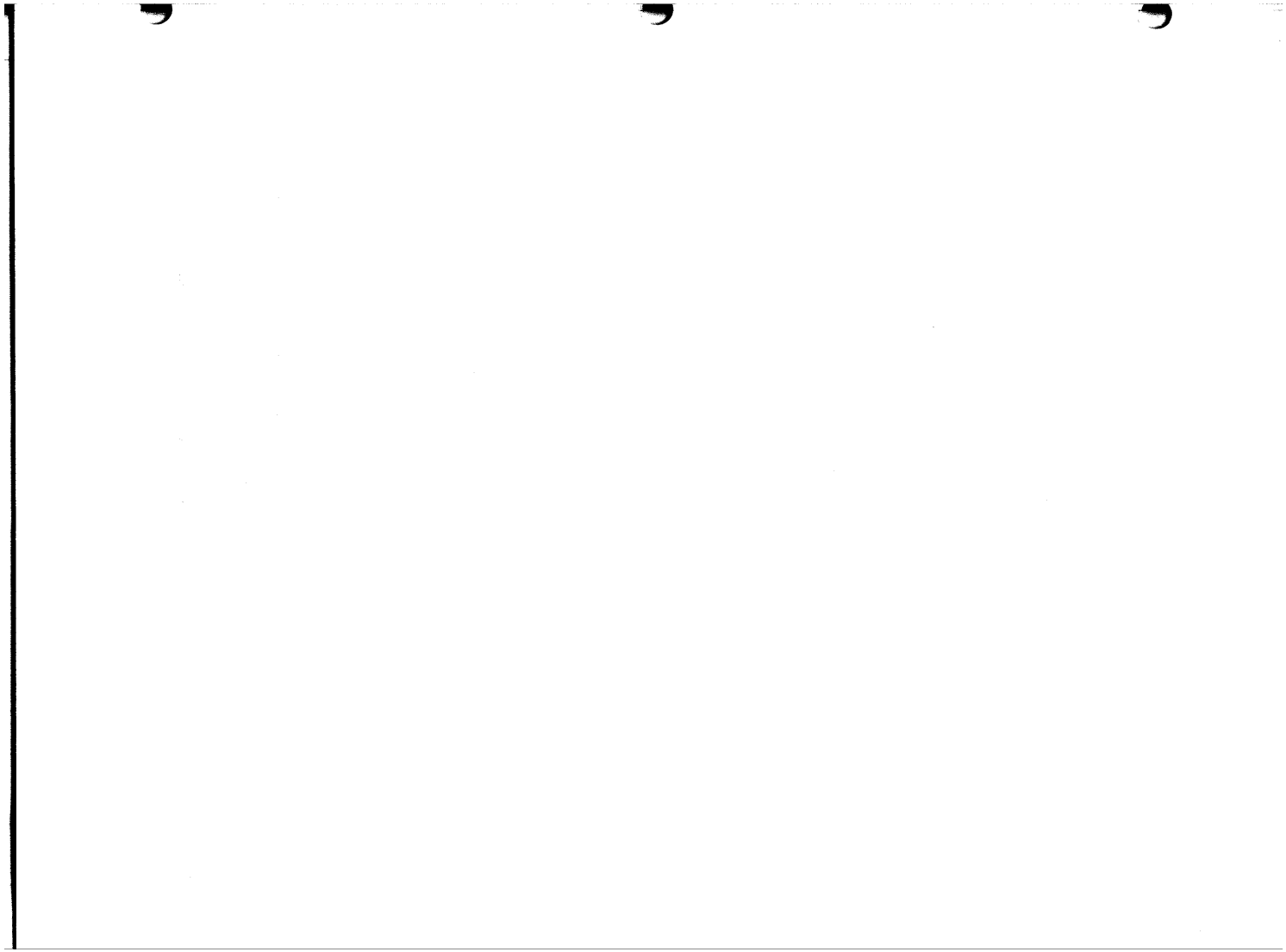
CONNECT IC N PIN 2 TO IC D PIN 13.

NOTE THAT THESE CHANGES ARE REFLECTED ON THE SCHEMATIC.

N: 11-5
14-4

N2 - B13

N6 - E4



88-PIO
Parts List
June 1975

BAG 1

3	74L00	101080
2	74L02	101072
3	74L04	101073
1	74L30	101082
1	7406	101054
4	8T97	101040
1	MC7805	101074

BAG 2

3	1K ohm 1/2W	101928
2	30uF 10V	100369
10	.1uF 10V	100348

BAG 3

2	4 3/4" 26 gauge wire	103006
1	20" 25-conductor cable	103057
2	Card guides	101714
1	100-pin edge connector	101864

BAG 4

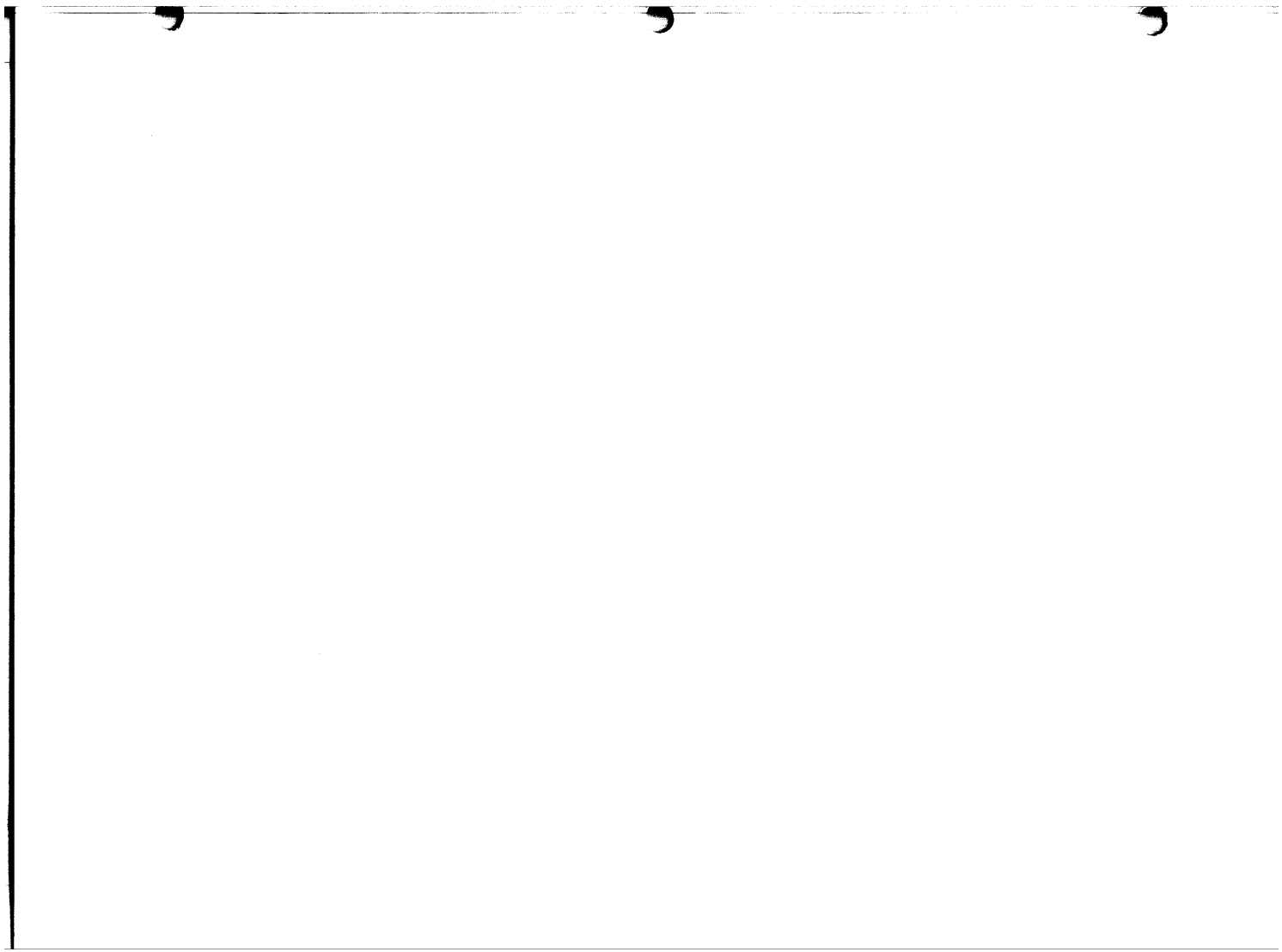
4	1/2"-6/32 screw	100918
1	#6 nut	100933
1	6-32 x 1/4 screw	100917
1	#6 lockwasher	100942
2	10-pin plug	101768
2	10-pin right angle	101812
20	Pins	101769
1	Heatsink (small)	101870

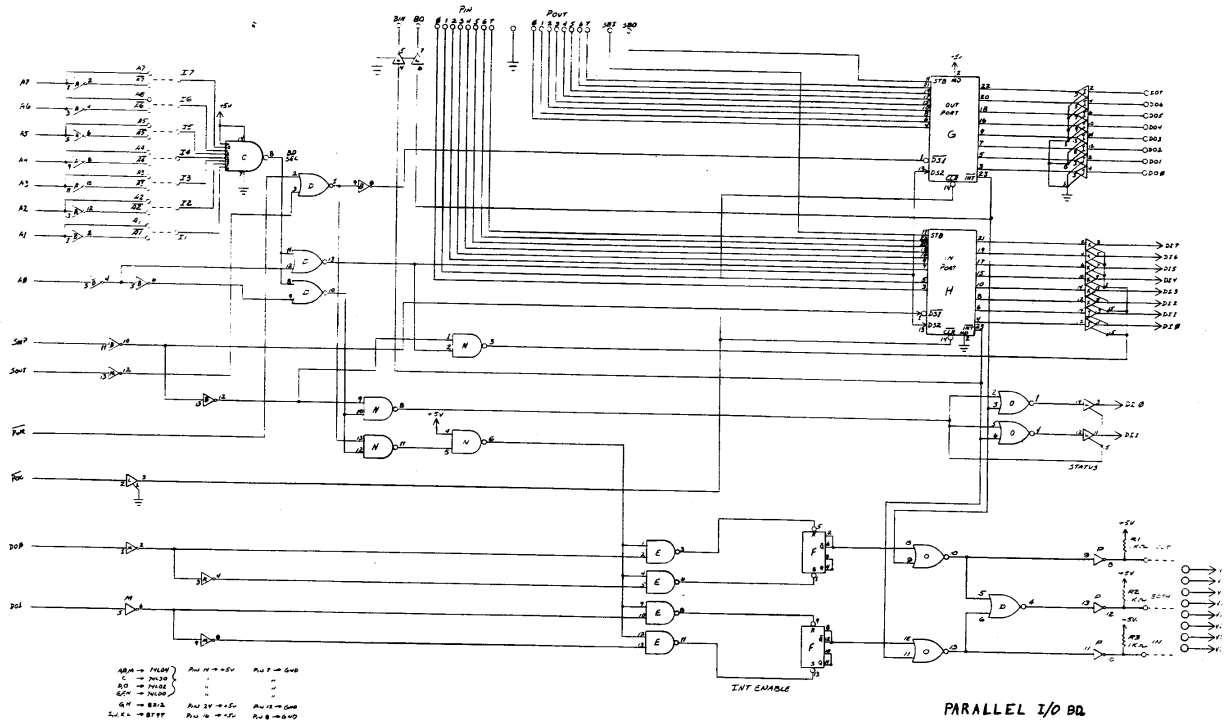
MISCELLANEOUS

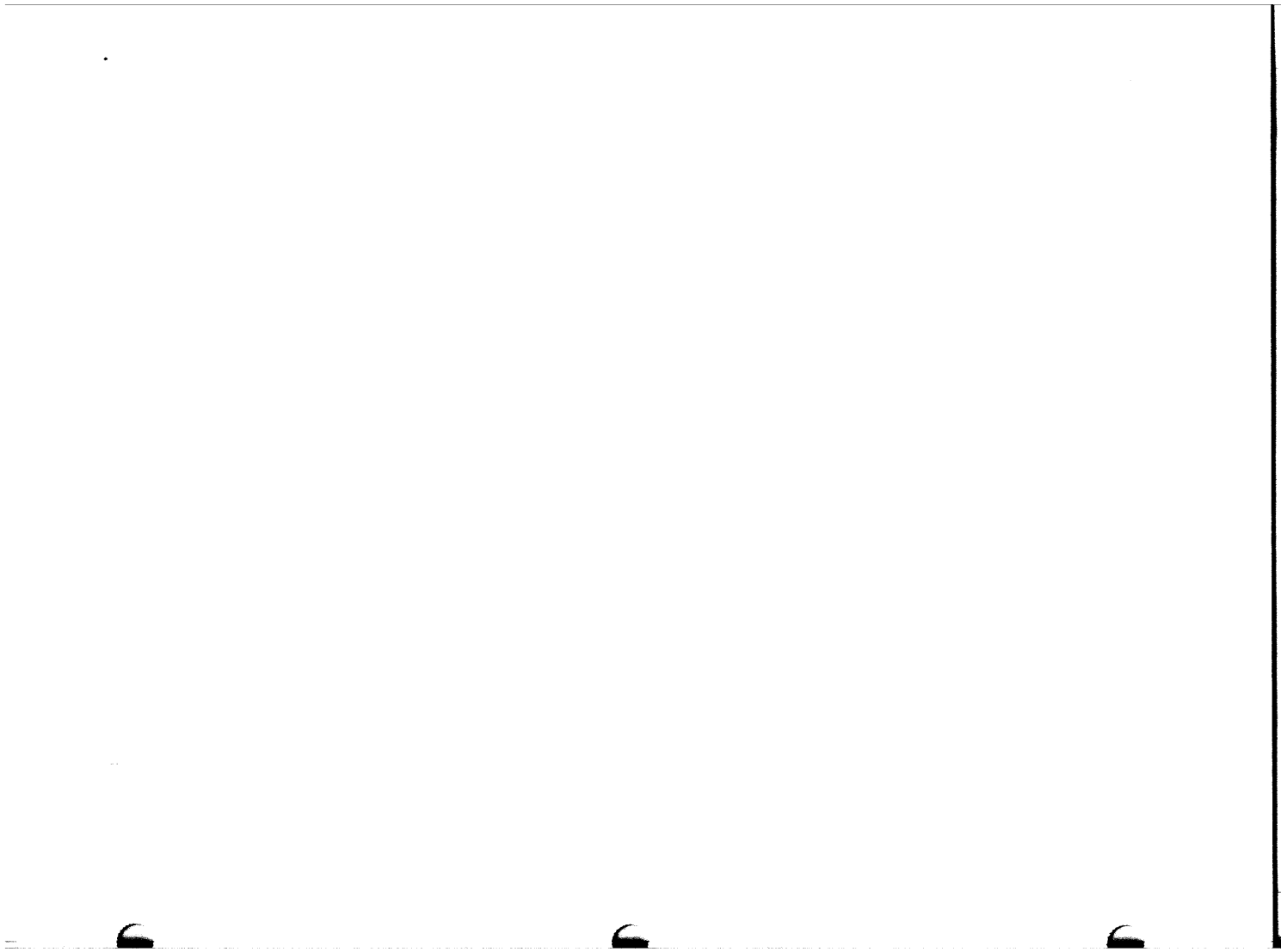
1	PC Board	100169
1	Manual	101540

BAG 5

2	8212	101071
2	24-pin socket	102105




PARALLEL I/O BD
INT ENABLE
STATUS



This places the status information onto the two status bit lines, DI0 and DI1. If DI0 is high, the output device is ready to recieve new data from the computer. If DI1 is high, the input device has sent data and the computer can now access it.

When an "OUT" instruction is followed by the even address of the board, the four gates of IC E in the interrupt control circuitry become partially enabled.

Data bits D00 and D01 are inverted then split and one signal inverted again. These four signals are fed into the remaining inputs of IC E. The outputs of IC E are fed through R-S flip-flops and some NOR gates to the vectored interrupt jumper lines.

The state of data bits D00 and D01 is used to determine which of the interrupt lines will be enabled. If D00 is high, the output device interrupt is enabled. If D01 is high, the input device interrupt is enabled. If the "BOTH" jumper is used, then either signal being high will cause an interrupt.

Data Channel

If the incoming address for the board is the odd address (A0 is high), IC D pin 13 will go high selecting the data channel.

When the signal on IC D pin 13 goes high IC H is partially enabled, along with one gate of IC N at pin 2. When the "SINP" signal goes high the IC H latch becomes completely enabled, and IC N pin 3 is enabled. The signal at IC N pin 3 enables the data buffers from latch H, placing the data on the bus lines DI0 through DI7.

For an output instruction, the odd address again partially enables IC G through IC D pin 13.

When the "OUT" instruction is executed the "SOUT" signal goes high, followed by "$\overline{\text{PWR}}$" going low. This enables IC D pin 1, which in turn completely enables IC G. This causes the data present on the bus to be latched into IC G.

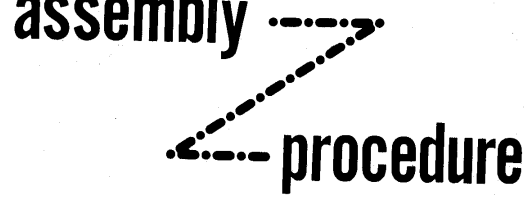
Interrupt

The pads "OUT", "IN" and "BOTH" may be jumpered to the pads VI0 through VI7 to provide hardware interrupt capability for the board. The first three pads represent the OUTput device, the INput device and BOTH devices. The pads VI0 through VI7 are the interrupt lines which connect to the Vectored Interrupt Board (88-VI), and the 0 to 7 portion corresponds to the 8 priority levels with 0 the lowest and 7 the highest priority.

The input device and the output device may each be assigned a different priority, or both devices may be assigned a single priority. If the 88-VI board is not in the system, one of the three pads, "OUT", "IN" or "BOTH", on one of the I/O boards may be jumpered to the CPU input interrupt line. (see assembly procedure)

The last method above will allow one level of interrupt to the CPU. When the interrupt occurs, the processor will immediately jump to the location 70 (octal) and begin execution. Place the interrupt service routine in locations 70 through 77 (octal).

PARALLEL I/O BOARD



8800 PARALLEL I/O BOARD ASSEMBLY

There are 16 integrated circuits (IC's) to be installed on the 8800 Parallel I/O Board (88-PIO). Two of these, IC's G & H, will be provided with 24-pin IC sockets.

NOTE: The 24-pin IC sockets may be one of two different types. One type will be a single solid piece, and should be installed in the same manner as the IC's. The other type is actually two pieces, joined by 4 cross pieces. To install this type, cut the 4 cross pieces away and install the two 12-pin sides separately.

(✓) Referring to the component layout, set the 24-pin IC socket for IC G into place on the silk-screened side of the board. Be sure it is straight, then tape it in place with a piece of masking tape.

(✓) Turn the board over and solder each pin to the foil pattern on the back side of the board. Be sure to solder each pin and be careful not to leave any solder bridges.

(✓) Turn the board over again and remove the piece of masking tape.

(✓) Install the socket for IC H in the same manner.

Install the IC's according to the following procedure.

(✓) Referring to the component layout, remove the IC with the correct part number from its holder. If there are any bent pins, straighten these using needle-nose pliers. Ensure that you choose the IC with the correct part number as you install each one.

(✓) Orient the IC so that its notched end corresponds with the notch printed on the PC board, and pin 1 of the IC corresponds with the pad marked with an arrowhead on the board.

NOTE: If the IC does not have a notch on one end, refer to the IC Orientation Chart included in your manual for the identification of pin 1.

(✓) When you have the correct orientation, start the pins on one side of the IC into their respective holes on the silk-screened side of the PC board. DO NOT PUSH THE PINS IN ALL THE WAY. If you have difficulty getting the pins into the holes, use the tip of a small screwdriver to guide them.

(✓) Start the pins on the other side of the IC into their holes in the same manner. When all of the pins have been started, set the IC in place by gently rocking it back and forth until it rests as close as possible to the board. Make sure that the IC is perfectly straight and as close as possible to the board; then tape it in place with a piece of masking tape.

(✓) Turn the board over and solder each pin to the foil pattern on the back side of the board. Be sure to solder each pin and be careful not to leave any solder bridges.

(✓) Turn the board over again and remove the piece of masking tape.

Use the same procedure to install each of the remaining IC's. Be sure you choose the IC with the correct part number as you install each one.

( ) IC's G & H are 8212's Install IC sockets for these two

(✓) IC P is a 7406

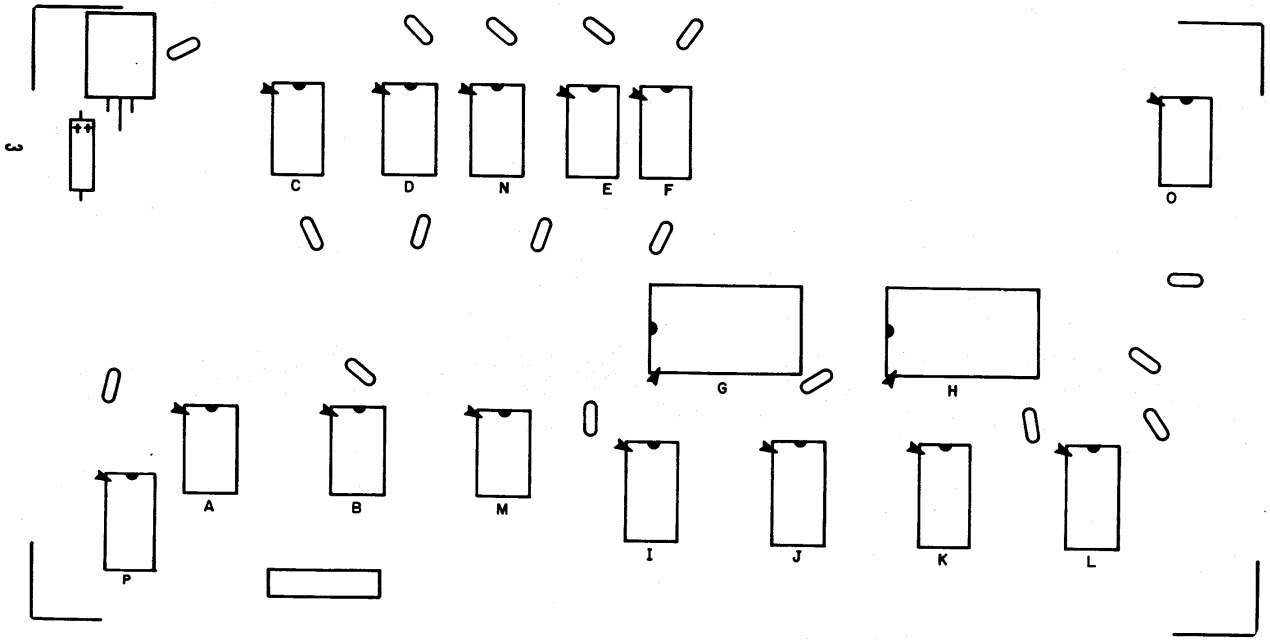
(✓) IC's A, B & M are 74L04's

(✓) IC C is a 74L30

(✓) IC's D & O are 74L02's

( ) IC's E, F & N are 74L00's

( ) IC's I, J, K & L are 8T97's



Resistor Installation

There are three resistors to be installed on the Parallel I/O Board which are not illustrated on the silk-screen.

NOTE: Resistors are color-coded according to their value. The resistors in your kit will have four or possibly five bands of color. The fourth band in both cases will be gold or silver, indicating the tolerance. In the following instructions we will be concerned only with the three bands of color to one side of the gold or silver band. Be sure to match these three bands of color with those called for in the instructions as you install each resistor.

Using needle-nose pliers, bend the leads of the following resistors at right angles to match their respective holes on the PC board.

There is a group of nine pads to the right of IC P and just below IC A. The three pads on the right are labeled "OUT", "IN" & "BOTH". There is another group of three pads just next to these three, and another group of three pads next to IC P. These three resistors are to be installed between the two groups of pads to the left of the first group labeled as stated above. They should be parallel with the bottom of the board when installed correctly.

(✓) These three resistors are each 1K-ohm (brown-black-red), either 1/4 or 1/2 Watt.

(✓) Install all three by placing them into the correct holes on the silk-screened side of the board and soldering them in place on the back side.

(✓) Clip off any excess lead lengths.

PARALLEL I/O BOARD ERRATA

THE FOLLOWING APPLIES TO PAGES 5 & 6 OF THE ASSEMBLY SECTION OF THE PARALLEL I/O BOARD DOCUMENTATION.

CERAMIC DISK CAPACITOR C1 WILL NOT FIT ONTO THE BOARD AS SHOWN IN THE COMPONENT LAYOUT. THE HOLE FOR THE LEAD CLOSEST TO THE VOLTAGE REGULATOR IS UNDERNEATH WHERE THE HEAT SINK WILL BE MOUNTED.

SIMPLY TWIST THE CAPACITOR AROUND, AWAY FROM THE HEAT SINK. THE LEAD NORMALLY FURTHEST FROM THE REGULATOR SHOULD REMAIN IN ITS NORMAL POSITION. THE LEAD THAT WOULD BE UNDERNEATH THE HEAT SINK SHOULD BE SOLDERED DIRECTLY TO THE GROUND LAND WHICH RUNS ALONG THE TOP OF THE BOARD. THIS MAY BE CHECKED BY SETTING THE HEAT SINK IN PLACE AND CHECKING TO SEE THAT IT CLEARS THE CAPACITOR.

Capacitor Installation

There are 17 ceramic disk capacitors and 1 electrolytic capacitor to be installed on the 8800 Parallel I/O Board.

Refer to the component layout and install the ceramic disk capacitors according to the following procedure.

( ) Choose the capacitor with the correct value as called for in the instructions. Straighten the two leads as necessary and bend them to fit their respective holes on the PC board.

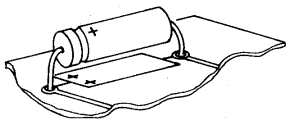
(✓) Insert the capacitor into the correct holes from the silk-screened side of the board. Push the capacitor down until the ceramic insulation almost touches the foil pattern.

( ) Holding the capacitor in place, turn the board over and bend the two leads slightly outward.

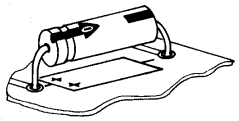
( ) Solder the two leads to the foil pattern on the back side of the board; then clip off any excess lead lengths. Save the excess lead lengths for later use in the address selection wiring.

Install all of the ceramic disk capacitors in this manner. Be sure that you have the correct value capacitor as you install each one.

The electrolytic capacitor for the Parallel I/O Board has polarity requirements which must be noted before installation. Those contained in your kit may have one or possibly two of three types of polarity markings. To determine the correct orientation, look for the following: (see drawing above right)



ELECTROLYTIC CAPACITOR



One type will have plus (+) signs on the positive end; another will have a band or a groove around the positive side in addition to the plus signs. The third type will have an arrow on it; in the tip of the arrow there is a negative (-) sign and the capacitor must be oriented so the arrow points to the negative polarity side.

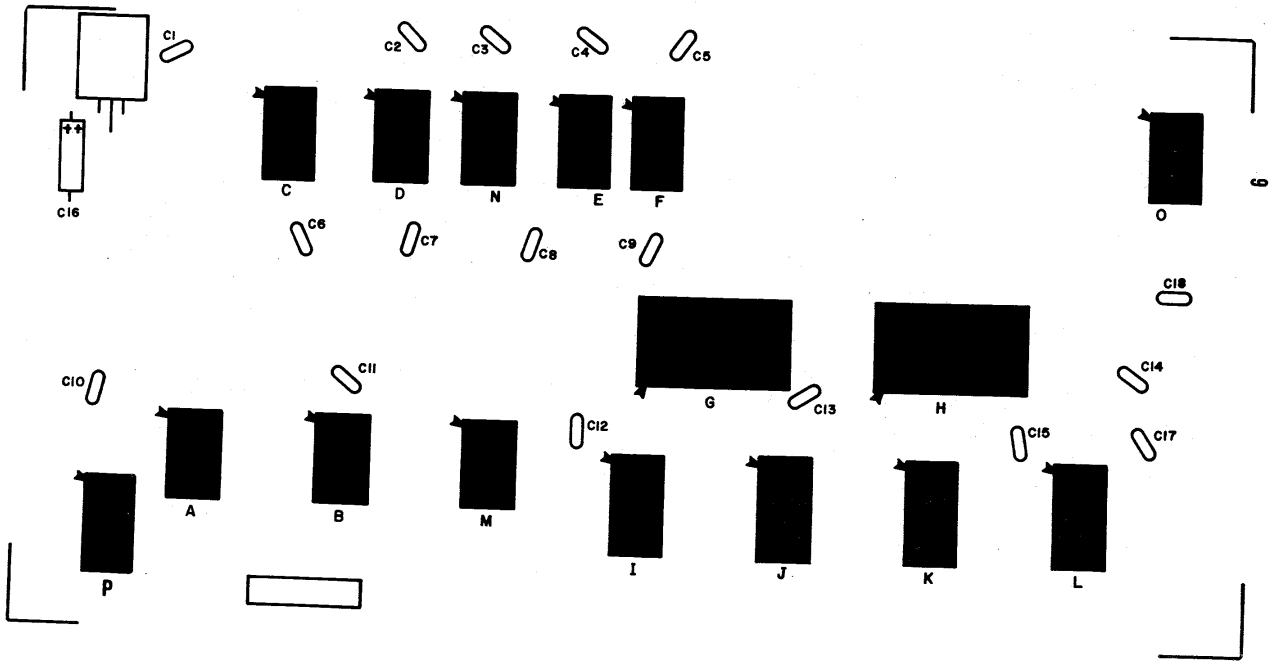
Referring to the component layout, install the electrolytic capacitor onto the board.

(✓) Bend the two leads of the capacitor with the correct value at right angles to match their respective holes on the board. Insert the capacitor into the holes on the silk-screened side of the board. Be sure to align the positive polarity side with the "+" signs printed on the board.

( ) Holding the capacitor in place, turn the board over and bend the two leads slightly outward. Solder the leads to the foil pattern and clip off any excess lead lengths.

(✓) C1 through C15 and C17 & C18 are .1uf disks

(✓) C16 is a 35uf electrolytic



Voltage Regulator Installation

There is one MC7805 5-volt regulator to be installed on the 8800 Parallel I/O Board.

(✓) Set the MC7805 in place on the board and align the mounting holes. (see drawing)

(✓) Use a pencil to mark the point on each of the three leads where they line up with their respective holes on the board.

(✓) Use needle-nose pliers to bend each of the three leads at a right angle on the points where you made the pencil marks.

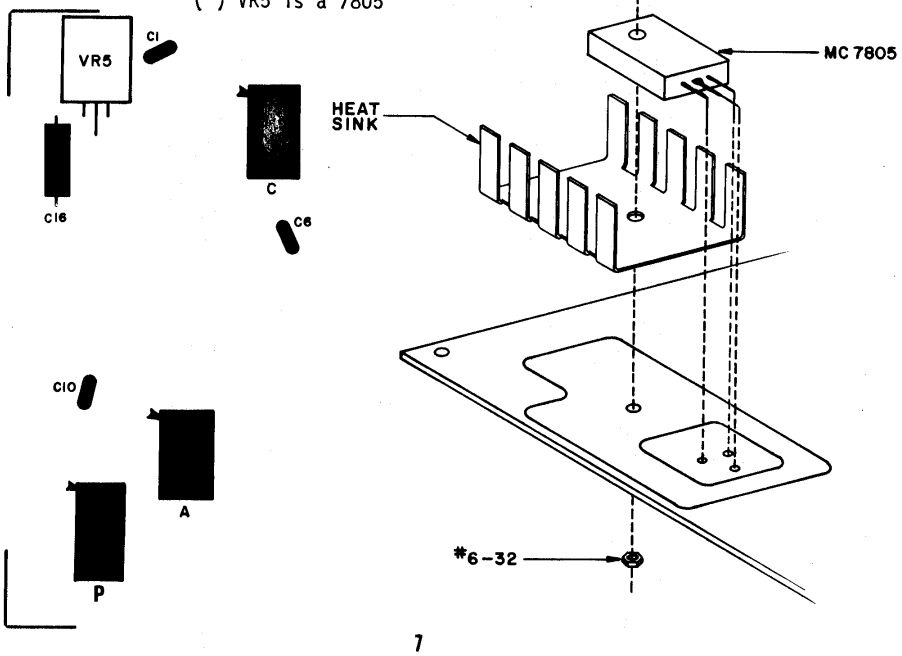
NOTE: Use heat-sink grease when installing this component. Apply the grease to all surfaces which come in contact with each other.

(✓) Referring to the drawing, set the regulator and heat sink in place on the silk-screened side of the board. Use the smaller, 6 pronged, heat sink instead of the 8 pronged one shown in the drawing. Secure them as shown, holding the regulator in place as you tighten the nut.

(✓) Turn the board over and solder the three leads to the foil pattern on the back side of the board. Be sure not to leave any solder bridges.

(✓) Clip off any excess lead lengths.

( ) VR5 is a 7805



Hardwire Connections

There are seven address selection jumpers and one or two optional interrupt jumpers to be connected on the 8800 Paralled I/O Board.

The connections for the address selection should be made with the component leads saved earlier in the assembly procedure.

Address Selection

(✓) Connect pads I1 through I7 to pads A1 or $\overline{A1}$ through A7 or $\overline{A7}$ according to the information in the I/O Address Selection Chart to obtain the octal address listed in the left column.

(✓) Bend the leads as necessary and insert them into the correct holes from the silk-screened side of the board.

(✓) Turn the board over and solder the leads to the foil pattern on the back side of the board; then clip off any excess lengths.

Refer to the Theory of Operation section for further explanation of this function.

Vectored Interrupt

This is an optional function on the 8800 system, and need not be used at all. If it is to be used, it must be used in conjunction with the 88-VI vectored interrupt card. There is one exception to this which will be explained towards the end of this section.

The 8800 Parallel I/O Board has provisions for vectored interrupt hardwire connections. This provides the user with the option of selecting a priority level for the input device and the output device, or a single priority level for both.

The vectored interrupt offers 8 levels of priority, 0 through 7, with 7 being the highest priority level.

There are three pads to the right of IC P that are labeled "OUT", "IN" and "BH". There are eight pads at the bottom of the board labeled "VI" and numbered "0" through "7". The eight numbered pads correspond to the eight priority levels respectively.

Cut wires to length and make these connections in the same manner as the address selection jumper connections.

You may connect the "OUT" (output device) pad to some priority level, and the "IN" (input device) pad to some priority level; or you may connect the "BH" (both devices) pad to a desired priority level for both devices. If the "BH" pad is used to set the priority level, the "OUT" and "IN" pads should not be used.

(✓) Connect the vectored interrupt priority level as desired per the information above.

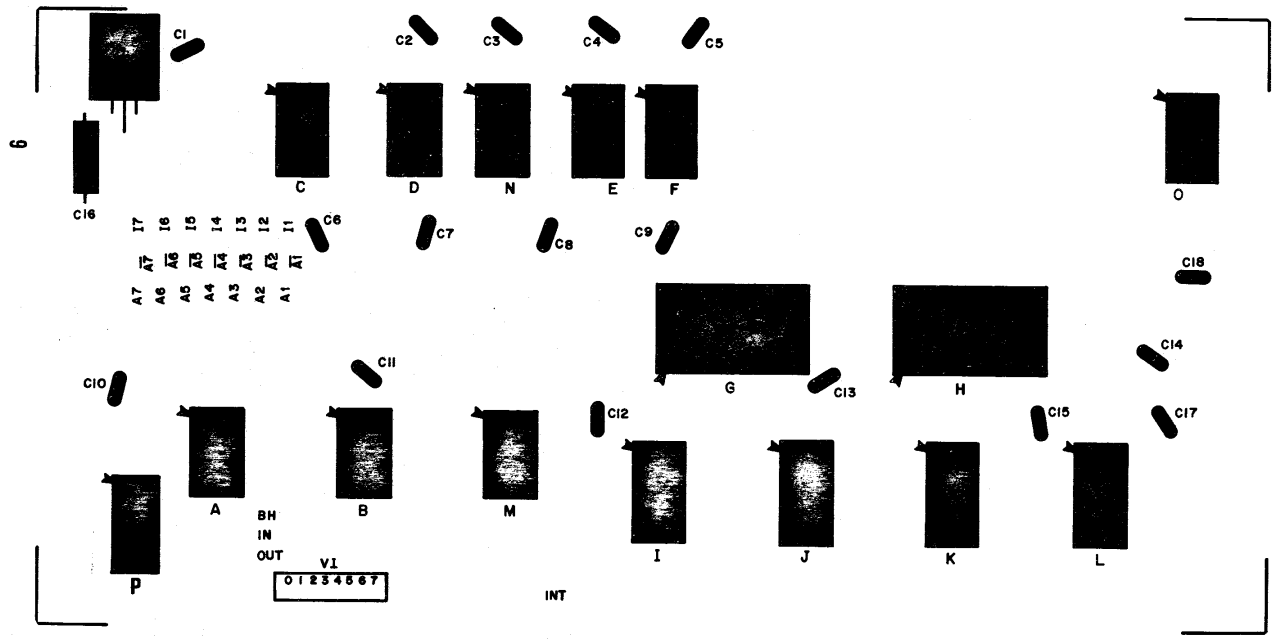
It is possible to obtain a single level of interrupt priority on this board without the necessity of the 88-VI vectored interrupt card.

This may be used only on one of the I/O cards in your system, and only one of the three pads ("OUT", "IN" or "BH") can be used to make the connection.

(✓) Connect the pad near the bottom of the board labeled "INT" to one of the three pads mentioned above to obtain a single level of interrupt priority.

Remember, only one of the 3 pads "OUT", "IN" or "BH" may be used and only one I/O board may be connected in this manner.

Make all hardwire connections as instructed.

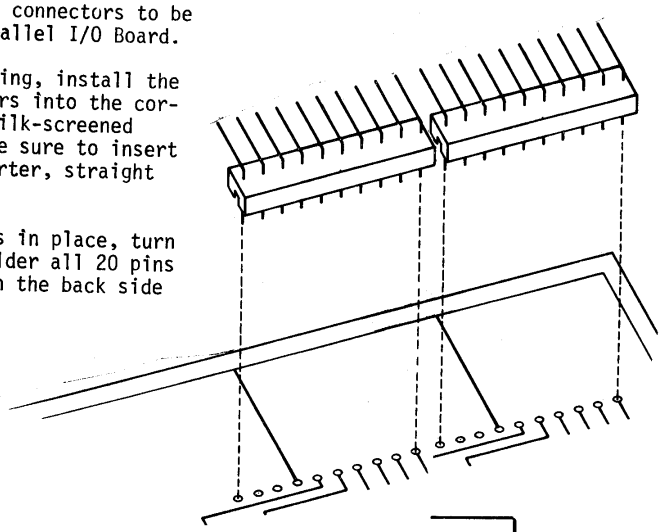


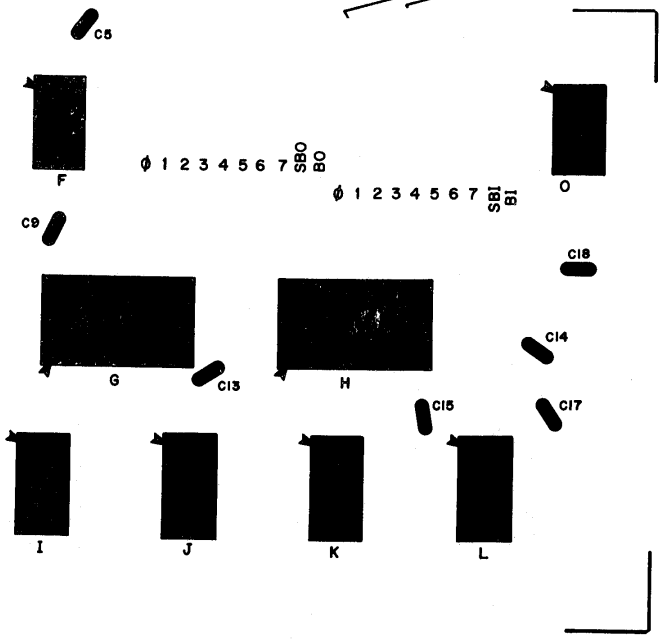
Wafer Connector Installation

There are two 10-pin male connectors to be installed on the 8800 Parallel I/O Board.

(✓) Referring to the drawing, install the 10-pin wafer connectors into the correct holes from the silk-screened side of the board. Be sure to insert the side with the shorter, straight pins.

(✓) Holding the connectors in place, turn the board over and solder all 20 pins to the foil pattern on the back side of the board.





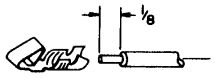
I/O Connector Wiring

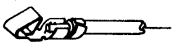
There are two 10-pin female connectors provided with your kit, along with a 20 inch length of 25-conductor cable. The three must be wired together according to the following procedure.

(✓) Using a small sharp knife, strip 2 1/2 inches of cable sheath from one end of the 25-conductor cable. Do this by cutting a circle around the sheath 2 1/2 inches from the end, being very careful not to cut into the insulation on the wires inside. Then simply pull the end of the sheath off of the cable.

(✓) Strip 1/8 inch of insulation from the end of each of the 25 wires now exposed, and tin the uninsulated portion by applying a thin coat of solder.

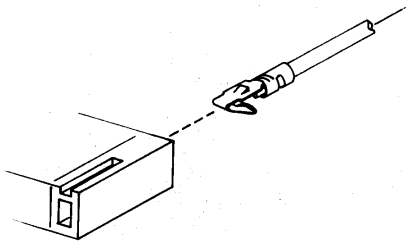
(✓) Referring to the drawing below, install one of the connector pins onto the end of each of 20 of the 25 wires. Do this by crimping the wire into place; then soldering the end to the pin itself.





(✓) Referring to the drawing below, insert the pins just connected into the female connectors. Install 10 of the pins into each connector.

(✓) There will now be 5 wires left over. Four of these will not be used and may be cut off at the cable sheath. The fifth wire will be used later for a ground connection.

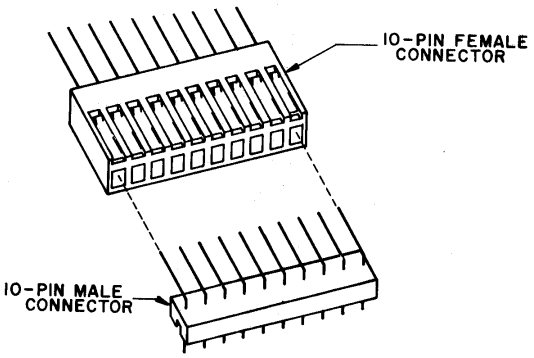


Final Assembly

(✓) IC's G & H (8212's) may now be installed into the sockets installed earlier for this purpose. Be sure to maintain the correct orientation and be careful not to bend any of the pins underneath the IC's when installing them.

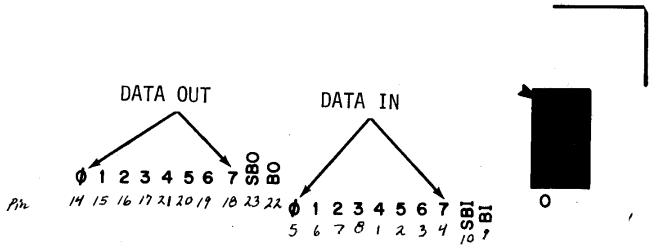
( ) The two 10-pin female connectors should now be installed onto the male connectors previously installed on the board. Install them with the orientation shown in the drawing on the right.

( ) There is a ground land running along the top edge of the board with several plated-through holes in it. The extra wire from the cable should be inserted into one of these holes closest to the connectors, and soldered into place.



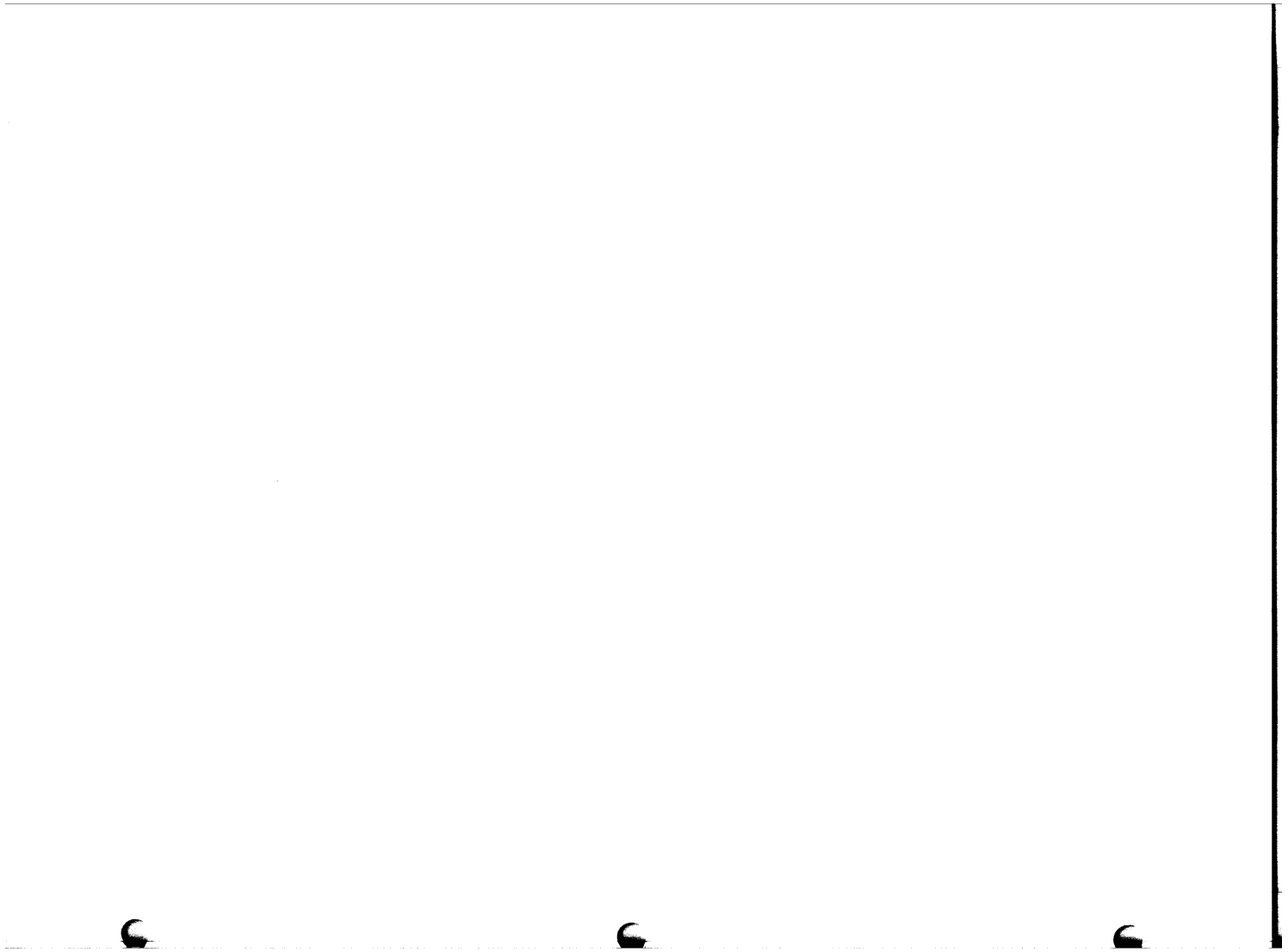
The silk-screen illustration below shows the signal designations for interfacing the board to some I/O device. By noting the color of the wire attached to a specific pin, the signal wire can be correctly determined on the opposite end of the cable. The connections to the device should be made according to the device specifications. For further information on these signals refer to the Theory of Operation section of this manual.

There are spaces provided on the 8800 Back Panel for mounting 25-pin connectors. Both male and female connectors are available from MITS upon order. The connectors are also to be wired according to the device specifications.



PIN CONNECTIONS BETWEEN VLCT AND PARALLEL I/O

1	DI4
2	DI5
3	DI6
4	DI7
5	DI0
6	DI1
7	DI2
8	DI3
9	BI (reset)
10	SBI (ready)
11	---
12	----
13	Gnd
14	DO0
15	do1
16	DO2
17	DO3
18	DO7
19	DO6
20	DO5
21	DO4
22	BO (data ready)
23	SBO (ready key)
24	---
25	Busy (not connected)



I/O ADDRESS SELECTION CHART

ADDRESS OCTAL	CONNECTIONS I7	I6	I5	I4	I3	I2	I1
000	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$
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004	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	A2	$\overline{A1}$
006	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	A2	A1
010	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	A3	$\overline{A2}$	$\overline{A1}$
012	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	A3	$\overline{A2}$	A1
014	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	A3	A2	$\overline{A1}$
016	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	A3	A2	A1
020	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	A4	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$
022	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	A4	$\overline{A3}$	$\overline{A2}$	A1
024	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	A4	$\overline{A3}$	A2	$\overline{A1}$
026	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	A4	$\overline{A3}$	A2	A1
030	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	A4	A3	$\overline{A2}$	$\overline{A1}$
032	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	A4	A3	$\overline{A2}$	A1
034	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	A4	A3	A2	$\overline{A1}$
036	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	A4	A3	A2	A1
040	$\overline{A7}$	$\overline{A6}$	A5	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$
042	$\overline{A7}$	$\overline{A6}$	A5	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	A1
044	$\overline{A7}$	$\overline{A6}$	A5	$\overline{A4}$	$\overline{A3}$	A2	$\overline{A1}$
046	$\overline{A7}$	$\overline{A6}$	A5	$\overline{A4}$	$\overline{A3}$	A2	A1
050	$\overline{A7}$	$\overline{A6}$	A5	$\overline{A4}$	A3	$\overline{A2}$	$\overline{A1}$
052	$\overline{A7}$	$\overline{A6}$	A5	$\overline{A4}$	A3	$\overline{A2}$	A1
054	$\overline{A7}$	$\overline{A6}$	A5	$\overline{A4}$	A3	A2	$\overline{A1}$
056	$\overline{A7}$	$\overline{A6}$	A5	$\overline{A4}$	A3	A2	A1
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ADDRESS OCTAL	CONNECTIONS I7	I6	I5	I4	I3	I2	I1
062	$\overline{A7}$	$\overline{A6}$	A5	A4	$\overline{A3}$	$\overline{A2}$	A1
064	$\overline{A7}$	$\overline{A6}$	A5	A4	$\overline{A3}$	A2	$\overline{A1}$
066	$\overline{A7}$	$\overline{A6}$	A5	A4	$\overline{A3}$	A2	A1
070	$\overline{A7}$	$\overline{A6}$	A5	A4	A3	$\overline{A2}$	$\overline{A1}$
072	$\overline{A7}$	$\overline{A6}$	A5	A4	A3	$\overline{A2}$	A1
074	$\overline{A7}$	$\overline{A6}$	A5	A4	A3	A2	$\overline{A1}$
076	$\overline{A7}$	$\overline{A6}$	A5	A4	A3	A2	A1
100	$\overline{A7}$	A6	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$
102	$\overline{A7}$	A6	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	A1
104	$\overline{A7}$	A6	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	A2	$\overline{A1}$
106	$\overline{A7}$	A6	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	A2	A1
110	$\overline{A7}$	A6	$\overline{A5}$	$\overline{A4}$	A3	$\overline{A2}$	$\overline{A1}$
112	$\overline{A7}$	A6	$\overline{A5}$	$\overline{A4}$	A3	$\overline{A2}$	A1
114	$\overline{A7}$	A6	$\overline{A5}$	$\overline{A4}$	A3	A2	$\overline{A1}$
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120	$\overline{A7}$	A6	$\overline{A5}$	A4	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$
122	$\overline{A7}$	A6	$\overline{A5}$	A4	$\overline{A3}$	$\overline{A2}$	A1
124	$\overline{A7}$	A6	$\overline{A5}$	A4	$\overline{A3}$	A2	$\overline{A1}$
126	$\overline{A7}$	A6	$\overline{A5}$	A4	$\overline{A3}$	A2	A1
130	$\overline{A7}$	A6	$\overline{A5}$	A4	A3	$\overline{A2}$	$\overline{A1}$
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140	$\overline{A7}$	A6	A5	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$
142	$\overline{A7}$	A6	A5	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	A1

ADDRESS OCTAL	CONNECTIONS I7	I6	I5	I4	I3	I2	I1
144	$\overline{A7}$	A6	A5	$\overline{A4}$	$\overline{A3}$	A2	$\overline{A1}$
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150	$\overline{A7}$	A6	A5	$\overline{A4}$	A3	$\overline{A2}$	$\overline{A1}$
152	$\overline{A7}$	A6	A5	$\overline{A4}$	A3	$\overline{A2}$	A1
154	$\overline{A7}$	A6	A5	$\overline{A4}$	A3	A2	$\overline{A1}$
156	$\overline{A7}$	A6	A5	$\overline{A4}$	A3	A2	A1
160	$\overline{A7}$	A6	A5	A4	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$
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170	$\overline{A7}$	A6	A5	A4	A3	$\overline{A2}$	$\overline{A1}$
172	$\overline{A7}$	A6	A5	A4	A3	$\overline{A2}$	A1
174	$\overline{A7}$	A6	A5	A4	A3	A2	$\overline{A1}$
176	$\overline{A7}$	A6	A5	A4	A3	A2	A1
200	A7	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$
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ADDRESS OCTAL	CONNECTIONS I7	I6	I5	I4	I3	I2	I1
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230	A7	$\overline{A6}$	$\overline{A5}$	A4	A3	$\overline{A2}$	$\overline{A1}$
232	A7	$\overline{A6}$	$\overline{A5}$	A4	A3	$\overline{A2}$	A1
234	A7	$\overline{A6}$	$\overline{A5}$	A4	A3	A2	$\overline{A1}$
236	A7	$\overline{A6}$	$\overline{A5}$	A4	A3	A2	A1
240	A7	$\overline{A6}$	A5	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$
242	A7	$\overline{A6}$	A5	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	A1
244	A7	$\overline{A6}$	A5	$\overline{A4}$	$\overline{A3}$	A2	$\overline{A1}$
246	A7	$\overline{A6}$	A5	$\overline{A4}$	$\overline{A3}$	A2	A1
250	A7	$\overline{A6}$	A5	$\overline{A4}$	A3	$\overline{A2}$	$\overline{A1}$
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254	A7	$\overline{A6}$	A5	$\overline{A4}$	A3	A2	$\overline{A1}$
256	A7	$\overline{A6}$	A5	$\overline{A4}$	A3	A2	A1
260	A7	$\overline{A6}$	A5	A4	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$
262	A7	$\overline{A6}$	A5	A4	$\overline{A3}$	$\overline{A2}$	A1
264	A7	$\overline{A6}$	A5	A4	$\overline{A3}$	A2	$\overline{A1}$
266	A7	$\overline{A6}$	A5	A4	$\overline{A3}$	A2	A1
270	A7	$\overline{A6}$	A5	A4	A3	$\overline{A2}$	$\overline{A1}$
272	A7	$\overline{A6}$	A5	A4	A3	$\overline{A2}$	A1
274	A7	$\overline{A6}$	A5	A4	A3	A2	$\overline{A1}$
276	A7	$\overline{A6}$	A5	A4	A3	A2	A1
300	A7	A6	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$
302	A7	A6	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	A1
304	A7	A6	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	A2	$\overline{A1}$
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ADDRESS OCTAL	CONNECTIONS I7	I6	I5	I4	I3	I2	I1
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312	A7	A6	$\overline{A5}$	$\overline{A4}$	A3	$\overline{A2}$	A1
314	A7	A6	$\overline{A5}$	$\overline{A4}$	A3	A2	$\overline{A1}$
316	A7	A6	$\overline{A5}$	$\overline{A4}$	A3	A2	A1
320	A7	A6	$\overline{A5}$	A4	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$
322	A7	A6	$\overline{A5}$	A4	$\overline{A3}$	$\overline{A2}$	A1
324	A7	A6	$\overline{A5}$	A4	$\overline{A3}$	A2	$\overline{A1}$
326	A7	A6	$\overline{A5}$	A4	$\overline{A3}$	A2	A1
330	A7	A6	$\overline{A5}$	A4	A3	$\overline{A2}$	$\overline{A1}$
332	A7	A6	$\overline{A5}$	A4	A3	$\overline{A2}$	A1
334	A7	A6	$\overline{A5}$	A4	A3	A2	$\overline{A1}$
336	A7	A6	$\overline{A5}$	A4	A3	A2	A1
340	A7	A6	A5	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$
342	A7	A6	A5	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	A1
344	A7	A6	A5	$\overline{A4}$	$\overline{A3}$	A2	$\overline{A1}$
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350	A7	A6	A5	$\overline{A4}$	A3	$\overline{A2}$	$\overline{A1}$
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360	A7	A6	A5	A4	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$
362	A7	A6	A5	A4	$\overline{A3}$	$\overline{A2}$	A1
364	A7	A6	A5	A4	$\overline{A3}$	A2	$\overline{A1}$
366	A7	A6	A5	A4	$\overline{A3}$	A2	A1
370	A7	A6	A5	A4	A3	$\overline{A2}$	$\overline{A1}$

ADDRESS OCTAL	CONNECTIONS I7	I6	I5	I4	I3	I2	I1
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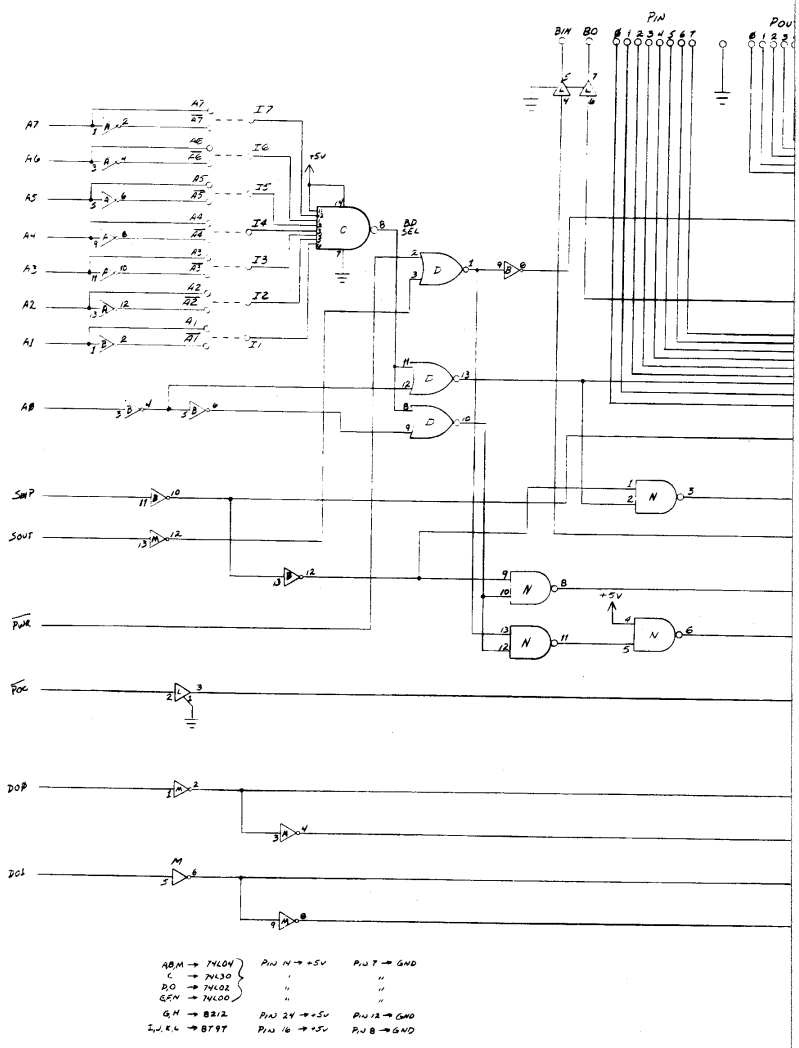
376	A7	A6	A5	A4	A3	A2	A1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SOUT
PWR
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DO1
+5V
BD SEL
I7
I6
I5
I4
I3
I2
I1
C
D
N
M
A0,M → 74LO4
C → 74L30
D,O → 74L02
GEN → 74L00
G,M → 8212
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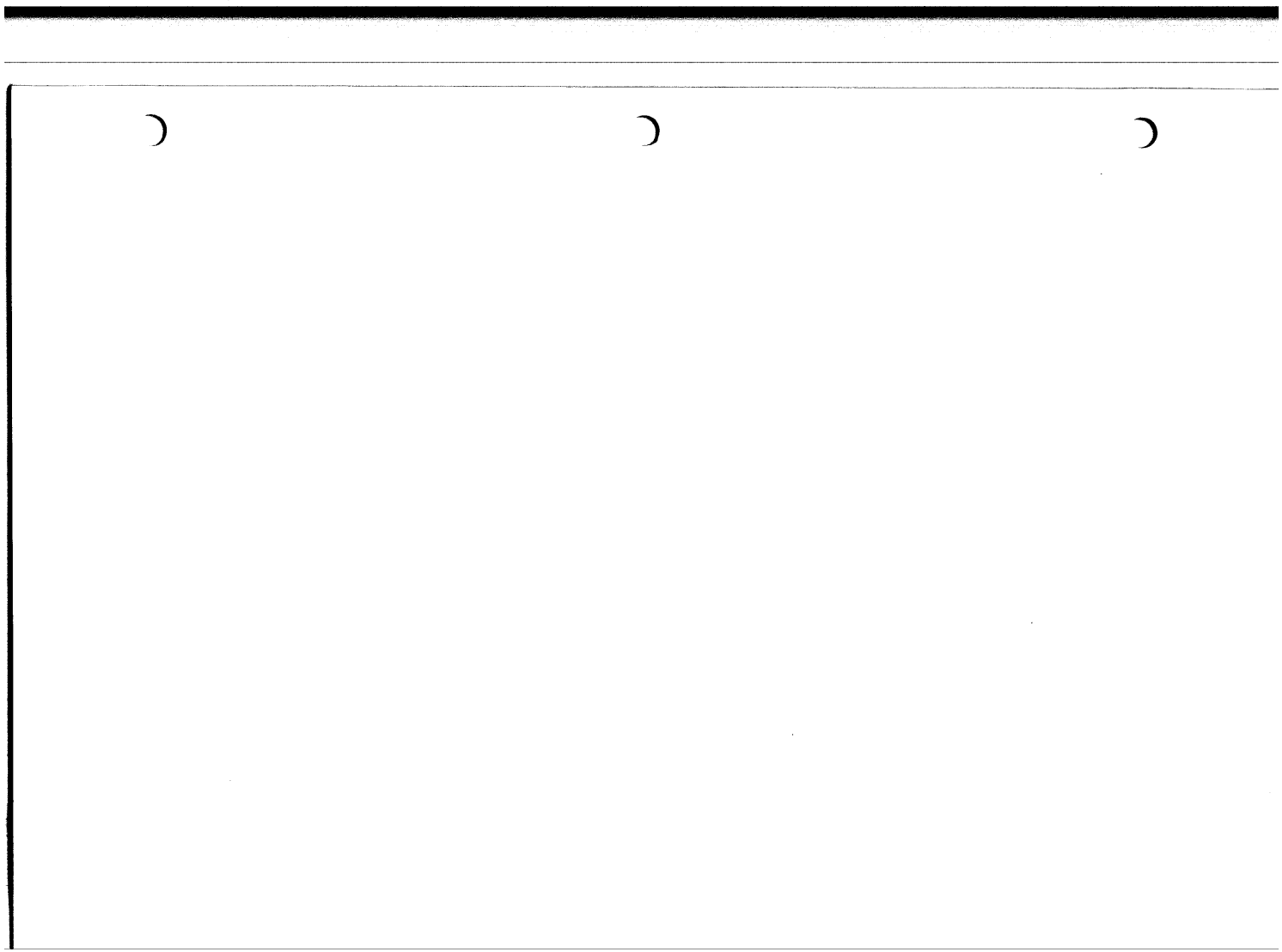

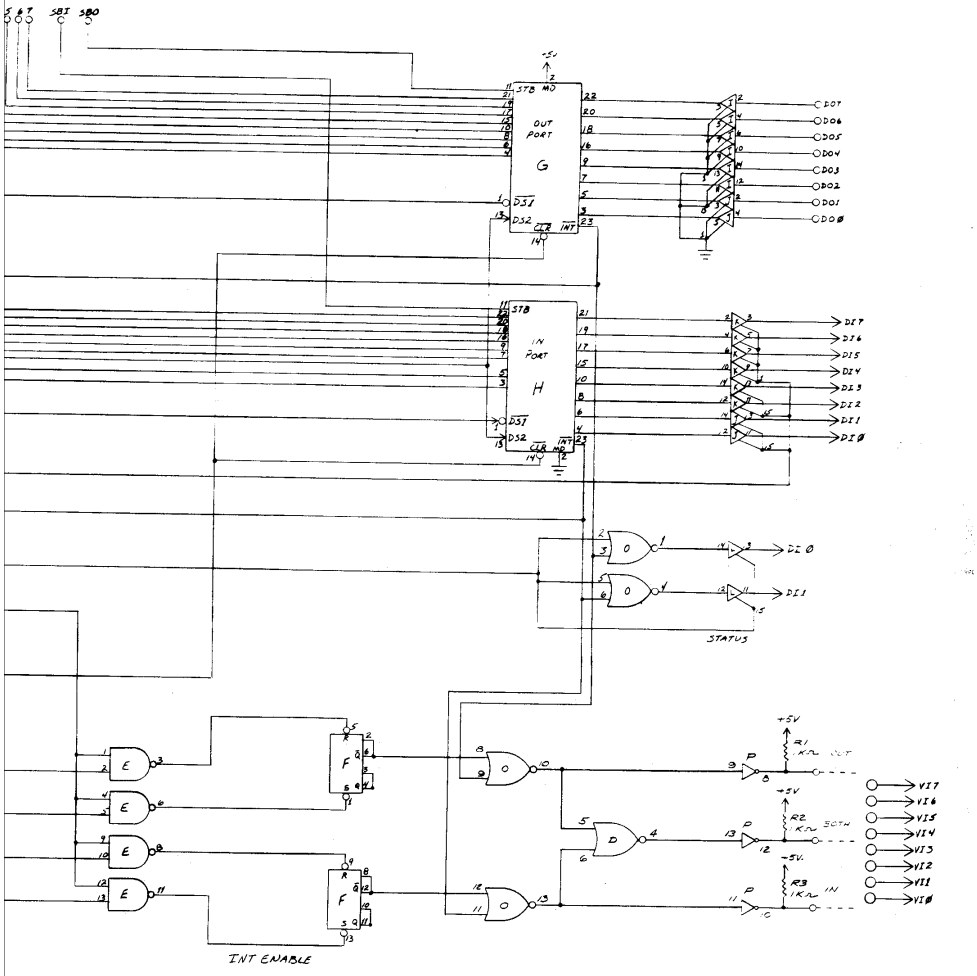

PARALLEL I/O BD