NorthStarComputersInc
2547 Ninth Street
Berkeley, Ca. 94710

North Star
Z80 Processor Board ZPB-A

25006
ZPB-DOC
Revision 3

This manual was digitally remastered by Howard M. Harte, June 2003.

http://www.hartetec.com

If you find any errors, or can supply clearer scans of the schematics, please email hharte@hartetec.com.

North Star

Z80A PROCESSOR BOARD ZPB-A

Contents

REVISION 3

CAUTIONS

1. Correct this document from the errata sheets, if any, before doing anything else.

2. Building this product from a kit is a complex, demanding project. It should not be attempted without prior kit building experience.

3. Do NOT insert or remove the ZPB from the computer while the power is turned on. Note that the power is not completely off until the capacitors have discharged, several seconds after turning of the power switch.

4. Do NOT insert or remove IC's from the board while the power is turned on.

5. Be sure each 5 volt regulator is generating 5 volt output voltage before installing any IC's.

6. Be careful to insert all IC's in correct positions and with correct orientation. Be sure all IC pins are correctly inserted into the socket holes and are not bent under the IC and are not outside the socket.

7. Carefully observe the anti-static handling procedure for the static sensitive devices (these are the Z80A and the 2708 PROM in the PROM option). The procedure is described in the Assembly Information section of this manual.

INTRODUCTION

The North Star Computers Z80A Processor Board (ZPB) provides Z80 microprocessor capability on the S-100 bus. The use of the Z80A chip allows full speed 4MHz operation as a standard feature. The ZPB can be used in any standard S-100 bus computer and will operate in conjunction with nearly all other S-100 bus boards. However, the ZPB has been specifically designed to integrate into the North Star Computers HORIZON computer system. In addition to the Z80A microprocessor and support logic to interface to the standard S-100 bus, the ZPB contains the following features and options:

1. AUTO-JUMP feature that will cause an automatic jump to any address at power-on or reset.

2. VECTORED INTERRUPTS. ZPB logic will respond to eight levels of interrupt requests, determine the highest priority request pending and generate the appropriate RST instruction. The logic may be disabled to allow the function to be performed on another board.

3. FRONT PANEL INTERFACE for direct connection to IMSAI and other similar front panels.

4. ADDRESS MIRROR feature to simulate the input/output characteristics of the 8080 microprocessor. This feature maintains compatibility with some S-100 bus peripheral boards. Address mirroring may be disabled to allow use of the more powerful Z80 protocol.

5. PROM OPTION. 1K of 2708 type erasable PROM can be added to the ZPB. This allows configuration of systems that require resident monitor and bootstrap programs.

If you have purchased the ZPB as a kit, first skim this entire manual. Before beginning assembly, carefully read the Assembly Information section.

Whether you purchased the ZPB as a kit or assembled, read the Configuration section before attempting to use the ZPB. Note that a Z80 Technical Manual has been included to fully describe the operation of the Z80A.

LIMITED WARRANTY

North Star Computers, Inc. warrants the electrical and mechanical parts. and workmanship of this product to be free of defects for a period of 90 days from date of purchase. If such defects occur, North Star Computers, Inc. will repair the defect at no cost to the purchaser. This warranty does not extend to defects resulting from improper use or assembly by purchaser, nor does it cover transportation to the factory. Also, the warranty is invalid if all instructions included in the accompanying documentation are not carefully followed. Should 'a unit returned for warranty repair be deemed by North Star Computers, Inc. to be defective due to purchaser's action, then a repair charge not to exceed $30 without purchaser's consent will be assessed. ANY UNIT OR PART RETURNED FOR WARRANTY REPAIR MUST BE ACCOMPANIED BY A COPY OF THE ORIGINAL SALES RECEIPT. This warranty applies to units located outside the United States of America only if all costs and arrangements for transportation of the product to and from the factory are borne entirely by the customer. This warranty is made in lieu of all other warranties, expressed or implied, and is limited to the repair or replacement of the product. No warranty, expressed or implied, is extended concerning the completeness, correctness, or suitability of the North Star equipment for any particular application. There are no warranties which extend beyond those expressly stated herein.

OUT OF WARRANTY REPAIR

If your unit is out of warranty and you are unsuccessful at diagnosing or repairing the problem, out-of-warranty service may be arranged with a local dealer or other experienced local computer technician. Alternatively, any North Star products may be shipped PREPAID to the North Star address with a clear written description of the problem. Include as many details as possible about the problem and about your system configuration. Your unit will be returned, C.O.D., within 30 days after receipt by North Star. Out-of-warranty repair service is billed at the rate of $25.00 per hour. If you wish to place an upper limit on the amount of time spent on your unit, mention this in the written description.

ZPB-A PARTS LIST

1	ZPB Manual
1	Z80 Technical Manual
1	ZPB printed circuit board, 5" x 10"
1	40-pin IC socket
7	20-pin IC sockets
14	16-pin IC sockets
14	14-pin IC sockets
1	16-pin DIP header
1	1N4148 diode
2	5 volt regulators, 7805 or 340T-5
2	heat sinks, 6107E-14
1	crystal, 8MHz
2	6-32x3/8" machine screws
2	#6 lock washers
2	6-32 nuts

Integrated Circuits

3	74LS00	1	74LS132
2	74LS02	1	74LS148
1	74LS03	3	74LS175
2	74LS04	7	74LS241
7	74LS08	2	74LS257
1	74LS14	1	7404
1	74LS32	3	74367
1	74LS74	1	8T97
1	74LS75	1	Z80A

Resistors

1	100 ohm	(brown-black-brown)
1	330 ohm	(orange-orange-brown)
2	470 ohm	(yellow violet-brown)
11	1K ohm	(brown-black-red)
1	10K ohm	(brown-black-orange)
4	1K ohm networks, Part No. 10-9-1-R1K	
1	2.2K ohm network, Part No. 10-9-1-R2.2K	

Capacitors

1	33pf	Dipped mica (may be marked "330J03")
1	470pf	Dipped mica
19	.047uf	ceramic disc
2	6.8uf	Dipped tantalum
1	39uf	Dipped tantalum
1	100uf	Electrolytic

PROM OPTION PARTS LIST

74LS136 IC
2708 EPROM
+12 volt regulator, 78L12
-5 volt regulator, 79L05
24-pin IC socket
14-pin IC sockets
14-pin DIP header
1K resistor (brown-black-red)
3.9K resistor (orange-white-red)
3.9K resistor network, Part No. 10-9-1-R3.9K
2.2uf dipped tantalum capacitors

ASSEMBLY INFORMATION

Read completely through each section before beginning the first instruction step of that section. Perform all operations in the sequence indicated. Read each step entirely, including any notes that accompany the step, before beginning to follow the step.

WORK AREA AND TOOLS

Start with a clean, well-lit and well-ventilated area to work. The area should be large enough to accommodate the kit, tools. parts and assembly instructions. Suggested tools are: screwdrivers, needle-nose pliers, diagonal cutters, soldering iron, solder, and masking tape. A number of tests will require using a VOM (ohmmeter-voltmeter) or VTVM Also highly desirable, but not necessary, are an IC inserter, a screw-holding screwdriver, an oscilloscope or logic probe, and an extender card. [Note that if you do not have an oscilloscope or logic probe, waveforms can be detected by one of the procedures described in Appendix 1.]

SOLDERING TIPS

For best results use a 15 to 25 watt soldering iron or an iron with a temperature controlled tip (approximately 700 degrees). The tip should be no wider than the solder pads on the printed circuit board. Use only a fine gauge rosin core solder (60/40 or 63/37). Do NOT use acid core solder as this can severely damage a printed circuit board. When soldering, keep the soldering iron tip on the pad just long enough for the solder to completely flow. If the solder does not draw up the wire then more solder is required. Do not use so much solder that it overflows the pad. If a solidified joint is not shiny. it may be a cold solder joint and should be re-melted. The soldering iron tip should be cleaned frequently by wiping on a damp sponge

When you have completed assembly of a board, inspect it for unintended solder connections or "bridges", as well as unsoldered leads. After soldering, it is recommended that the rosin flux be removed from the board using flux remover, FREON or paint-thinner type solvent. This will make looking for soldering problems easier and give the board a clean, professional appearance.

IC SOCKET INSTALLATION

Integrated circuit (IC) sockets can be installed by first inserting them into the printed circuit board, then placing another flat board over the IC sockets and finally turning over this sandwich. Be sure that each IC socket is inserted into the proper location and is oriented such that pin 1 of the socket corresponds to the pin 1 indication on the PC board layout legend. (Refer to figure 1A to identify pin 1 on an IC socket.) To solder IC sockets, first solder just two opposite corner pins

for all sockets being installed. Then re-melt the corner connections while applying pressure down on the board. This will remove any gaps that may be present between the IC sockets and the PC board. Finally, solder the remaining pins of the IC sockets.

DIP HEADER SOLDERING

When making jumper connections on a DIP header, solder resistor or capacitor lead clippings between the leads to be connected. When more than two pins are to be connected together, bend a single wire so that it routes to each pin, and solder each pin once. Insert the header in an IC socket on a PC board to hold it during soldering. Overheating the pins with the soldering iron will melt the plastic of the header. If there are multiple jumpers on a header, make sure that no unintended connections are made by carefully routing the jumpers, or insulating each jumper with some wire insulation.

RESISTOR AND CAPACITOR INSTALLATION

To install resistors or capacitors, first make right angle bends in the leads to fit the PC board hole spacing. (Some capacitor leads are already appropriately spaced and do not need bending). Then insert the leads as far as possible through the correct holes in the PC board and spread the leads slightly on the solder side of the board to keep the part in place. After a group of resistors or capacitors has been inserted, then solder the leads on the solder side of the board and snip off the excess leads as close to the board as possible. Use caution to avoid eye injury from flying bits of wire. Save the lead clippings for later use in making jumper connections.

PRINTED CIRCUIT BOARD LAYOUT

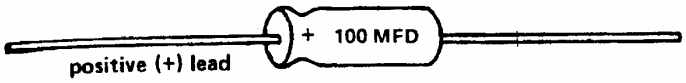
The white component layout legend is printed on the component side of a printed circuit (PC) board. All components are inserted from this side (component side) and soldered on the other side (solder side). Locations on the PC board are identified by two-character codes as marked on the board: a digit followed by a letter indicating the horizontal and vertical coordinates of the location. Note that in North Star kits, IC's can be found on styrene pads in positions corresponding to their intended locations on the PC board.

Pin numbering conventions for the S-100 edge pins are as follows: When viewing the component side of the board (with the pin edge facing down), pins 1 2, ... 50 range from left to right. When viewing the solder side of the board, pins 100, 99, ..., 51 range from left to right.

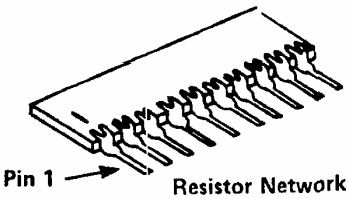
MOS INTEGRATED CIRCUIT HANDLING

Some North Star PC boards use some MOS-type ICs. These parts are identified as such in the instructions. MOS devices can be damaged by static electricity discharge, so special handling is necessary to protect them. Handle MOS devices as little as possible and avoid touching the pins. Place the conductive foam or tube which contains the MOS device onto the PC board before removing the device from the foam or tube. Also, be sure both hands are touching the foam or tube when the device is removed from the foam or tube.

Once an MOS device has been installed in a PC board, handle the board as little as possible. Of course, never insert or remove any IC while power is applied to the board, and never remove or insert a PC board while power is applied to the motherboard.

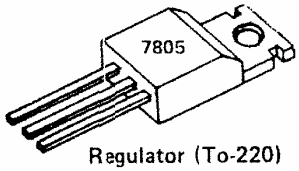


Axial Lead
Electrolytic Capacitor

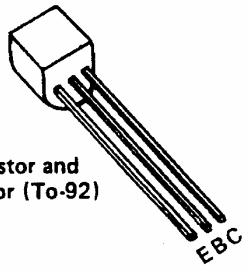


Resistor Network

Resistor

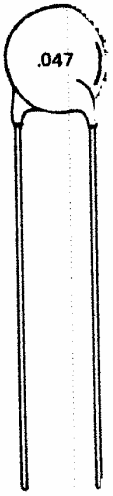


Regulator (To-220)

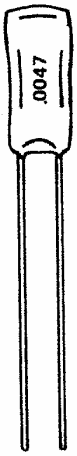


Transistor and
Regulator (To-92)

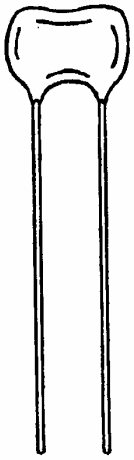
Quick-Connect
Lug



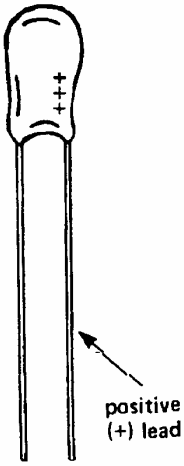
Ceramic
Disc
Capacitor



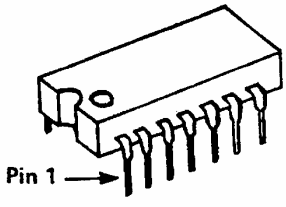
Dipped
Mylar
Capacitor



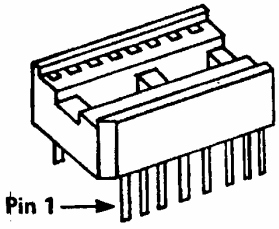
Dipped
Mica
Capacitor



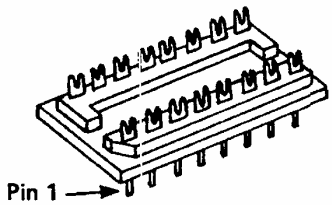
Dipped
Tantalum
Capacitor



Integrated Circuit (IC)



IC Socket



DIP Header

ZPB ASSEMBLY

Before beginning assembly of the ZPB, first check that you have all the parts listed in the parts list.

Note that in the following instructions, "left" and "right." refer to those directions when viewing the component side of the PC board with the 100-pin edqe facing down.

Z1. Using an ohmmeter, check for open circuits between the pair of solder pads for each of the following seven capacitor locations: C22, C23, C25, C26, C27, C28, and C29. If any shorts are found, locate and correct the problem or return the PC board for replacement.

Z2. Insert and solder the 40-pin IC socket at location 3C, following the procedure given in the Assembly Information section.

Z3. Insert and solder the seven 20-pin IC sockets with correct orientation.

Z4. Insert and solder a 16-pin IC socket at location 1G. Note that this socket has reverse orientation from all the others, with pin 1 in the upper right corner.

Z5. Insert and solder the remaining thirteen 16-pin sockets with correct orientation.

Z6. Insert and solder the fourteen 14-pin sockets with correct orientation. Do not install sockets in locations 5C, 5D, and 5E (inside dashed line) unless you are assembling the PROM option at this time.

Z7. Insert and solder the five single-in-line (SIP) resistor networks labeled RN1, RN2, RN4, RN5, and RN6 on the layout legend. RN6 is a 2.2K ohm network and the remaining four are 1K ohm networks. RN3 is part of the PROM option. Orient each SIP so the end marked with a "1" (sometimes this end has a beveled corner) corresponds to the end marked with a dot on the layout legend.

Z8. Insert and solder the. following sixteen resistors. Refer to the Assembly Information section for resistor installation procedures.

	Resistor	Value	Color-code	Location
( )	R1	470 ohm	yellow-violet-brown	1F

( )	R2	470	ohm	yellow-violet-brown	1F
( )	R3	1K	ohm	brown-black-red	2E
( )	R5	1K	ohm	brown-black-red	5G
( )	R6	1K	ohm	brown-black-red	4F
( )	R7	330	ohm	orange-orange-brown	4C
( )	R8	1K	ohm	brown-black-red	6B
( )	R9	1K	ohm	brown-black-red	6B
( )	R11	1K	ohm	brown-black-red	4G
( )	R12	1K	ohm	brown-black-red	7C
( )	R13	1K	ohm	brown-black-red	7A
( )	R14	1K	ohm	brown-black-red	7A
( )	R15	1K	ohm	brown-black-red	8F
( )	R16	10K	ohm	brown-black-orange	8G
( )	R17	100	ohm	brown-black-brown	8G
( )	R18	1K	ohm	brown-black-red	8G

Z9. Insert and solder the 1N4148 diode at location 8G. The end of the diode marked with a band is the cathode end and should be oriented toward the top of the board.

Z10. Insert and solder the 100uf electrolytic capacitor (C29) located near 8A. The positive end (marked with a "+" or a red dot) should be oriented toward the right as indicated on the layout legend. Some capacitors mark the negative end with a "-" instead of the positive end.

Z11. Insert and solder the 39uf tantalum capacitor (C21) near location 7G. Be sure to orient the capacitor so that the lead marked with a "+" is inserted through the hole marked with a "+".

Z12. Insert and solder the two 6.8uf tantalum capacitors (C22 and C23) at locations 8F and 8G. Be sure to orient the capacitors so that the lead marked with a "+" is inserted through the hole marked with a "+".

Z13. Insert and solder the 470pf dipped mica capacitor (C1) at location 1F. Some 470pf capacitors are marked "471JO".

Z14. Insert and solder the 33pf dipped mica capacitor (C5) at location 2F. Some 33pf capacitors are marked "330JO3".

Z15. Insert and solder the nineteen ceramic disc bypass capacitors in locations marked with an asterisk on the layout legend.

Z16. Insert and solder the 8MHz crystal at location 1F. Make right angle bends in the two leads so the crystal will lie parallel with the PC board. To hold the crystal package in place, use a piece of snipped resistor lead to solder the top of the crystal package to the corresponding hole in the board. A. little space should be left between the crystal and the PC board to avoid the possibility of shorts.

NOTE: The 8MHz crystal is used for 4MHz operation of the processor. If 2MHz operation is desired, then a 4MHz crystal (not supplied) should be used. See the Configuration section for details.

Z17. Recheck the circuits between the capacitor leads as in step Z1 and make sure they are still open circuits. Note that the capacitors which have been installed may cause the ohmmeter needle to jump when first contact is made but the indication should rapidly return to a high resistance.

Z18. Insert and solder the two 5-volt regulators (Q3 and Q4). These parts will be marked "7805" or."340T-5". Bend down the three leads of the regulator 90 degrees so that the leads go into the correct holes while the machine screw holes line up. Install the heat sink and regulator so that the following sequence results from bottom to top: 6-32 machine screw head, PC board, heat sink, regulator, lock washer, and nut. Finally, make sure the leads do not touch each other or the heat sinks and then tighten the machine screw and solder the regulator leads.

NOTE: Heat sink grease may be used though it is not generally needed. Tightening the bolts too tight can crack the PC board.

With the computer power off, plug the partially assembled board into the motherboard. Then turn on the power. With a DC volt meter check that both regulators are generating 5 volts output. These voltages can be measured across the pins of C22 and C23. Wait a few minutes and measure again. The regulators should not get very hot in this configuration. However, with all parts installed it is normal for the regulator to feel quite hot to the touch. Remember to turn off the power before removing the board.

Z20. Construct a 16-pin DIP header with jumpers set up for a starting address of E800 hex. This is the standard HORIZON starting address. If some other starting address is desired, change the header after completing the checkout instructions. See figure 1Z for the details of the header configuration. Refer to the Assembly Information section for header construction procedures. Plug the completed header into location 2E (the POJ ADDRESS socket) with the correct orientation.

Insert the 33 integrated circuits (all except the Z80A chip). Be sure that all IC's have pin 1 oriented to the bottom left corner. Do not insert any IC's inside the area for the PROM option (outlined with a dashed line).

Recheck the regulator output voltages as in step Z19.

Remove the PC board from the computer and then plug in the Z80A chip with correct orientation. Refer to the Assembly Information section for MOS device handling procedures.

Inspect the board in a good light to insure that:

A. all solder joints are good, i.e. there are no bridges of solder beween adjacent solder joints, no unsoldered joints, and no cold solder joints indicated by a dull finish on the solder.

B. all IC pins are in the IC socket holes, not outside the socket and not folded under the chip. Pins folded under can often be detected by sighting down a row of chips to see if there is any blockage of light under the chips.

C. all parts are installed in the correct locations with the correct orientation.

The ZPB is now completely assembled. Proceed to the ZPB Board Checkout section.

BOARD CHECKOUT

The following checkout procedure should be followed for a newly assembled board. It can also be used to diagnose problems in previously operational boards.

This checkout procedure assumes that no other board besides the ZPB is plugged into the S-100 bus. This makes it possible to get the ZPB operational even if no other board in the system is yet working. This procedure assumes only that the correct unregulated voltages have been applied to the bus, that the computer has a reset switch, and that the bus lines are not shorted to each other.

The following terms are used in specifying expected test results.

GND	ground, 0 volts DC
LOW	logic zero, 0-.7 volts, normally about .3 volts
HIGH	logic one, 2.4-5.0 volts, normally about 3 volts
+5V	+5 volts from power supply
AC	Signal with pulses (as opposed to DC signal)

When referring to the name of a signal from the schematic drawings, if the signal is identified with a bar over its name then the name of the signal is followed by a slash (e.g., STORE/) in the checkout instructions. When describing an AC pulse, the notation (±W,P) refers to a positive or negative pulse with a width of W and a period of P. For example, a positive pulse of width 125 nanoseconds appearing every 25 microseconds would be represented as (+125ns,25us). See Appendix 1 for details on how to detect pulse signals.

The abbreviation MB before a pin number indicates a bus pin on the motherboard.

If an oscilloscope will be used to test the board, a "scope ground" may be installed by soldering a "bridge" of jumper wire between the two PC board holes that connect edge connector pins 50 and 100 near location 2A. Note that either of the two regulator machine screws can also be used for ground test points.

C1. Check for correct clock signals on the ZPB as follows:

A. Install a jumper wire at PE (near location 4G) if the PE trace was has been cut.

B. Remove the 1W jumper (near location 6G) if it was previously installed.

C. Install a jumper wire at MW (near location 6A) if the MW trace has been cut.

D. With the computer power off, install only the ZPB in the computer motherboard.

E. Turn on the computer power and check for the following signals. Note that all timing signals given below assume the ZPB is configured for standard 4MHz operation.

Signal	Location	Description
PHI	Z80 pin 6	AC,(+125ns,250ns)
PHI 2	MB pin 24	AC,(+125ns,250ns)
PHI 1	MB pin 25	AC,(+62ns,250ns)
2MHZ CLOCK/	MB pin 49	AC,(-250ns,500ns)

If any of these are wrong, trace back to the crystal to determine the cause.

C2. This step will check the reset logic. Use the same setup as the previous step and check the following signals while alternately depressing and releasing the computer reset switch.

Signal	Location	Switch Depressed	Switch Released
RESET/	MB pin 75	LOW	HIGH
	7G pin 6	HIGH	LOW
RST/	5G pin 6	LOW	HIGH
POC/	MB pin 99	LOW	HIGH

C3. Check the auto-jump logic as follows:

A. Leave the board configured as in the previous step.

B. Turn off the computer power and remove the ZPB from the computer. Temporarily connect the PRDY signal to ground by soldering a piece of jumper wire beween 7F pin 5 and 7F pin 7 on the solder side of the ZPB.

C. Install only the ZPB in the computer motherboard and then turn on the power and depress and release the reset switch. The processor should pause immediately after performing the auto-jump sequence and just before executing the first instruction at the auto-jump address. Check that: the SM1 signal at motherboard pin 44 is HIGH.

D. Assuming the jump address specified on the header at location E2 is E800, then E800 should be on the motherboard address lines. HIGH signals should be observed on the following motherboard pins:

pins 32, 85, 86, and 87

LOW signals should be observed on the following motherboard pins:
pins 29, 30, 31, 33, 34, 37, 79, 80, 81, 83, and 84

The processor should have executed a single instruction (JMP E800) and then gone into a wait state during the instruction fetch at that address. The Theory of Operation section describes the auto-jump sequence. If SM1 is high but the address is wrong, check the data paths through the POJ header and multiplexers. If SM1 is LOW, skip to the next step to see if the processor can execute instructions at all. If SM1 has an AC signal, check the wait logic from PRDY to WAIT/.

C4. This step checks out the Z80A while executing a one instruction program.

A. With the power off, remove the jumper from PRDY to ground from the ZPB.

B. Turn on the power and then depress and release the reset switch. The Z80 should be executing an RST 7 instruction repeatedly. Observe that all the data input (DI) lines are HIGH by checking the following motherboard pins:

pins 41, 42, 43, 91, 93, 94, and 95

C. If you have an oscilloscope, then check that the signals ZD0-ZD7 are HIGH during Ml at the Z80A chip pins:

pins 14, 15, 12, 8, 7, 9, 10, and 13

D. Check that the following motherboard address lines are AC signals:

pins 29-34, 37, and 79-87.

E. The RST 7 instruction causes a subroutine call to location 0038 hex, thus the stack address stored will be 0039 hex (stored as alternating 00 byte and 39 hex byte). Thus, if you have an oscilloscope, observing the data output bus(DO), the following motherboard bus pins should have AC signals that go low twice every 2.75 microseconds:

pins 35, 40, 88, and 90.

and the following motherboard bus pins should have AC signals that go low once every 2.75 microseconds:

pins 36, 38, 39 and 89

F. Check for the following signals at the Z80 chip:

Signal	Location	Description
PHI	pin 6	AC, (+125ns,250ns)
M1/	pin 27	AC, (-500ns,2750ns)
INT/	pin 16	HIGH
NMI/	pin 17	HIGH
WAIT/	pin 24	HIGH
RST/	pin 26	HIGH
Vcc	pin 11	+5V
ground	pin 29	GND

G. The following signals should be observed on the motherboard bus lines:

Signal	Location	Description
XRDY	Pin 6	HIGH
VI0/	Pin 4	HIGH
VI1/	Pin 5	HIGH
VI2/	Pin 6	HIGH
VI3/	Pin 7	HIGH
VI4/	Pin 8	HIGH
VI5/	Pin 9	HIGH
VI6/	Pin 10	HIGH
VI7/	Pin 11	HIGH
NMI/	Pin 12	HIGH
STAT-DSBL/	Pin 18	HIGH
CC-DSBL/	Pin 19	HIGH
ADDR-DSBL/	Pin 22	HIGH
DO-DSBL/	Pin 23	HIGH
PHLDA	Pin 26	LOW
PWAIT	Pin 27	LOW
PINTS	Pin 28	HIGH
SM1	Pin 44	AC,(+500ns,2750ns)
SOUT	Pin 45	LOW
SINP	Pin 46	LOW
SMEMR	Pin 47	AC,(+375ns,2750ns)
SHLTA	Pin 48	LOW
SSW-DSBL/	Pin 53	HIGH
PMREQ/	Pin 65	AC,4 -pulses every 2750ns
PRFSH/	Pin 66	AC,(-475ns,2750ns)
MWRITE	Pin 68	AC,(+250ns twice,2750ns)
RUN	Pin 71	HIGH
PINT/	Pin 73	HIGH
PHOLD/	Pin 74	HIGH
PSYNC	Pin 76	AC,3 +pulses every 2750ns
PWR/	Pin 77	AC,(-250ns twice, 2750ns)
PDBIN	Pin 78	AC,(+360ns,2750ns)
SWO/	Pin 97	AC,(-250ns twice, 2750ns)

If these checkout steps have been successful, then the ZPB has successfully done an auto-jump and executed a simple program. Therefore, most of the circuits on the ZPB have been tested. The ZPB should now have its configuration options set. Be sure to remove all special jumpers added during the checkout. It is then ready to be used in conjunction with the other boards in the computer system. If the PROM option is being used, install it at this time.

Diagnosis of a problem in a previously operational board will usually be successful using the following procedure:

1. Determine that the ZPB is in fact the board that has the problem by attempting to use it in another computer.

2. Check that the regulator outputs are correct. Then, in an orderly fashion begin replacing IC's in the ZPB with known good parts until the problem disappears. If a board that was working has not been subjected to any abnormal abuse then an IC failure will be the cause of the problem in nearly every case.

3. If the board is still failing then the problem may be a result of any of the following less likely conditions: dirty edge connector contacts, bad parts other than the ICs, bad connection in an IC socket, or introduction of a short or open in the traces on the board.

PROM OPTION ASSEMBLY AND CHECKOUT

Before assembling the PROM option, the rest of the ZPB should be completely assembled and checked-out.

P1. Insert and solder the 24-pin IC socket at location 4E with the correct orientation.

P2. Insert and solder the three 14-pin IC sockets with correct orientation.

P3. Insert and solder the resistor network RN3 at location 4D so that pin 1 (or the beveled corner) corresponds to the dot on the layout legend.

P4. Insert and solder R4 (3 9K, orange-white-red) at location 3E and R10 (1K, brown-black-red) at location 5C.

P5. Insert and solder the +12 volt regulator (marked "78L12") at location Q1 (near location 8B). Also insert and solder the -5 volt regulator (marked "79L05") at location Q2 (near location 8B). The regulators should be oriented so that the flat sides of the parts face the direction indicated on the layout legend.

P6. Insert and solder the four 2.2uf tantalum capacitors (C25, C26, C27, and C28) at location 8B oriented so that the leads marked with a "+" correspond to the holes marked with a “+” on the layout legend.

P7. Using the 14-pin DIP header and some lead snippings construct a header to determine the PROM location in memory. Refer to the Configuration section (step J8) for details. Plug the completed header into location 5E with correct orientation.

P8. Enable the PROM option by cutting the "PE" trace between locations 3G and 4G.

P9. Insert the 3 integrated circuits as indicated on the layout legend with correct orientation. When inserting the PROM observe the MOS device handling precautions given in the Assembly Information section.

P10. The PROM option can now be checked out by reading the contents of the PROM using a monitor program or control panel. Note, however, that control panels which display the DI bus (e.g., Altair) will not display the PROM contents.

CONFIGURATION OPTIONS

There are a number of configuration options possible on the ZPB that are specified by wiring jumpers on the board. The desired configuration should be wired according to the following instructions before the board is used.

J1. Signal grounding. Backplane pins 20 and 70 may be optionally connected to ground. These connections can be made by installing the jumpers labeled "EC20" and "EC70", respectively, located at 6A. These connections should be made unless these grounds would interfere with the operation of other boards on the bus. Grounding these pins will reduce backplane noise and thus provide more reliable performance. Both pins should be grounded with a HORIZON. Pin 20 should not be grounded for use with the IMSAI. Neither pin should be grounded on an Altair.

J2. Memory wait states. The "1W" jumper to the right of location 7G, if connected, forces at least one wait state on every memory or I/O reference made by the processor. (If a memory board specifies one or more wait states, then that number of wait states will be used for references to that board.) The jumper should be installed if memory in the system is not fast enough to run with zero wait states at 4MHz (about 300ns or faster) and the memory itself cannot be configured to have one wait state. If you are not sure your memories are this fast, connect the jumper to get the system running and experiment later. The North Star 16K RAM Board does not require any wait states.

J3. Processor speed. Normally the processor runs at 4MHz. However, provision has been made to run at 2MHz. To achieve 2MHz operation, replace the 8MHz crystal at location 1F with a 4MHz crystal (not supplied). Then cut the "4" trace above location 6F and install the "2" jumper instead. This keeps the clock on backplane pin 49 at 2MHz as required by some S-100 bus boards.

J4. Address mirroring. As required by some S-100 bus boards the ZPB simulates an 8080 during IN and OUT instructions by driving the port address onto both 8-bit halves of the address bus. To disable this feature and take advantage of the greater flexibility of the Z80, cut the "AM" (address mirror) trace to the left of location 7F and install the "NM" (no mirror) jumper instead.

J5. Control panel. The ZPB normally generates the MWRITE signal to backplane pin 68. if the ZPB is used in systems with control panels or other boards that generate MWRITE, then the "MW" trace below location 6B should be cut. Leave the trace in place for use in the HORIZON. Cut the trace when used with an Altair or IMSAI.

J6. Vectored interrupts. The ZPB is supplied with logic to respond to an interrupt request on the vectored interrupt request lines VI0-VI7 by generating the indicated RST instruction. This logic may be disabled by installing the "ID" jumper above location 7E. This will allow some other board to respond to interrupt conditions.

J7. PROM option. If the PROM option is installed, then the "PE" trace to the left of location 3G must be cut to enable the on-board PROM.

J8. PROM Address Selection. The 1K bytes of on-board PROM can be selected to reside in any of sixty-four 1K regions of the Z80 address space. The address selection logic compares the six high order address bits (A10-A15) from the Z80 against the six bits specified with jumper wires on the header at location 5E. Pins 8-13 correspond to the six address bits A10-A15, respectively. All bits that should match a "zero" bit should have their corresponding pins connected to pin 1 or pin 2 with jumper wires. All bits that should match a "one" bit should have their corresponding pins connected to pin 6 or pin 7 with jumper wires. Figure 1P shows the jumper pin assignments and some examples.

J9. Auto-Jump Address Selection. Any of the 64K different addresses may be specified as the auto-jump address with jumper wires on the 16 pin header at location 2E. The eight pins 9-16 on the header correspond to pairs of address bits according to the following table.

Pin	Low Addr Bit	High Addr Bit
9	0	8
10	1	9
11	2	10
12	3	11
13	4	12
14	5	13
15	6	14
16	7	15

The address bit pins 9-16 should each be connected to one of the pins 1-8 according to the following table:

Connect to pin 1 or 2 if both the high order and low order address bits of the pair are "ones".

Connect to pin 3 or 4 if the high order address bit is a "one" and the low order address bit is a "zero".

Connect to pin 5 or 6 if the high order address bit is a "zero" and the low order address bit is a "one".

Connect to pin 7 or 8 if both the high order and low order address bits of the pair are "zeros".

For example, if bit 9 of the jump address is a "one" and bit 1 is a "zero" then pin 10 should be connected to pin 3 or pin 4. If jump address bit 15 is a "zero" and bit 7 is a "zero" then pin 16 should be connected to pin 7 or pin 8. Figure 1Z shows the jumper pin assignments and some examples.

Z80A AND CONTROL CIRCUITS

The primary function of the ZPB is to interface the Z80A processor to the S-100 bus with its control lines. The following list gives the S-100 control signals along with pertinent comments about their use and derivation. A slash at the end of a name indicates that the signal is active low (negative logic).

Pin	Signal	Description
22	ADDR-DSBL/	Disables the address line drivers onto the S-100 bus when true.
19	CC-DSBL/	Disables drivers for PSYNC, PDBIN, PWAIT, PWR, PMREQ, and PRFSH when true.
23	DO-DSBL/	Disables the data output bus (DO) drivers when true.
68	MWRITE	True during a memory write operation of the Z80. This signal should be disconnected if the ZPB is used in a system where MWRITE is generated on the control panel board or some other board.
78	PDBIN	Indicates that the Z80 is reading the DI bus during a memory read, input, or interrupt acknowledge operation.
26	PHLDA	The hold acknowledge response by the Z80 to a hold request (PHOLD). Indicates that the Z80 execution is suspended and that a DMA bus operation may begin.
74	PHOLD/	Used to request the Z80 to suspend activity and allow direct memory access by a peripheral device.
73	PINT/	Interrupt request line to the Z80 from the on-board Vectored interrupt logic or from some other board.
28	PINTE/	This signal ("interrupts enabled" on 8080 systems) is normally true but goes false momentarily during interrupt acknowledge sequences thus providing an edge to latch the VI lines for boards such as the IMSAI PIC-8.
65	PMREQ/	Memory cycle request signal from the Z80.
12	PNMI	Non-maskable interrupt request to Z80.
99	POC/	System reset synchronized to the Z80 clock. True when the RESET switch is depressed or momentarily when power first comes on.
72	PRDY	When false, causes the Z80 to WAIT. Usually generated by memory boards to extend memory cycles for slow access time memories. See also XRDY.

75	PRESET/	Connected to the reset switch.
66	PRFSH/	Dynamic memory refresh signal generated by the Z80.
76	PSYNC	This signal is true between memory and/or IO cycles of the Z80. Usually one clock cycle wide (sometimes two). Usually used by wait state counters on memory boards.
27	PWAIT	True when the Z80 is in the wait state caused by PRDY or XRDY.
77	PWR/	Timing signal generated during memory write and output operations which indicates that valid data is on the DO bus.
71	RUN	Signal generated by a control panel to indicate the processor should be in run mode
48	SHLTA	True if the Z80 is executing a halt instruction.
46	SINP	True during an input operation.
96	SINTA	True during an interrupt acknowledge operation.
47	SMEMR	True during a memory read operation.
44	SM1	True during the instruction opcode fetch portion of each instruction cycle of the Z80. For instructions with two opcode bytes, this signal is true twice.
45	SOUT	True during output operations.
21	SS	Generated by a control panel to indicate that the Z80 should be in run mode during a single step operation.
98	SSTACK	Always false. On 8080 systems indicates that a stack reference cycle is in progress.
53	SSW-DSBL	Disables DI bus receivers and enables CP bus receivers. Used during input of sense switches from a control panel.
18	STA-DSBL/	Disables drivers for SMEMR, SWO, SINP, SHLTA, SM1, SOUT, and SINTA.
97	SWO	True when the Z80 is sending data out on the DO bus
03	XRDY	Causes the Z80 to enter wait mode when false. Usually generated by a control panel to cause a control panel stop. There has been some conflict of use between this signal and PRDY so care should be taken to guarantee that drivers on this line from different boards cannot be simultaneously active.

DATA BUS

NOTE: This and the following sections will be more meaningful if the schematic drawings are referenced while they are read. The capitalized signal names refer to names used in the drawings. The Z80 data bus (ZD0-ZD7) is the 8 data bits directly connected to the Z80 processor. The data bus from the control panel (CP0-CP7) is gated onto the ZD bus by the CPIN-EN signal during control panel operations. The S-100 data input bus (DI0-DI7) is

gated onto the ZD bus by the DI-EN signal during Z80 read operations (RD-D) except on-board PROM reads and during interrupt operations (XINTA). The ZD bus is gated onto the control panel bus whenever a control panel operation is not in progress. The ZD bus is gated onto the S-100 data output bus (DO0-DO7) by DO-EN during memory write and output operations of the Z80. The data from the on-board PROM is gated onto the ZD bus directly by the PROM-EN signal during on-board PROM read operations.

ADDRESS BUS

The sixteen address lines from the Z80 (ZA0-ZA15) are connected through drivers to the S-100 address bus (A0-A15) except during input/output operations. In this latter case, if the address mirroring feature is enabled then the low order 8 address bits from the Z80 are gated onto both the top and bottom 8 bits of the S-100 address bus. This feature allows simulation of 8080 I/0 operations for systems that include S-100 boards that take advantage of this 8080 characteristic.

VECTORED INTERRUPTS

The on-board vectored interrupt capability provides for a priority response to 8 interrupt levels. Whenever the Z80 generates an interrupt acknowledge condition (INTA), the state of the eight interrupt request lines (VI0-VI7) is latched (8B, 8C) and the latch outputs are fed to a priority encoder (8D). The three encoder outputs indicate the highest priority pending interrupt request. These lines are merged with "1" bits at the multiplexers (2D, 1E) to provide the correct RST instruction on the Z80 data bus (ZD0-ZD7) when the multiplexer is enabled by MX-EN. The INT-RQ signal out of the encoder indicates that at least one interrupt request level is pending and causes an interrupt request to the Z80 if on-board interrupts are enabled (OBIE).

AUTO-JUMP

The auto-jump feature causes an automatic jump to a jumper-wire-specified address (2E) upon power-on or reset. The register at 4G is configured to be a four state counter. The restart condition (RST) resets the register and each successive read cycle (RD) causes the register to shift to the next state until the auto-jump sequence is done in the fourth state (AUJ-DONE). The first three states cause the three bytes of an unconditional jump instruction to the specified address to be multiplexed (1E, 2D) onto the Z80 data bus (ZD0-ZD7). The AUJ-DONE signal disables the auto-jump feature until the next restart condition reinitiates the entire sequence. The AUJS signal causes the two address bytes to be selected by the multiplexers (1E, 2D) during the second and third states. The jump opcode is generated during the first state as a special case of the interrupt logic which generates a JMP instruction rather than an RST.

The auto-jump feature can be disabled by removing the 74LS175 chip from location 4G.

ON-BOARD PROM OPTION

The ZPB has provision for one on-board 2708 type EPROM. The PROM address can be specified by jumper wire selection (5E) to start on any 1K address boundary. The address comparison to test for on-board PROM addresses is performed by the exclusive-or gates (5C, 5D) The PROM is enabled (PROM-EN) if the high order 6 address bits compare during a memory read operation. A wait state is provided for the PROM so that the rest of memory may run at full speed.

APPENDIX 1. PULSE SIGNAL DETECTION

Some steps in the checkout procedure will require test equipment capable of distinguishing a signal containing pulses from a DC signal. Any one of the following will suffice.

1. Use of an oscilloscope is best since the shape and frequency of the pulses can also be determined.

2. Use a logic probe that detects pulses.

3. If the RAM-16-A is being assembled for use with a HORIZON, then use a counter on the motherboard to divide the frequencies down to the audio range and then play the result through a hi-fi amplifier. To do this, remove the 74LS161 at location 7D on the motherboard. Then attach the test probe wire to jumper 2D pin 16 (this is the input to the divider). Next, take the output of the divider at jumper 10A pin 11 and connect to the AUX input of the audio amplifier. Finally, connect the AUX input ground on the audio amplifier to signal ground on the motherboard. This arrangement will divide high frequency signals by 4096 and thus put the resulting signal in the audible range. Thus a 4 MHz signal will be heard as a tone one octave higher than a 2MHz signal.

4. Construct the "probe" shown in figure 1C on a piece of cardboard or perf-board. This probe converts high frequency signals to DC signals. The voltage of the resulting DG signal will be proportional to the duty factor of the tested wave form.

APPENDIX 2. S-100 BUS SIGNALS

PIN #	SIGNAL	PIN #	SIGNAL
1	+8 VOLTS	51	+8 VOLTS
2	+16 VOLTS	52	-16 VOLTS
3	XRDY	53	SSW-DSBL/
4	VI0/	54	EXT-CLR/
5	VI1/	55	
6	VI2/	56	
7	VI3/	57	
8	VI4/	58	
9	VI5/	59	
10	VI6/	60	
11	VI7/	61	GROUND
12	NMI/	62	
13		63	
14		64	
15		65	PMREQ/
16		66	PRFSH/
17		67	PHANTOM/
18	STA-DSBL/	68	MWRITE
19	CC-DSBL/	69	PS/
20	GROUND (optional)	70	GROUND
21	SS	71	RUN
22	ADDR-DSBL/	72	PRDY
23	DO-DSBL/	73	PINT/
24	PHI 2	74	PHOLD/
25	PHI 1	75	PRESET/
26	PHLDA	76	PSYNC
27	PWAIT	77	PWR/
28	PINTE	78	PDBIN
29	A5	79	A0
30	A4	80	A1
31	A3	81	A2
32	A15	82	A6
33	A12	83	A7
34	A9	84	A8
35	D01	85	A13
36	D00	86	A14
37	A10	87	A11
38	D04	88	D02
39	D05	69	D03
40	D06	90	D07
41	DI2	91	DI4
42	DI3	92	DI5
43	DI7	93	DI6
44	SM1	94	DI1
45	SOUT	95	DI0
46	SINP	96	SINTA
47	SMEMR	97	SWO/
48	SHLTA	98	SSTACK
49	2MHZ CLOCK/	99	POC/
50	GROUND	100	GROUND

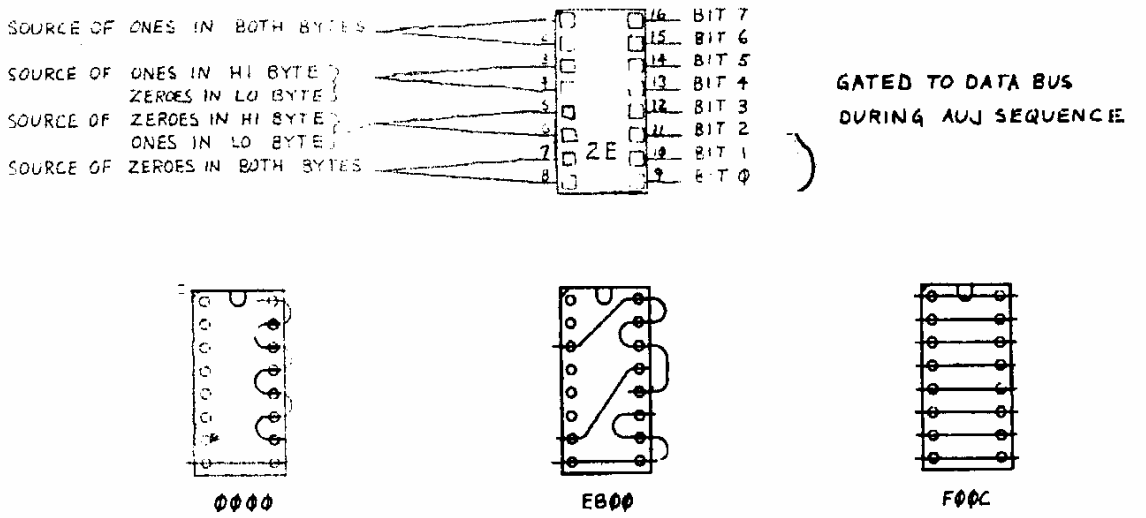


FIGURE 1Z: AUJ (POJ) ADDRESS HEADER (LOCATION 2E), WITH THREE EXAMPLES.

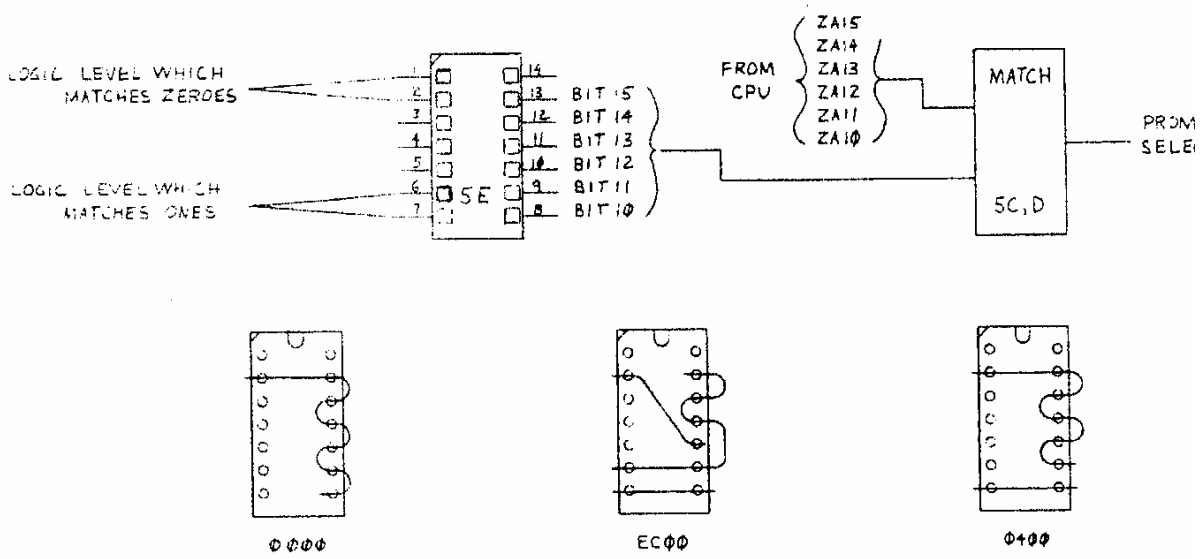


FIGURE 1P: PROM ADDRESS HEADER (LOCATION 5E), WITH THREE EXAMPLES.

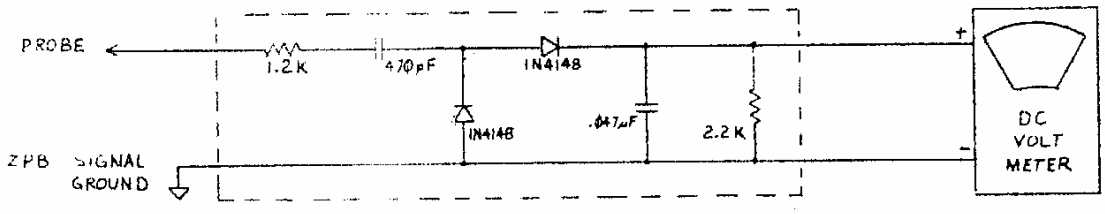
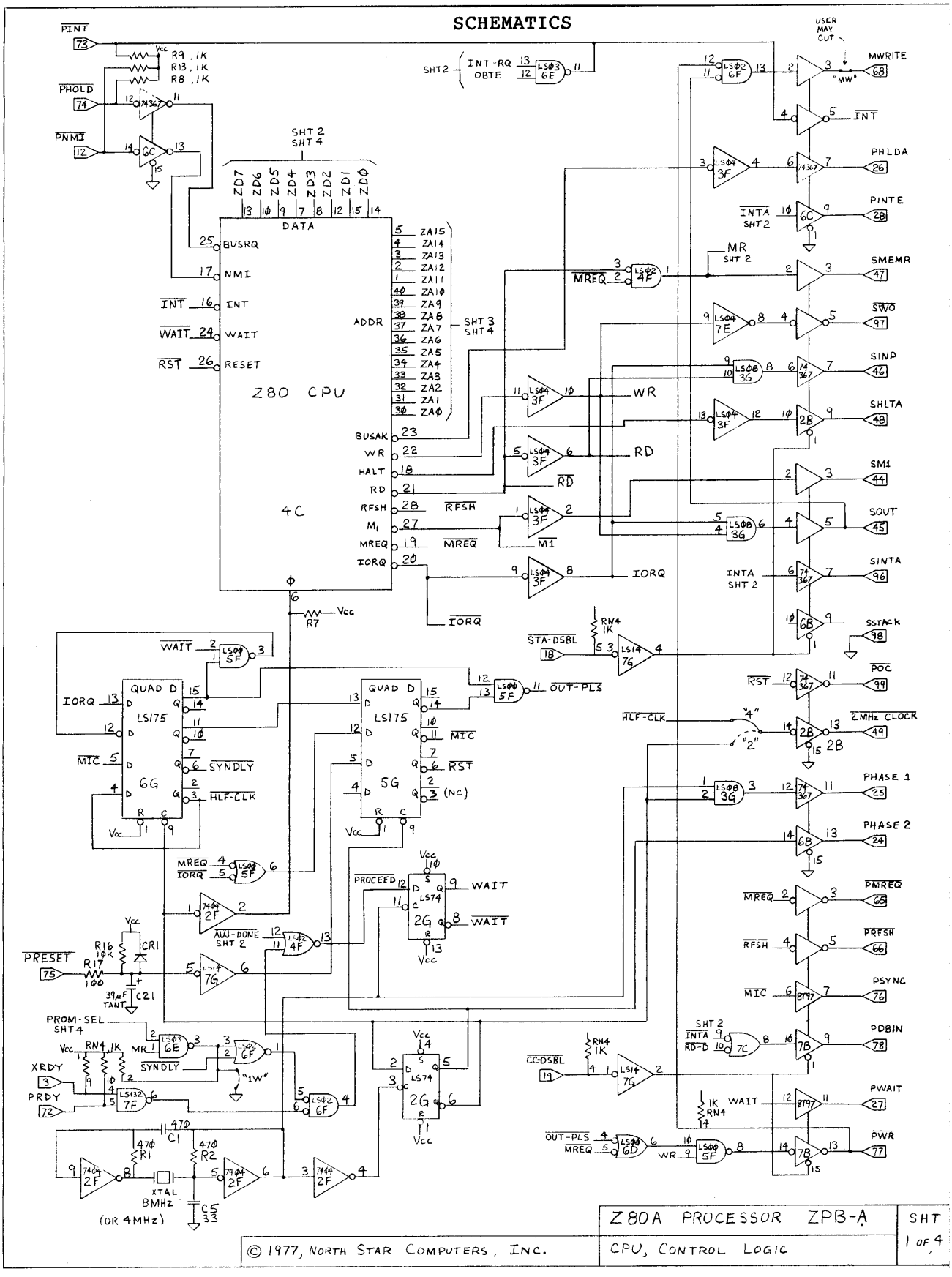
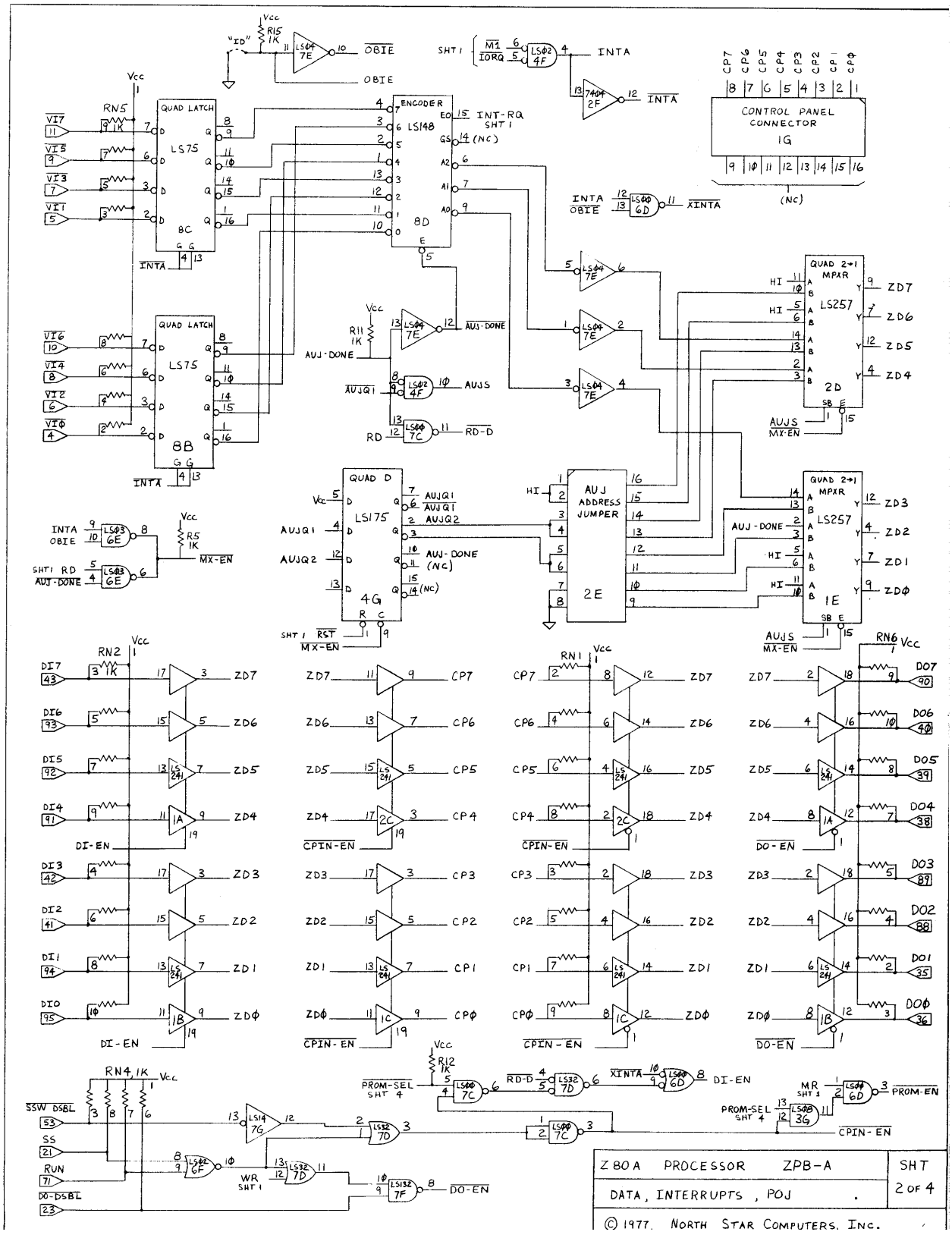
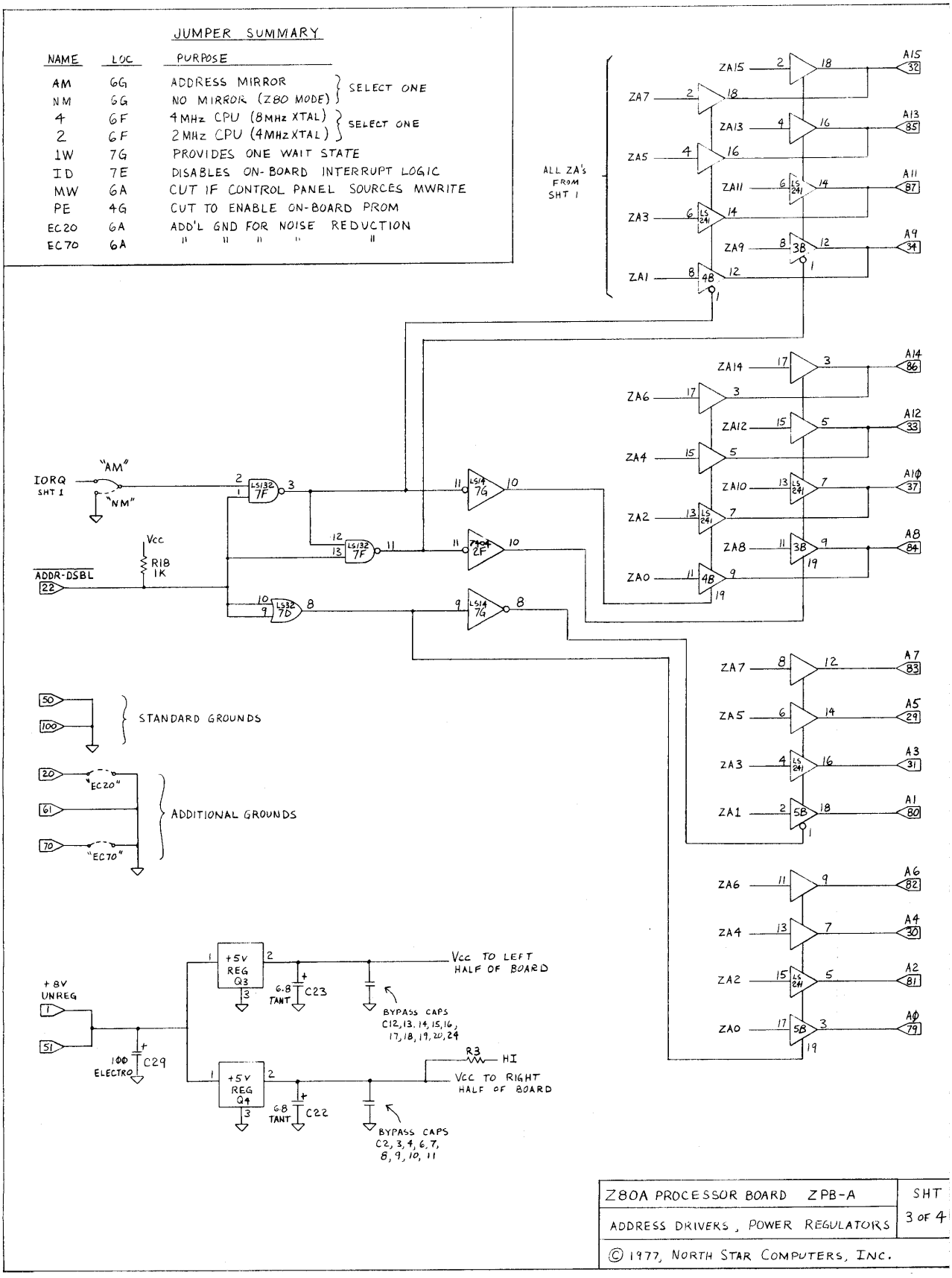


FIGURE 1C: A.C. SIGNAL DETECTOR


SCHEMATICS
Z80 CPU
4C
DATA
ADDR
BUSRQ
NMI
INT
WAIT
RESET
BUSAK
WR
HALT
RD
RFSH
M1
MREQ
IORQ
RST
PINT
PHOLD
PNMI
R9 ,1K
R13 ,1K
R8 ,1K
SHT 2
SHT 4
SHT 3
SHT 4
INT-RQ
OBIE
USER MAY CUT
MWRITE
"MW"
INT
PHLDA
PINTE
MR
SHT 2
SMEMR
SWO
SINP
SHLTA
SM1
SOUT
SINTA
SSTACK
POC
2.MHz CLOCK
2B
PHASE 1
PHASE 2
PMREQ
PRFSH
PSYNC
PDBIN
PWAIT
PWR
WR
RD
IORQ
INTA
SHT 2
STA-DSBL
CC-DSBL
OUT-PLS
MREQ
IORQ
WAIT
RFSH
M1
R7
Vcc
QUAD D
LS175
6G
5G
SYNDLY
HLF-CLK
MIC
RST
(NC)
OUT-PLS
PROCEED
AUJ-DONE
SHT 2
PRESET
R16 10K
R17 100
CR1
39MF TANT C21
PROM-SEL
SHT 4
XRDY
PRDY
"1W"
R1 470
R2 470
C1 470
XTAL 8MHz
(OR 4MHz)
C5 33
© 1977, NORTH STAR COMPUTERS, INC.
Z80A PROCESSOR ZPB-A
CPU, CONTROL LOGIC
SHT 1 OF 4


Z80A PROCESSOR ZPB-A
SHT 2 OF 4
DATA, INTERRUPTS, POJ
© 1977. NORTH STAR COMPUTERS, INC.
CONTROL PANEL CONNECTOR
1G
ENCODER
LS148
8D
QUAD LATCH
LS75
8C
8B
QUAD D
LS175
4G
AUJ ADDRESS JUMPER
2E
QUAD 2→1 MPXR
LS257
2D
1E
CPIN-EN
DO-EN
DI-EN
MX-EN
AUJS
AUJ-DONE
INT-RQ SHT 1
INTA
OBIE
XINTA
PROM-SEL SHT 4
PROM-EN
SSW DSBL
DO-DSBL
WR SHT 1
RD-D
RD
SHT 1 RST


JUMPER SUMMARY
NAME LOC PURPOSE
AM 6G ADDRESS MIRROR } SELECT ONE
NM 6G NO MIRROR (Z80 MODE) }
4 6F 4MHz CPU (8MHz XTAL) } SELECT ONE
2 6F 2MHz CPU (4MHz XTAL) }
1W 7G PROVIDES ONE WAIT STATE
ID 7E DISABLES ON-BOARD INTERRUPT LOGIC
MW 6A CUT IF CONTROL PANEL SOURCES MWRITE
PE 4G CUT TO ENABLE ON-BOARD PROM
EC20 6A ADD'L GND FOR NOISE REDUCTION
EC70 6A
ALL ZA's FROM SHT 1
ZA15
ZA7
ZA13
ZA5
ZA11
ZA3
ZA9
ZA1
A15
A13
A11
A9
ZA19
ZA6
ZA12
ZA4
ZA10
ZA2
ZA8
ZA0
A14
A12
A10
A8
IORQ SHT 1
"AM"
"NM"
Vcc
R18 1K
ADDR-DSBL
22
STANDARD GROUNDS
50
100
ADDITIONAL GROUNDS
20
61
70
"EC20"
"EC70"
ZA7
ZA5
ZA3
ZA1
ZA6
ZA4
ZA2
ZA0
A7
A5
A3
A1
A6
A4
A2
A0
+8V UNREG
1
51
100 ELECTRO C29
+5V REG Q3
+5V REG Q4
6.8 TANT C23
6.8 TANT C22
Vcc TO LEFT HALF OF BOARD
Vcc TO RIGHT HALF OF BOARD
BYPASS CAPS C12, 13, 14, 15, 16, 17, 18, 19, 20, 24
BYPASS CAPS C2, 3, 4, 6, 7, 8, 9, 10, 11
R3
HI
Z80A PROCESSOR BOARD ZPB-A
ADDRESS DRIVERS, POWER REGULATORS
SHT 3 OF 4
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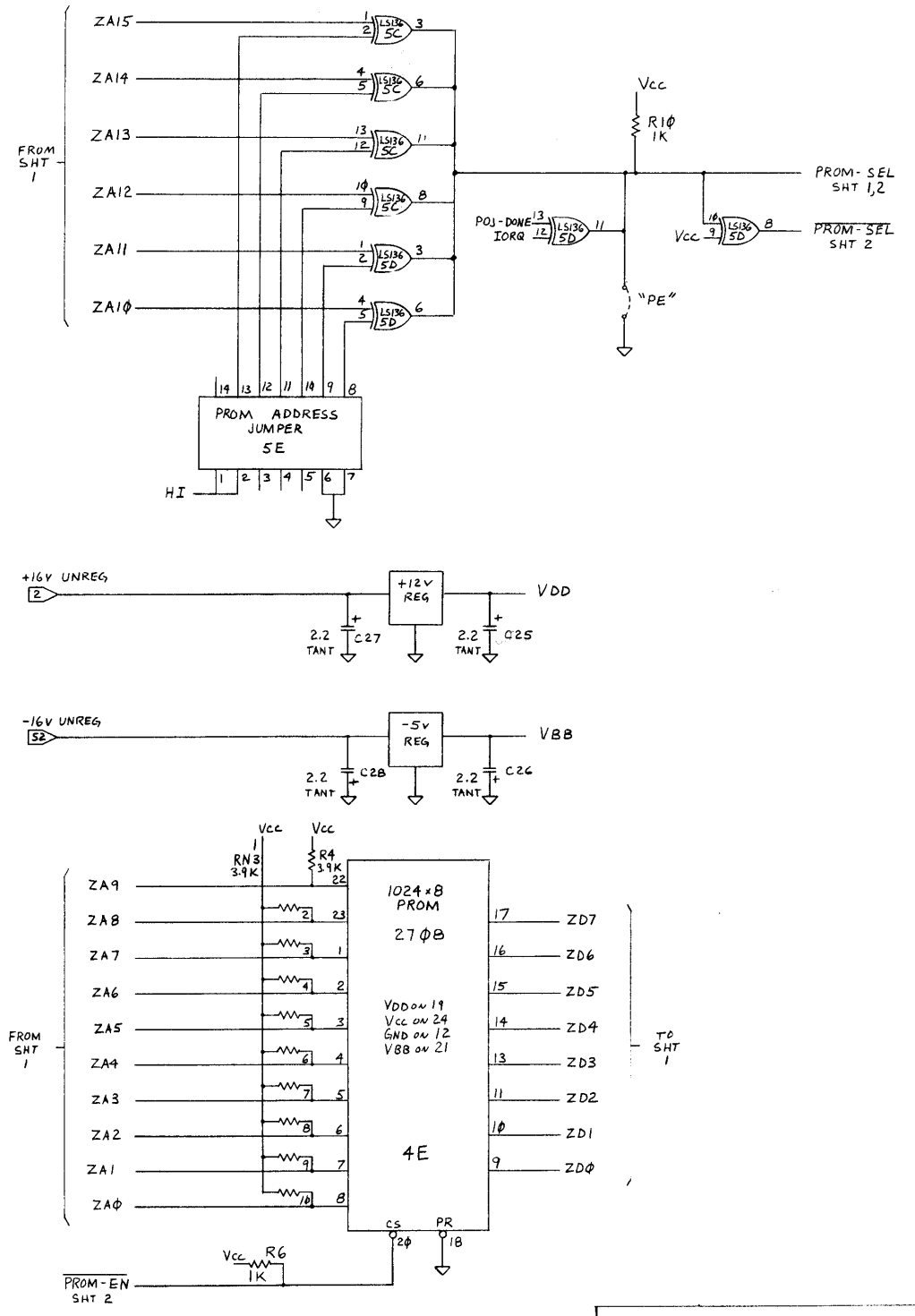

Z80A PROCESSOR ZPB-A	SHT 4 OF 4
PROM OPTION	
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