Helios II

Model 2 (Part No. 300000)

Model 4 (Part No. 304000)

Disk Memory System Manual

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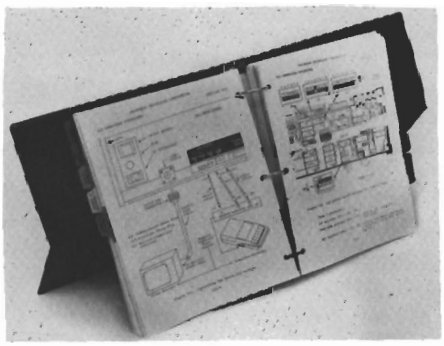
PREFACE

As a convenience feature for the user, this three-ring binder is an "easel" binder. The cover is hinged across the front and back as well as down the binding. You may find it helpful to stand up the binder in its easel position for two-handed operations when reference to the manual is necessary at the same time, as in the assembly sections, or troubleshooting.

TO USE THIS FEATURE: (Refer to illustration below)

1. Lay the manual open on a table. Bend back the full width of the bottom half of the binder along the creased hinge until a resistance to further bending is felt.

2. Set the manual up on the table, with the bottom of the pages down against the table, and the top inclining away from you. (It is supported from falling by the portion of the binder you have bent back.)



IMPORTANT NOTE

The first part of this manual you should read is at the very end: the Updates section. Integrate this information into your manual before you begin.

The reader is invited to participate in the evolution of this manual. Please send your comments or suggestions for improvements to Processor Technology.

In Memoriam

This book is dedicated in grateful memory of Noel Leffler, a fine engineer and good person who is largely responsible for this book, but who died before his Helios II project was completed.

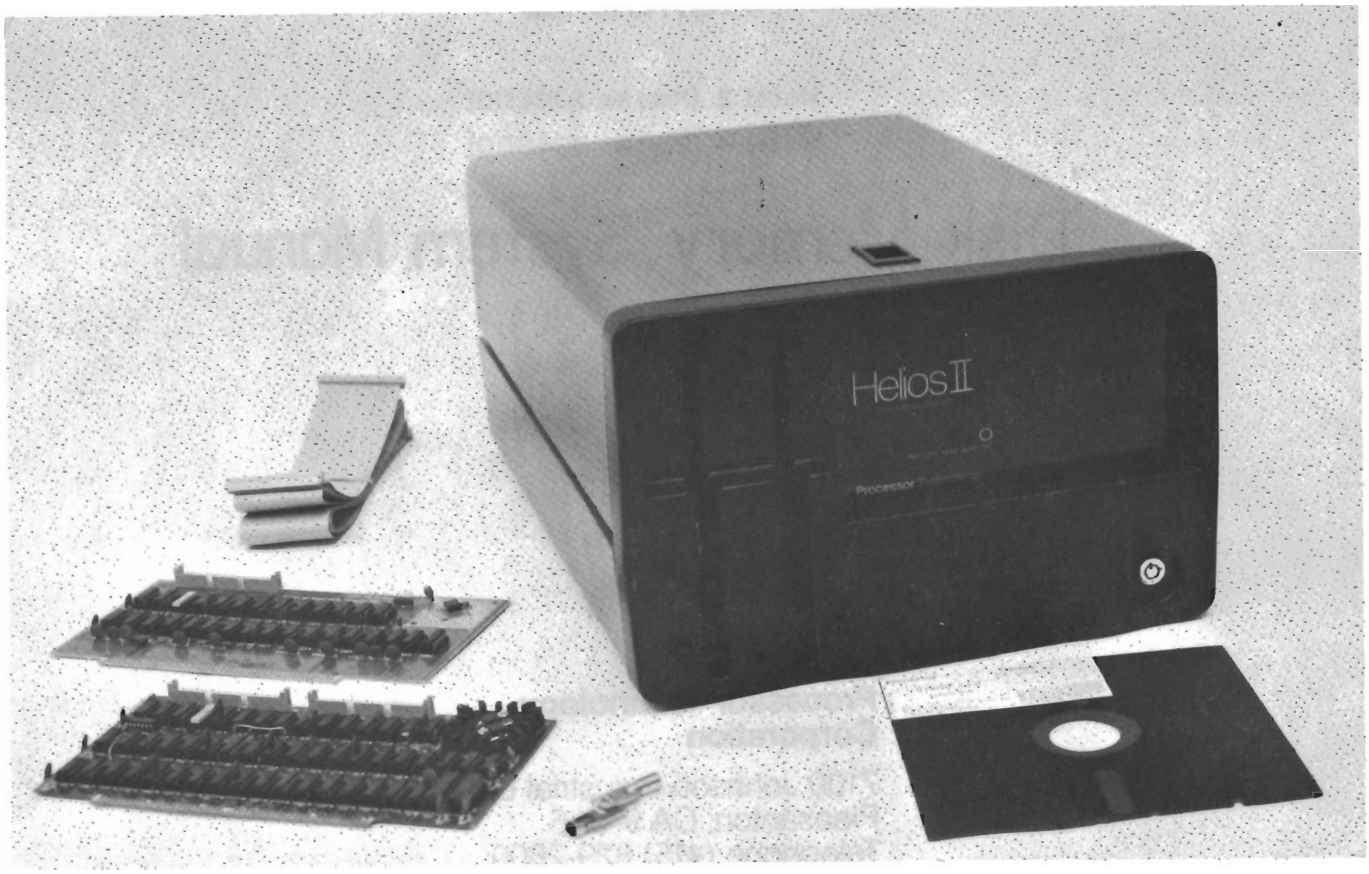


Fig. Ø Helios II System: Diskette Drive Cabinet, Controller and Formatter PCBs and Diskette containing PTDOS

CONTENTS OUTLINE

Detailed contents precede each section.

SOFTWARE MANUAL: PTDOS User's Guide

NOTE

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ABBREVIATIONS

±	Plus or minus
A	Ampere; Automatic; Address
AC	Alternating current
ACI	Audio Cassette Interface
ADDR DSBL	Address Disable
A/R	As received
Assy	Assembly
Aux	Auxiliary
AWG	American Wire Gage
BC	Bit Counter
BCTC	Bit Counter transmission complete
Bin	Binary
BO	Bootload
Br.	Bridge
BTU	British Thermal Unit
BUSTR	Bus Strobe
C	Celsius (centigrade); Capacitor
CC	Construction Counter
CC DSBL	Command/Control Disable
Cer	Ceramic
CF	Carbon film
CI	Command Interpreter
Cm	Centimeter
CNTR	Counter
Comm	Commoning
Conn	Connector
CPSI	Clock Pulse Serial Input
CPSO	Clock Pulse Serial Output
CPU	Central Processing Unit
CR	Carriage Return
CRC	Cyclic Redundancy Check
CRC ERR	CRC Error
CUTS	Computer Users Tape System
CWE	Check Write Enable Signal on formatter, CRC gen.
D	Display
DC	Direct Current
DI	Data Input
DIO	Diode
DIP	Dual-In-Line Package
DMA	Direct Memory Access
DNSYNC	Name of a FF on the controller
DO	Data Output
DO DSBL	Data Out Disable
DOS	Disk Operating System
Drv	Drive
DS	Data Serial
EMI	electromagnetic interference
EO	Enable Output (Fifo signal)
EX-OR	exclusive OR
F	Fahrenheit
Fab	Fabrication
FF	Flipflop
FIFO	First-In, First-Out (LSI Buffer)
FIFOPL	FIFO Parallel Load
FIFO QS	Fifo Serial Output
Fig	Figure
ft	feet
FW	Flat Washer
g	gravity (unit of measure)
GND	Ground
Hex	hexidecimal
HN	hex nut

HRR	Hold Request Resynchronized
Hz	Hertz (cycle)
IC	Integrated Circuit
ID	Identifier
IESA	Input Enable Serial, A
IESB	INPUT Enable Serial, B
Insul.	Insulated
Inv	Inverter
I/O	Input/Output
IRF	Input Register Full
ITLW	Internal Tooth Lock Washer
J	Jack
JK	Inputs to a JK Flipflop
K	kilobyte
Kg.	kilogram
kHz	kilohertz
LED	Light Emitting Diode
LS	Low Power Schottky
mA	milliampere
µf	microfarad
max.	maximum
MOS	Metal Oxide Semiconductor
MPX	multiplexer
MR	Master Reset (Fifo signal)
µs	microsecond
ms	millisecond
MTBF	Mean Time Between Failures
MTTR	Mean Time To Repair
N	number
NA	Not Applicable; National Semiconductor
NET	network
No.	number
NPN	Negative, Positive, Negative
ns	nanosecond
Ω	ohm
OD	outside diameter
OESA	Output Enable Serial, A (Fifo signal)
OESB	Output Enable Serial, B (fifo signal)
ORE	Output Register Empty
P	Plug; Processor
PC	Punctuation Counter
PCB	Printed Circuit Board
PCHI	Signal on formatter
PCL	Punctuation Counter L
PCQ	Punctuation Counter Output
PCX	Punctuation Counter X
PDBIN	Processor Data Bus In
PHLDA	Processor Hold Acknowledge
PHLDAR	Delayed PHLDA
PHMS	Phillips Head Machine Screw
PINTE	Processor Interrupt Enable (S-100 signal)
PL	Parallel Load
Plex	plexiglas
POC	Power On Clear
PRDY	Processor Ready
PT	Processor Technology
PTDOS	Processor Technology Disk Operating System
PWAIT	Processor Wait (S-100 signal)
PWR	Processor Write
Pwr	power

Q	transistor; Output of a JK flipflop
R	Resistor
RAM	Random Access Memory
RCLOCK	Read Clock
RDATA	Read Data
Recpt.	receptacle
Rect.	Rectifier
Reg.	regulator
REV	revision
RH	Relative Humidity
RMC	Read missing clock
RND	Round
rpm	revolutions per minute
RSECT	Sector Reset
RQST	Request
R/W	Read or Write
S	Seek; Status
S-100	name of Intel standard 100-pin bus interface
SREADY	Status Ready
SS	solid strand
sec.	second
SHLTA	Status Halt Acknowledge
SINP	Status Input
SINTA	Status Interrupt Acknowledge
Sldr	solder
SM1	Status Machine Cycle 1
SMEMR	Status Memory Read (S-100 signal)
SOUT	Status Output
SWO	Status Write Out (S-100) Signal
SYNC	Synchronization
Tant	tantalum
TC	Transmission Complete
TCSI	Transmission Complete Serial Input
TOP	Transfer Out Parallel (Fifo Signal)
TOS	Transfer Out Serial (Fifo Signal)
TP	Test Point
TR	transfer
TRANS COMM	transfer command
TTS	Transfer to Stock, FIFO signal
U	Integrated Circuit
UFO	Unidentified Flying Object
UUT	Unit Under Test
ϕ2	Phase 2 (Signal on Controller)
V	Volt(s)
VAC	Volts AC
VCC	+5 V (Fifo pin)
VDC	Volts DC
VDM	Video Display Module
VOM	volt/ohm meter
XCVR	transceiver
XEQ	Execute
XRDY	External Ready

CONTENTS

SECTION 1 INTRODUCTION

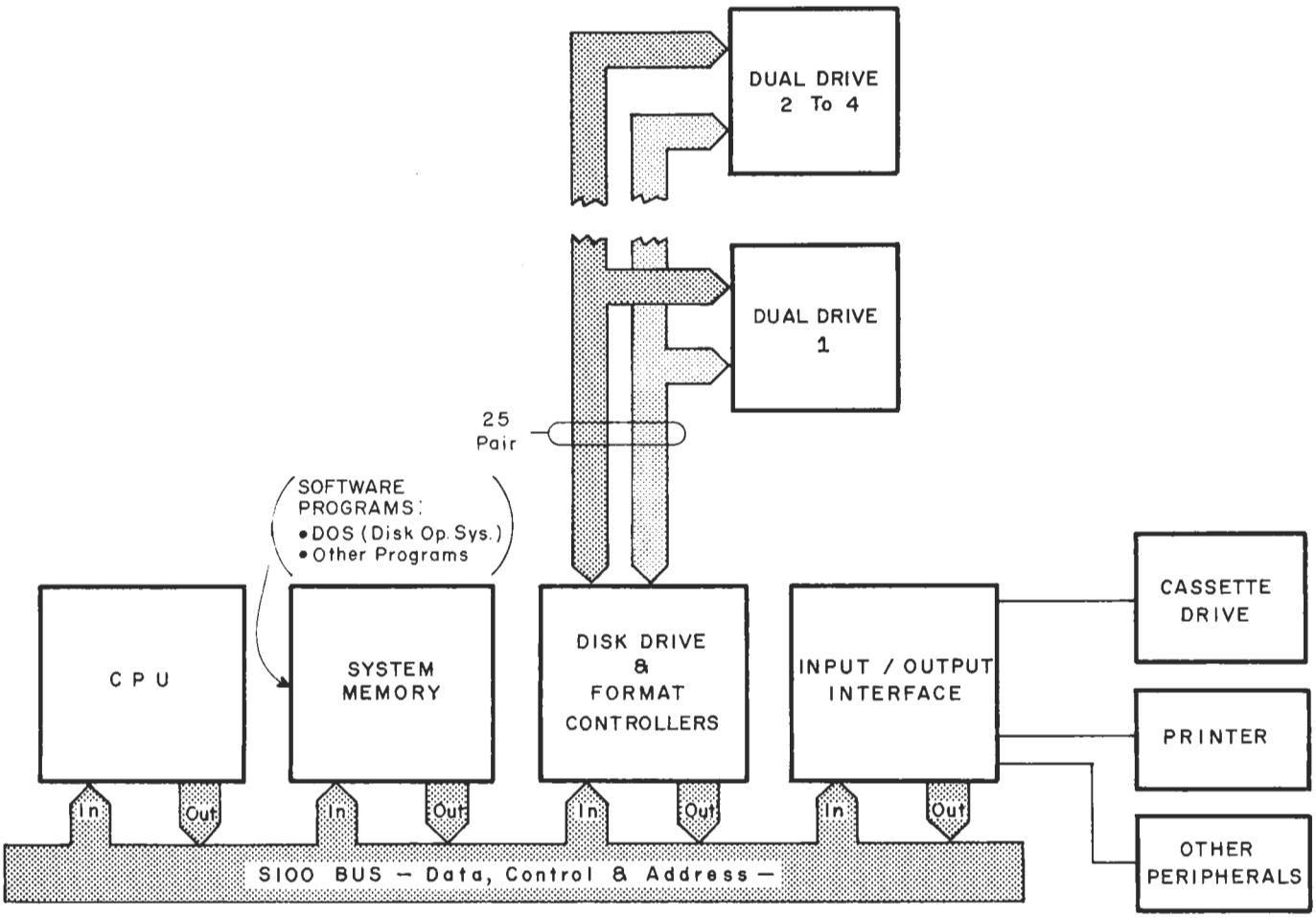

Fig. 1-1 Helios II System, Generalized Block Diagram

SECTION 1 INTRODUCTION

1.0 SCOPE OF THIS MANUAL

This manual is an operating and light maintenance reference for Helios II floppy disk memory system in its various configurations. The binder containing this manual also contains the system software manual, PTDOS User's Manual.

For detailed drive assembly troubleshooting, and replacement procedures for authorized dealers, refer to Helios II Service Manual.

1.1 GENERAL DESCRIPTION OF THE Helios II SYSTEM

(Refer to Fig. 1-1, Helios II System, Generalized Block Diagram.)

The Helios II is a dual floppy disk drive system designed as a mass data storage for host microcomputers using the S-100 bus. The disk drive unit is a firm-sectored type, which uses an optical sector and indexing system. The diskette required is a standard 32+1 hole diskette. System storage capacity is approximately 768,768 bytes per dual drive (two diskettes). The controller in the system is capable of interfacing up to four dual drives in two cabinets. Access time is approximately 173 ms typical. DMA (Direct Memory Access) transfer rate is approximately .66 megabyte per second. A sixteen byte fifo buffers the drive and computer.

1.2 PHYSICAL CONFIGURATION (Refer to Fig. 3-4, Diskette Drive Cabinet, Inside View.)

A. Model 2

The Helios II Model 2 consists of one dual drive unit, in its own air cooled cabinet, a controller PCB and formatter PCB which plug into the backplane of the S-100 bus, a power supply and cabling. (Refer to the frontispiece "Helios II System ...") The formatter is virtually part of the controller. The formatter PCB does not have to be plugged into the backplane. A Model 2 can be upgraded to a Model 4.

B. Model 4

The Helios Model 4 consists of two dual drive units in a cabinet the same size as the Model 2. It differs from the Model 2 in that it has two fans, a higher capacity power supply, and a larger indicator display. It uses the same controller and formatter PCBs.

Two Model 4s can be daisy-chained in an 8-diskette-unit system which can be accommodated by standard controller and formatter PCBs and PTDOS software.

1.3 OPERATING SYSTEM and TEST/DIAGNOSTIC PROGRAMS

A disk operating system called PTDOS (Processor Technology Disk Operating System) is provided on a diskette. A test program is also provided on cassette.

1.4 DESCRIPTION OF DISKETTE DRIVE ASSEMBLY

(Refer to Item 7, Fig. 8-2, Cabinet Assembly, Model 2, Exploded.)

The Helios II diskette drive assembly (commonly referred to hereafter as "drive assembly") is installed in the Helios II cabinet as a separate subassembly without DC power or cabling of its own. Signal and power are provided from interconnections from other subassemblies in the system.

The Helios II diskette drive is designed to provide a means of low-cost, random-access data storage. This is accomplished through the recording of data on, and the retrieval of data from two separate rotating magnetic surfaces, as represented by two separate diskette cartridge assemblies (commonly called diskettes).

Means for easy acceptance, rotation, and quick independent removal of each diskette is provided by spindles which are linked to and derive their rotational motion from an electrical drive motor.

The diskette drive consists of: selectable read/write/erase electronics; common positioning control electronics; a common head positioning actuator; a common Track ØØ sensor; a common spindle drive mechanism; two read/write/erase heads; two head loading actuators; two separate index sensors.

1.4.1 DISKETTE ACCESS

Data is transferred to or from each diskette through its separate read/write/erase head.

Each read/write/erase head is assembled on a carriage which is located on the common head positioning actuator. The read/write/erase head is in direct contact with the diskette media surface. The head employs a single read/write gap followed by tunnel erase elements to provide erased areas between data tracks. Thus, normal track position tolerances between media and drives will not degrade the signal-to-noise ratio, and the diskette interchangeability is enhanced.

1.4.2 ELECTRONICS

A. Sufficient control electronics are employed to provide minimal data access time at optimal data transfer rates within compatibility requirements.

   The electronics perform the following functions:

1. Interpret and generate control signals.
2. Move the read/write/erase heads to the selected track.
3. Load the heads and read or write data.
4. Drive the spindle motor.

B. The electronics are packaged on printed circuit boards containing the following circuits:

1. Head positioning actuator driver.
2. Head load actuator drivers.
3. Read/write/erase amplifier and transition detector.
4. Index detection.
5. Track position and data safety sensing.
6. Spindle motor driver.

1.5 DISKETTE (Refer to Section 2, for specifications.)

The diskette is a cartridge that consists of a flexible magnetic disk enclosed in a plastic jacket. The disk is free to rotate within the jacket. Access and sector/index holes for the read/write/erase head and for data timing are provided. There are 32 sector holes and one index hole. Data is recorded only on one side of the diskette at the present time. The Helios II has provisions for the addition of another index photosense assembly to accommodate recording on both sides of the diskette. Reading and writing are done with the head in contact with the disk.

The diskette is provided with an envelope and container to protect the diskette when not in use. Detailed handling instructions are described in Section 4, Operating Instructions.

1.5.1 DISKETTE INTERCHANGEABILITY

Each diskette drive in conjunction with the controller transfers data to and from the diskette in such fashion that diskettes are fully "write/read" interchangeable within any other Helios II diskette drive system. (See Section 4.3.3, Diskette Compatibility with Other Systems.)

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SECTION 2 SPECIFICATIONS

CONTENTS (Continued)

SECTION 2 SPECIFICATIONS

2.0 INTRODUCTION

These specifications are divided into four subsections:

1. System (the cabinet and the PCBs installed in the host computer and cabling).
2. The PCBs excluding those in the drive assembly.
3. The diskette drive assembly.
4. The diskette.

All specifications pertain to a Model 2 (one dual drive) unless noted otherwise.

2.1 SYSTEM SPECIFICATIONS

2.1.1 PHYSICAL

A. Net Shipping Weight: 24.04 Kg. (53 lbs.)

B. Cooling: Forced air with passive mechanical filter.

C. Dimensions (cabinet) Height: 23.47 cm (9.24")
Width: 35.59 cm (14.01")
Length: 50:72 cm (19.97")

2.1.2 ENVIRONMENTAL

A. Temperature and Humidity

1. Operating

a. Range: 10 to 38°C (50 to 100°F)

b. Max. gradient: 36°C (20°F) per hour.

c. Relative Humidity: 8 to 80%.

d. Max. Wet Bulb Temperature: 25°C (78°F).

2. Storage (Non-operating)

a. Range: -29 to +49°C (-20 to +120°F).

b. Max. gradient: 36°C (20°F) per hour.

c. Relative Humidity: 8 to 80%.

d. Max. Wet Bulb Temperature: 29°C (85°F).

B. Ambient Air: Clean, dust and particle free air, cool with 50% humidity. No corrosive gases in the air. No colloids such as tobacco smoke.

C. Other: (See 2.3.3, Diskette Drive Assembly.)

2.1.3 POWER REQUIREMENTS (Cabinet with contained components, excluding PCBs in host computer.)

117 VAC, 8A Max; 5.0 nominal running

OR: 230 V, 50 Hz

Average Power Consumption: 30 watts

2.2 PCBs

The following PCBs are components of the system outside of the diskette drive assembly:

1. Controller
2. Formatter
3. Indicator Panel
4. Regulator

A. IC Technology

TTL and low power Schottky TTL.

B. Power Requirements

PCB	Voltage	Current (Typical)
Controller	+8 VDC (typical) +7.25 VDC (min.)	1600 mA
Formatter	+8 VDC unregulated +7.25 V (min.)	600 mA
Regulator	+8 VDC unregulated (min.); -8 V 60 Hz (min.); 24 V 60 Hz (min.)	
Indicator	+5 VDC	175 mA

C. Connectors

J2 of formatter PCB (jack which mates with P2): consists of a female shell: Molex Part No. 22-01-2015 and three pins, Molex Part No. 09-50-01114. (P2 is not supplied; see Section 3.5, Optional DC Power for Formatter PCB.)

2.3 DRIVE ASSEMBLY (Removed from cabinet and system)

2.3.1 DIMENSIONS

Height: 21.84 cm (8.6")
Width: 11.18 cm (4.4")
Depth: 38.1 cm (15.0") overall from mounting surface
Weight (shipping): 11.34 Kg. (25 lbs. max.)
Weight (installed): 9.07 Kg. (20 lbs. max.)

2.3.2 MULTIPLE-DRIVE OPTION

The multiple-drive option provides for the operation from one controller and two power supplies of up to four dual diskette drives (8 drive units) in close physical proximity to each other. All diskette drives in this system configuration use the same printed circuit boards. However, the line-terminating resistors on the diskette drive electronics printed circuit board (Data and Interface PCB) and indicator panel PCBs and are removed from all but the drive farthest from the controller, and the proper drive selector module is inserted in each drive. (Refer to Section 4.2.2, Drive Configuration.)

2.3.3 ENVIRONMENTAL REQUIREMENTS:

The diskette drive and diskette should be in the same environment and subject to the same environmental conditions (especially temperature and humidity) for at least one hour prior to operation, as normal recommended operating procedure.

A. Temperature, Relative Humidity, Maximum Wet Bulb

(See Section 2.1.2, System Environmental.)

B. Magnetic Fields

1. Operating

The ambient stray magnetic field in the region of the head should not exceed 15 Gauss.

2. Storage

The ambient stray magnetic field in the region of the diskette should not exceed 50 oerstads.

C. Altitude

1. Equipment Operational

Sea level to 10,000 feet.

2. Equipment Non-operational

Sea level to 35,000 feet.

D. Shock and Vibration

The equipment should not suffer damage nor fail to perform as specified after having been subjected to the following shock and vibration under non-operational conditions:

1. Shock

Internal bracing is allowed if needed to meet this requirement. Eighteen (18) impact shocks of 5 g's (±10%) consisting of three shocks in opposite directions along each of three mutually perpendicular axes. Each shock impulse shall be a half sine wave with a time duration of 11 (±1) ms.

2. Vibration

Internal bracing is allowed, if needed, to meet this requirement. 1.5 g's (±10%) for the 5 to 55 (Hz) range for four hours on each axis with a 20-minute frequency scan.

E. Cleanliness

The Helios II diskette drive assembly is designed for use in commercial and industrial environments. However, no air filters or forced-air systems are provided within the diskette drive itself. Therefore, it should be kept in the Helios cabinet. If it must be removed from the cabinet for maintenance, and operated, optimum performance can be expected when used in a computer room environment with the resultant air cleanliness found in such a location. Dust and other airborne contaminants are a major threat to the operating life of the media and drive recording and positioning systems. (Refer to Section 6, Maintenance.)

2.3.4 ELECTRICAL SPECIFICATIONS

A. DC Power

The following DC power is required per dual diskette drive:

+5V DC = 5%	1.7 A nominal running. 2.2 A maximum running.
+8V DC Unregulated (Limits: 7.0 to 10.0V)	1.2 A nominal running. 2.0 A maximum running.
-5V DC = 10%	0.15 A nominal. 0.20 A maximum.
+24V DC + 10%	1.0 A nominal when seeking. 0.2 A nominal when not seeking. 1.2 A maximum seeking with 3.0 A. maximum peak surges for up to 10 ms at start of seek.

B. Logic Levels

Interface line logic levels are as follows:

Negative level = 0.0V to ±0.5V.
Positive level = ±2.5V to ±5.5V or open circuit.
I/O signals are negative when selected (True).

2.3.5 FUNCTIONAL SPECIFICATIONS

A. Diskette Loading Controls

Diskette loading and unloading is under manual operator control. Loading and unloading mechanisms within the drive provide the following features:

1. Positive diskette registration when loaded.
2. Visible, partial ejection of the diskette when unloading.
3. Minimum possibility of diskette damage due to loading/unloading.

4. Easy diskette loading and unloading.
5. Unloading initiated manually or by remote control line (remote on designated options only).

B. Diskette Rotational Speed Control

1. Spindle Drive System

A direct-coupled DC spindle motor servoed to follow a reference frequency comprises the diskette spindle drive system. Spindle power is applied by inserting one or both diskettes into the diskette drive.

2. Motor Speed Regulation

a. Average Diskette Rotational Speed: 360 ±7 rpm

b. Instantaneous Speed Variation: ±5 rpm

3. Motor Start Time

The diskette drive comes up to speed and attains operational status with 1 second after the application of drive DC or diskette insertion.

C. Head Loading

1. Head Engage Time

The head engage time is less than 40 ms.

2. Head Contact Force

The head-to-disk contact force is 13 grams nominal, as established by testing and vendor recommendations.

D. Head Positioning

1. Head Positioning Times

Track-to-track, including settling time: 10 ms max.

Inside-to-outside track, including settling: 100 ms max.

2. Rotational Latency

Average rotational latency: 83.3 ms.

3. Head Positioning Error Rate

The head positioning error rate is less than one positioning error per 10^6 seek executions.

E. Data Recording

1. Recording Mode

Data is represented on the diskette by 8-bit bytes.

2. Recording Format

Firm-sectored type, formatted by PTDOS (Refer to Section 7, Theory of Operation.)

3. Recording Density

Data is recorded at a nominal density of 6536 (±4%) flux changes per inch for an all 1's pattern on the innermost track, and 3672 (±4%) flux changes per inch for an all 1's pattern on the outermost track.

4. Recording Capacity

Unformatted data capacity is 3.1 megabits per diskette and 41 kilobits per track, single-side recording. Seventy-seven (77) tracks are available.

5. Write Data Transfer Rate

The write data bit rate is determined by the controller. The nominal bit rate is 250 kilobits per second. To insure that the recording density and read data bit rate are held within the specified limits, the write data bit rate shall not vary more than ±0.3% from nominal.

6. Read Data Transfer Rate

The read data bit rate is determined by the recording density and the rotational speed of the diskette being read. The nominal bit rate is 250 kilobits per second. Due to variations between diskette drives and controllers, this bit rate may vary as much as ±17% on an instantaneous basis (including pulse crowding effects).

7. Recoverable Read Error Rate

A recoverable read error is defined to be a read error corrected by no more than three attempts to read the record in error. The recoverable read error rate is less than one error per 10^9 bits read. All error rates are quoted for reading and writing on the same machine without removal and re-insertion of the diskette. All error rate tests are to be performed with a new (unused) diskette.

8. Non-recoverable Read Error Rate

A non-recoverable read error is defined to be a read error which cannot be corrected after three attempts to read the record in error. The non-recoverable read error rate is less than one error per 10^{12} bits read. Errors caused by the diskette (i.e., due to surface flaws, etc.) shall not be included in the computation of the non-recoverable read error rate.

F. Data Addressing at Track Locations

The diskette drive is designed to locate data at the 77 defined tracks on the initialized surface of a diskette. Recorded tracks after tunnel erasure are 0.012" on 0.021" centers. The 77 tracks are numbered from ØØ for the outermost track to 76 for the innermost track. Track centerline is defined by the formula:

centerline radius = 2.029" + (76-N)/48"
±(tolerance)"

where N is the physical track number.

G. MTBF, MTTR: (See Section 6, Maintenance.)

2.3.6 SAFETY REQUIREMENTS

A. Interlocks

An interlock indicating that a diskette has been properly mounted in the diskette drive is provided for each individual unit within the dual drive. This interlock inhibits operation of the spindle motor and generation of the Ready interface signal when diskettes are not properly mounted in the diskette drive.

B. Heat Dissipation

Nominal heat dissipation for the all-DC-power diskette drive is 109 BTU per hour. Average operating power is 28 watts.

2.3.7 INTERFACE CONNECTORS

Within the configuration of a diskette system, all diskette drives are connected to the controller through a signal connector, either directly or by cabling routed in parallel to other diskette drives. Power is supplied to each diskette drive through a separate power connector.

A. Signal Interface

(For names and descriptions of signals, see Section 7, Theory of Operation.)

The signal connector of the first diskette drive in a diskette system is connected directly to the controller through a 50-conductor flat cable, or through a cable consisting of twenty-five twisted wire pairs. The signal connectors of subsequent diskette drives are connected in parallel with the signal connector of the first diskette drive through similar cables.

All signal lines should have a maximum length of 20 feet, and shall use a wire diameter equivalent to AWG #30 or larger.

B. Power and Interface Pin Connections

(See Section 7, Theory of Operation.)

C. DC Power to Diskette Drives

All DC power lines shall have lengths and wire diameters consistent with meeting the power regulation requirements of the diskette drive, as specified in Paragraph 2.3.4.

Eight lines are used to transmit DC power from the power supply through a separate power connector for each drive. One line pair (high and ground) is used for +5 VDC, one for +5 VDC unregulated, one for +24 VDC, and one for -5 VDC. In addition, a separate single line is available to connect drive and power supply chassis grounds.

Five-foot lengths of #18 AWG wire are normally acceptable for use as DC power lines between the drive and typical power sources.

2.3.8 INTERFACE REQUIREMENTS

A. Power-on Sequence

DC power levels may be applied in any sequence to the diskette drive without causing damage to the drive unit.

B. Power-off Sequence

Power levels may be removed in any sequence from the diskette drive without causing damage to the drive.

C. Data Access and Transfer

The timing inter-relationship during head positioning, head selection, and data transfer satisfies the following criteria and remains within the tolerances specified below:

1. Diskette spindle speed: 360 ±12 rpm.
2. Maximum head positioning time for an adjacent rack seek: 10 ms.
3. Maximum head positioning time for a 76-track seek: 100 ms.
4. Average rotational latency: 83.3 ms.
5. Maximum motor start time: 1 sec.
6. Radial dimensions of recording tracks: 3.612" for track ØØ, 2.029" for track 76.
7. Separation between the read/write gap and the trailing erase gap: 0.035 ± 0.002".
8. Index pulse interval time: 166.7 ± 3.3 ms.
9. Read data cell time: 4.0 µs ± 4%.
10. Write clock pulse to write data pulse: 2.0 µs ± 0.3%.
11. Width of Read, Separated Data, and Separated Clock pulses: 200 ns ± 20%.
12. Write data frequency: 249.7 kHz ± 0.3%.
13. Head load time: 40 ms maximum.
14. Erase gate turn-on: 210 ± 8 µs after leading edge of Write Gate (internal drive timing).

15. Erase gate turn-off: 518 ± 10 µs after trailing edge of Write Gate (internal drive timing).

16. Maximum rise and fall time of interface pulses: 25 ns.

17. Phase-locked oscillator acquisition (lock-up) requirement is 4 bytes of all zeroes data.

18. Separated clock contains only those clocks that were written on the diskette.

19. Write current amplitude automatically switched by internal drive logic between Tracks 43 and 44.

20. Restore is a low-speed head positioning operation to Track ØØ. Completion of the Restore command is indicated by a negative level on the Seek Complete interface line.

21. Track position incrementing of the Track Difference Buffer Register in the drive is initiated by the positive-going (trailing) edge of the internal track detent pulse.

22. The Direction Select line shall be stable for a minimum of 100 ns prior to the leading edge of the Step pulse(s).

23. The entire pulse train on the Step line representative of a multi-track address change (one pulse per track) must be transmitted in less than 2.0 ms, at pulse recurrent frequencies of up to 500 kHz.

2.4 DISKETTE (For care and handling of diskettes, see Section 4.3.)

2.4.1 PHYSICAL

A. Type

Compatible to Dysan Part No. 101, having 32 sector holes and one index hole. Compatible diskettes are manufactured by Maxell.

B. Wearlife

200 hours of use on one track.

C. Dimensions

Inner Disk:	19.8 cm diameter (7.8")
Protective Jacket:	20.32 cm square (8")
Index Holes:	.025 cm (.01")

2.4.2 ENVIRONMENTAL

A. Temperature and Humidity

1. Operating

(See System Environmental, 2.1.2.)

2. Storage (Non-operating)

a. Range: 4°C to 53°C (40°F to 127°F).

b. Relative Humidity: 8% to 80%.

c. Max. Wet Bulb Temperature: 29°C (85°F).

3. Transportation

(Diskette in its envelope and in a protective box)

Range: -40°C to 53°C (-40 to 127°F).

Relative Humidity: 8 to 80%.

B. Ambient Air

Clean, dust and particle free air, cool with 50% humidity. No corrosive gases in the air. No colloids such as tobacco smoke.

CONTENTS

SECTION 3 UNPACKING AND ASSEMBLY TIPS

SECTION 3 UNPACKING AND ASSEMBLY TIPS

3.0 INTRODUCTION

This section contains information you may need from time to time for making hardware modifications and updates to your Helios. It includes PCB and IC handling, soldered and PCB modifying tips.

Instructions for hardware changes are in the form of Change Notices which are contained in Section 10, Updates. From time to time additional Change Notices may be sent to you.

Also, in this section are instructions for re-assembling the Helios II after special cleaning procedures in Section 6, Maintenance.

3.1 UNPACKING

1. Choose a clear, clean, flat area to unpack.

2. Inspect for shipping damage. If damage is detected, contact the carrier and Processor Technology immediately.

3. Do not pull the cardboard dummy diskettes out of the diskette slots. Wait until you have read Section 4, Operating Instructions. The cardboard must be ejected by the drive when AC power is applied.

4. Check the contents of the shipment against the following list and the packing list. If an item is missing, notify Processor Technology.

   a. Helios II cabinet(s) with 2 keys.
   b. Controller PCB.
   c. Formatter PCB.
   d. Cable Assembly, Controller/Formatter.
   e. Cable Assembly, Controller/Cabinet(s).
   f. Helios II Disk Memory System Manual (this Manual).
   g. PTDOS User's Guide software manual
      (in this binder, behind the white cardboard divider).
   h. Diskette, containing PTDOS.
   i. Diskette, blank.
   j. Cassette, Disk System Test.

NOTE: If you have purchased a computer system containing one or more Helios II cabinets, compare the contents of the shipment package(s) against the packing list instead of the above list.

There should also be an accessories price list and a warranty card in the binder of the manual.

5. Fill out the warranty card and mail it to Processor Technology.

6. When you are unpacked, go to Section 4, Operating Instructions.

3.2 ASSEMBLY TIPS

3.2.1 PRINTED CIRCUIT BOARDS

A. ORIENTATION OF PCBs
(Refer to the PCB Assembly drawings in Section 8, Drawings.)

Orient the PCB with the component side up, lying flat on the work bench, so that the printed matter on the component side is in normal reading position. The printed matter is called the legend. The legend contains the silkscreened component layout lines and the component identification words and numbers. The components are soldered in place over their respective outlines. There may or may not be traces on the component side in addition to the components. This side of the PCB is referred to as the "component side" or the "legend side."

The opposite surface of a PCB has trace circuits etched on it and is called the "trace side," or "circuit side," or "solder side." It is characterized by a lack of components and by the points of the component lead wires protruding above its surface (when assembled).

B. IDENTIFYING REVISION LEVELS OF ASSEMBLIES

1. Assembly Number

This number is marked on the component side of the PCB, either silkscreened as part of the legend or etched as part of the conductor pattern if a legend is not used. Example: "ASSY 123456 REV..." The revision level is marked separately and is not part of the silkscreen or etching. "Assembly" means the board is assembled with components to a certain configuration. The same schematic may be used for different assemblies or revision levels.

2. PC Number

This number (with Rev. letter) is etched on the solder side (trace side) of the PCB. Example: "PC 123456 REV X." This PC number gives the part number and revision level of the bare board.

3.2.2 DIP SOCKETS

There are two sizes: 14 and 16-pin. The correct size is indicated by the size of the legend on the component side of the PCB.

A. Orientation of DIP Sockets

Orient each socket with its end notch or #1 end matching the colored dot on the legend. The pin #1 end is indicated by the lower right-hand corner being filled in on an angle. Occasionally, the #1 pin end of a socket is indicated instead by a notch in the side of the socket. (See Figure 3-1, DIP Sockets.)

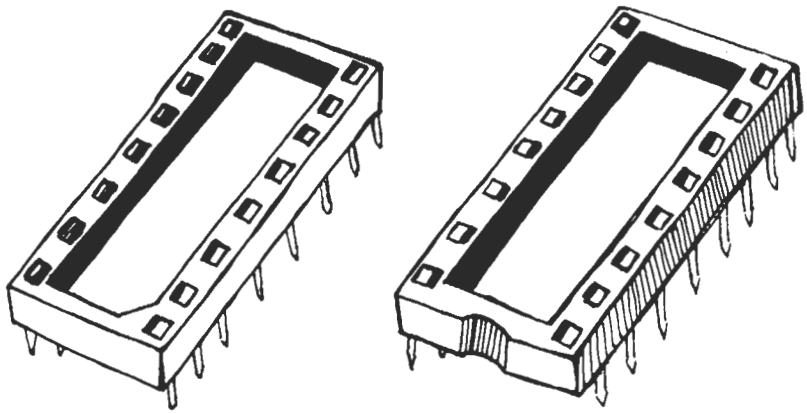


Figure 3-1, DIP Sockets

B. DIP Socket Installation Tip

1. Insert socket pins into the mounting pads at the appropriate location.
2. While pressing the socket in place to ensure that is is fully seated, on back (solder) side of board, bend pins at opposite corners of socket (e.g., pins 1 and 9 on a 16-pin socket) outward until they are at a 45° angle to the board surface. This secures the socket until it is soldered.
3. Repeat this procedure with each socket until all are secured to the board.
4. Solder the unbent pins on the trace side.
5. Straighten the bent pins and solder. Do not solder bent pins since that may cause solder bridges.

3.2.3 INTEGRATED CIRCUITS

> CAUTION
>
> Installing and Removing Integrated Circuits*
>
> NEVER install or remove integrated circuits when power is applied to the Helios II. To do so can damage the ICs.

*There are no MOS ICs on Helios PCBs.

A. ORIENTATION OF ICs AND SOCKETS

Orient the IC so that the number one pin is in the lower right hand corner. The pin number one position is indicated by a dot or small hole embossed into the lower right hand corner or by a notch molded into the IC on the lower edge when the IC is properly oriented. The assembly drawing and the legend both show the notch in the lower edge of the IC and a dot on the PCB in front of the outline of the IC socket. (See Figure 3-2, "Integrated Circuits.")

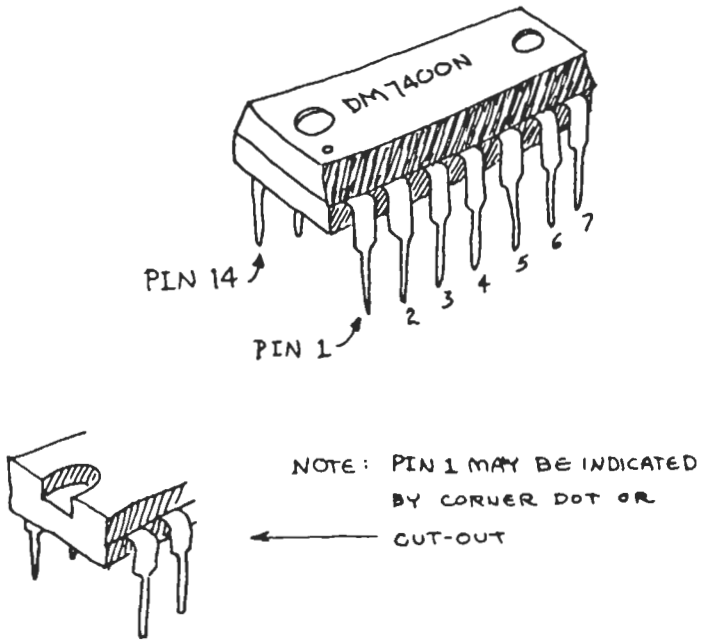


Figure 3-2, Integrated Circuits

B. LOADING ICs

Many DIP devices have their leads spread so that they may not be inserted directly into their sockets. They must be "walked in" using the following procedure.

Insert the pins from one row only into the socket until they barely engage. Push the device using both hands with even pressure to bend this first row of pins until the second row of pins lines up with the holes in the socket, then push the second row of pins into the socket. After all ICs are inserted, examine each to make sure that no pins are bent out or under. Careful examination might prevent hours of unnecessary troubleshooting later.

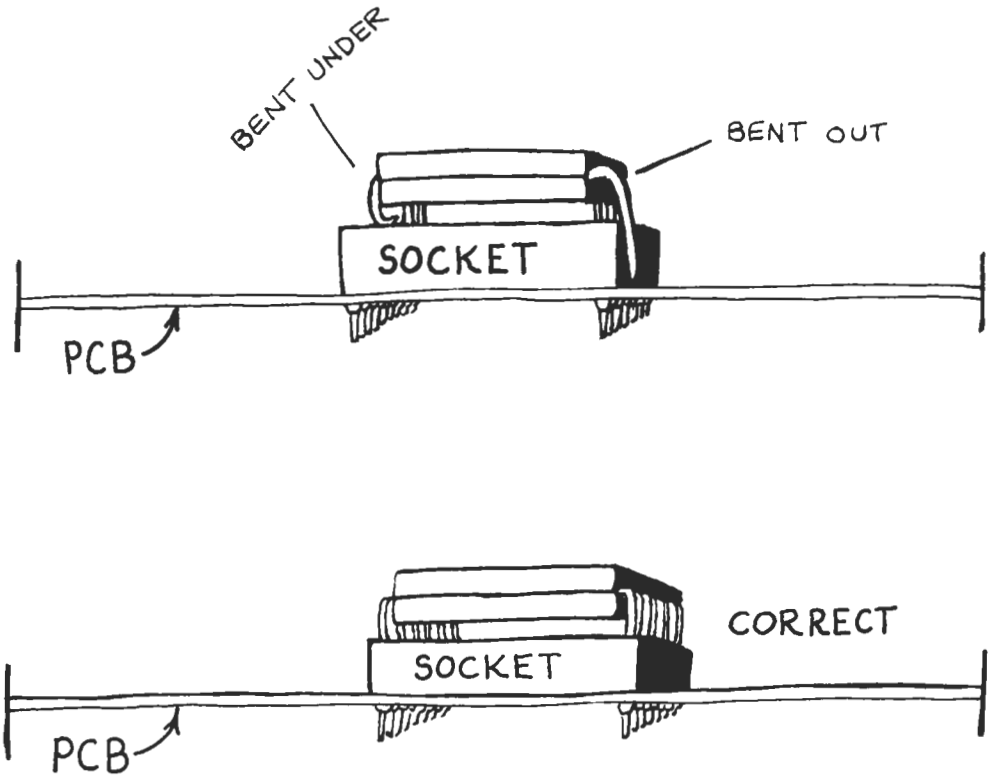


Figure 3-3, Checking IC Pins

3.2.4 SOLDERING

1. Use a low-wattage iron with a small screwdriver pointed tip, 25 watts maximum on the formatter, controller, and indicator panel PCBs. A higher wattage may be used on the regulator board.

   Larger irons run the risk of burning the printed-circuit board. Don't try to use a soldering gun, they are too hot.

2. To make a good solder joint the iron must be clean. Keep a damp piece of sponge by the iron and wipe the tip on it before using it and after each use.

3. Use only 60-40 rosin-core solder. NEVER use acid-core solder or externally applied fluxes. Use the smallest diameter solder you can get.

4. To solder, wipe the tip, apply a light coating of new solder to it, and apply the tip to both parts of the joint, that is, both the component lead and the printed-circuit pad. Apply the solder against the lead and pad being heated, but not directly to the tip of the iron. Thus, when the solder melts the rest of the joint will be hot enough for the solder to "take," (i.e., form a capillary film).

5. Always heat both parts that are to be soldered, preferably at their junction. Use a very light touch. Pressing the

tip of the iron too hard on pad or trace can cause the pad or trace to lift off the board and permanently damage the board.

6. Apply solder for a second or two, then remove the solder and keep the iron tip on the joint. The rosin will bubble out. Allow about three or four bubbles, but don't keep the tip applied for more than ten seconds.

7. Solder neatly and as quickly as possible. Wipe residual flux off the soldering iron with a damp sponge.

8. Solder Bridges

   Solder should follow the contours of the original joint. A blob or lump may well be a solder bridge, where enough solder has been built upon one conductor to overflow and "take" on the adjacent conductor. This causes a short circuit. Due to capillary action, these solder bridges look very neat, but they are a constant source of trouble when boards of a high trace density are being soldered.

   The Helios II uses circuit boards with plated-through holes. Solder flow through to the component (front) side of the board can produce solder bridges. After soldering each group of components, clean the soldered parts immediately and then check for such bridges.

   A few minutes of careful inspection at this time may prevent damage to components and hours of troubleshooting later. The best time to inspect for solder bridges is immediately after soldering; otherwise, time will be wasted going back to find the soldered areas with the possibility of overlooking or forgetting them.

   To remove solder bridges, it is best to use a vacuum "solder puller" if one is available. If not, the bridge can be reheated with the iron and the excess solder "pulled" with the tip along the printed circuit traces until the lump of solder becomes thin enough to break the bridge. Braid-type solder remover, which causes the solder to "wick up" away from the joint when applied to melted solder, may also be used.

9. The Helios II circuit boards have integral solder masks (lacquer coating); masks shield selected areas on the boards and minimize the chances of creating solder bridges during assembly. Do not put masking tape over the traces. When the masking tape is removed, it can tear off the solder mask.

SOLDER CLEANING INSTRUCTIONS

A. Select the following materials:

   a. Solder flux remover (kester).

   b. Flux (Acid) Brush (Cut off bristles of a tooth brush to 3/8 inch to make a cleaning brush).

   c. Paper towels (small Kimwipes are recommended).

B. Put flux remover on the area to be cleaned and scrub the area with the cleaning brush.

C. Put the paper towel over the scrubbed area.

D. Brush the back side of the paper towel.

E. Lift off paper towel and discard.

3.3 MODIFYING PCBs

3.3.1 TOOLS AND MATERIALS REQUIRED

1. Exacto knife.
2. Soldering iron and solder.
3. #24 insulated, solid jumper wire.
4. Magnifying glass.

3.3.2 LOCATING IC PINS

1. Orient the PCB as in section 3.2.1, Orientation of PCBs.
2. Put your finger on pin-1 of the device called for in the instructions; for example, U23-14 (IC 23, pin-14).
3. Keeping your finger at the place, flip the PCB over by twisting your wrist horizontally so that the trace side faces up and the Rev level of the board is in normal reading position.
4. Note to which pin lead or pad your finger is pointing at on the other side of the PCB. Pin-1 on the trace side is square; other pin pads are round.
5. Count the pins clockwise to arrive at the pin called for by the instructions. (The pins are counted counterclockwise on the legend side.)

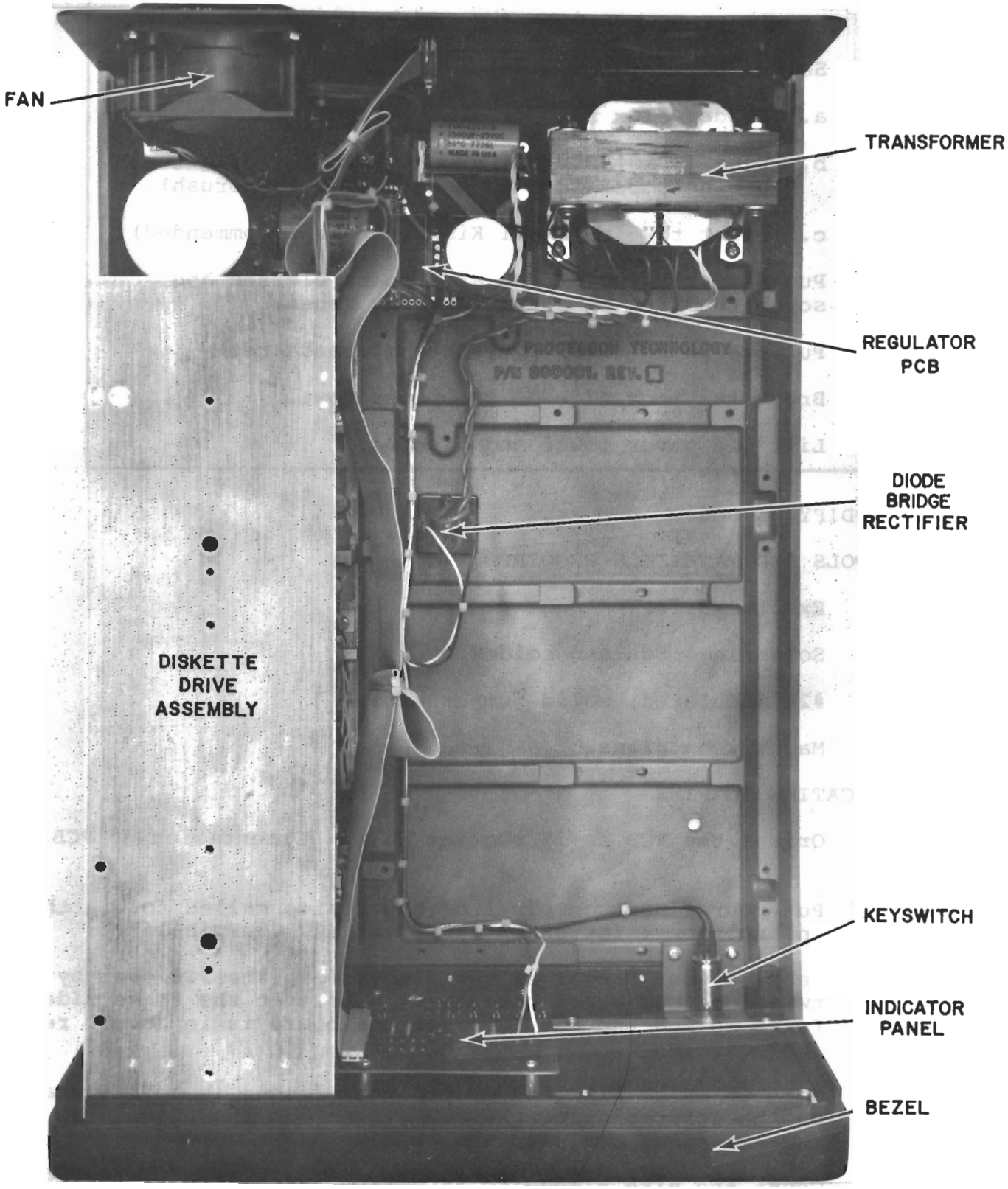


Figure 3-4 Helios II Diskette Drive Cabinet, Inside Top View

3.3.3 TO CUT A TRACE

1. Make two cuts between 1/32 and 1/16 inch apart.
2. Lift up the trace between the cuts with an exacto knife. (Sometimes space will not permit this.)
3. Inspect with a magnifying glass to be sure all copper has been removed.

> **NOTE**
>
> All trace cuts are to be made on the trace side of the PCB unless otherwise specified.

3.3.4 TO INSTALL A SOLDER BRIDGE

To solder a solder bridge onto a trace, first scrape off the solder mask so that the solder will adhere.

3.3.5 CHECK AFTER MODS

1. After you have soldered a connection, clean and inspect for solder bridges.
2. Check the modifications made by reversing the procedure in "Locating IC Pins;" that is, orient the PCB with the trace side up (where the mods are usually made); then put your finger on the connection; count the pin number, flip the PCB over and verify the device designation.

3.4 RE-INSTALLING THE DISKETTE DRIVE ASSEMBLY

(Refer to the exploded views of the cabinet, base, and bezel assemblies, Figures 8-2, 8-3, and 8-4, respectively.)

1. Choose a clean and uncluttered area to install the drive assembly. Optical and mechanical systems within the disk drive unit are particularly susceptible to dust and dirt accumulating especially when the top cover is removed; the working area should be thoroughly cleaned and kept clean while the drive is being installed.

> **CAUTION**
>
> Avoid handling the drive unit by its inner components; pick it up by its outer chassis only. Alignment of these components is critical. Do not touch them unnecessarily with the hand or tools. This is especially the case with the positioner mechanism.

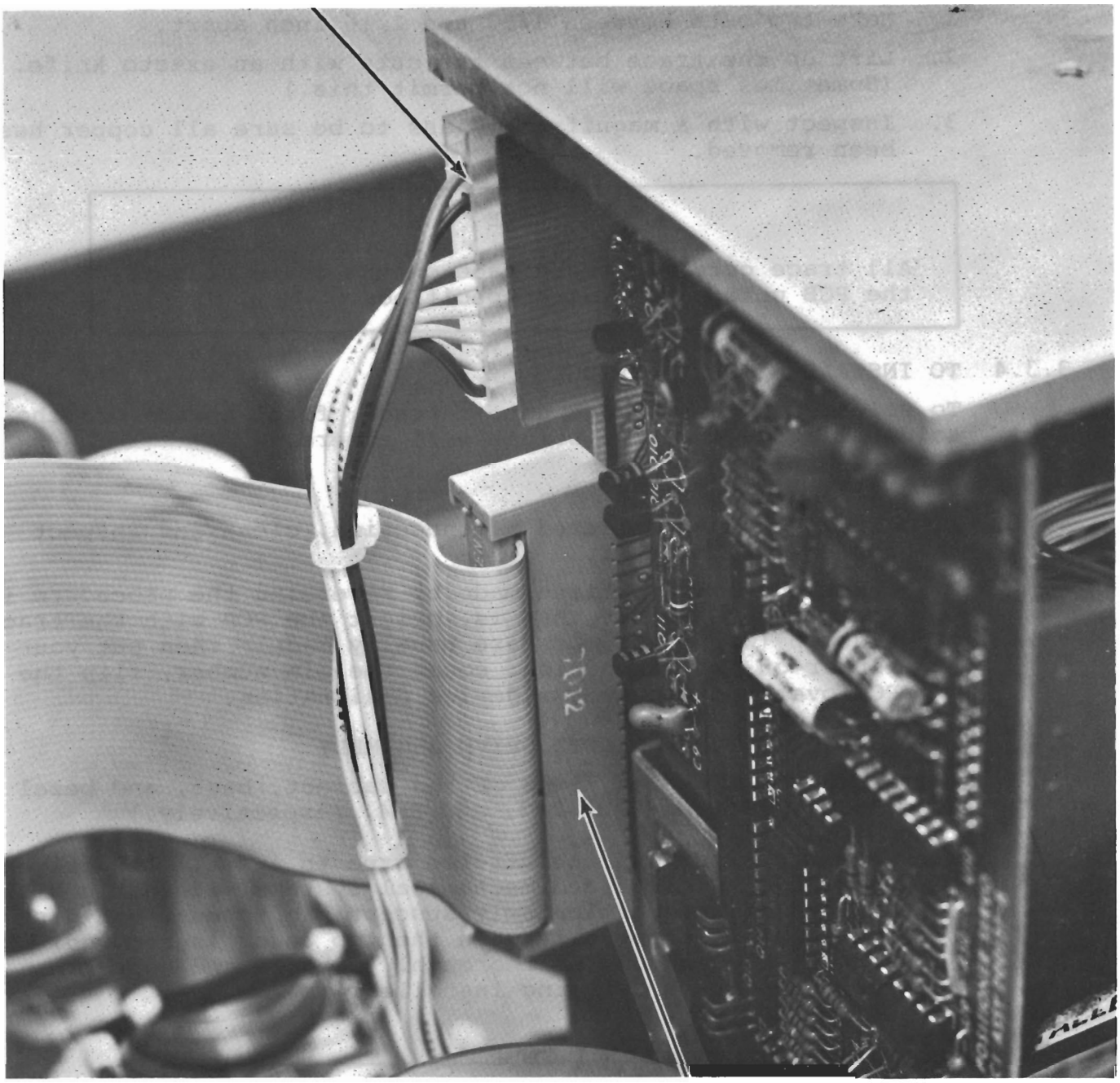


Fig. 3-5. Disk Drive DC Power and Signal Connectors

2. Select the Helios II bezel assembly and install the disk drive to bezel using two 8-32 x 1 inch cap screws. Do not tighten at this time.

3. Reinstall the pushbutton switches on the bezel as follows:

   a. Insert switch into hole provided on bezel.

   b. Attach and tighten the internal tooth lockwashers and hexnuts over the stems of the switches.

   c. Push-back-on the pushbutton covers.

4. Mount the drive assembly to the base assembly using four 8 x 32 x 5/8 inch screws, four #8 internal lockwashers; tighten the screws

5. Make sure the #8 cap screws (step 2) are still untightened at this time.

6. Attaching Bezel to Base

   (Refer to Fig. 8-2, Cabinet Assembly, Exploded.)

   a. Install three 6-32 x 7/16 inch screws and three #6 internal lockwashers from the bottom of the base into the bezel.

   b. Install one 6-32 x 1/2 inch screw and one internal lockwasher on the keyswitch side of the bezel into the base.

   c. Now tighten the two #8 cap screws which attach the bezel assembly to the drive assembly (installed in step 2).

7. Ensure that all screws are tight.

8. Connect the 10-pin plug connector from the power supply wiring harness to J3 of the rear of the disk drive unit. One of the pins is removed from J3 and a polarizing plug is inserted in the mating plug hole so that 10-pin plug connector can go on only one way. (See Fig. 3-5, Diskette Drive DC Power and Signal Connectors.)

9. Connect the flat 50-conductor signal cable (Signal/Indicator Panel Cable Assembly) from the indicator panel PCB to the disk drive at P1. P1 is an edge connector on the PCB* protruding its short edge at the rear of the drive assembly. The pin-1 end of the plug connector (indicated by the colored stripe on the pin-1 edge of the cable) goes on at the bottom of the mating PCB edge connector P1. Pin-2 is designated on the PCB legend at this end and pin-50 on the opposite end. (See Fig. 3-5, Disk Drive DC Power and Signal Connectors.)

*Data and Interface PCB.

10. Install the top cover on the drive cabinet. Using three 6 x 32 x 1/4 inch screws, attach the rear panel to the cover.

3.5 OPTIONAL DC POWER FOR FORMATTER PCB

The formatter PCB receives only DC power through the S-100 edge-connector. Instead of plugging the formatter into a S-100 backplane connector, when the connector would otherwise be useful, power may be supplied through P2. The connector, J2, which mates with P2 is specified in Section 2, Specifications.* It is not supplied in Helios II system.

To supply power through P2:

1. Apply +8 volts on pin 3 (center pin).

2. Ground on pins 1 and/or 5.

*Since the voltages are arranged symmetrically around the center pin, the plug is non-polarized. The jack which mates with P2 may be oriented either way.

CONTENTS

SECTION 4 OPERATING INSTRUCTIONS

Fig. 4-1 Helios II Front Panel

SECTION 4 OPERATING INSTRUCTIONS

4.0 INTRODUCTION

The Helios II should not be loaded with the PTDOS program until the Disk System Test in Section 5, "Testing and Trouble-shooting" is performed; however, this entire section should be read before performing the tests in Section 5.

This section builds up to the actual operating instructions rather than jumping into them. The operator must be adequately prepared with information and understand the relative importance of the elements in the system. For example, the care and handling of the diskette is critical in a floppy disk system. Special terminology used in this system must be defined. The sequence of steps is often as important as the steps themselves. Please read each section in the sequence given. Of course, when you become familiar with the content, the sections can be referenced as needed.

These instructions are aimed primarily at the operation of the system hardware with some references to disk operating system. Instructions for the software are in the PTDOS User's Guide, also contained in this binder.

4.1 SYSTEM REQUIREMENTS

1. Helios II tested as per Section 5, Testing and Trouble-shooting.
2. Host computer (S-100 bus compatible), preferably a Sol-20.*
3. 16 kilobytes of RAM memory (minimum) configured as follows:

   4K: ØØØØH to 3FFFH

   12K: 9ØØØH to BFFFH
4. Video monitor or black and white TV converted for video input. (For TV conversion instructions, see Sol Systems Manual, Appendices, or VDM-1 Video Display Module Assembly and Test Instructions (PTC).
5. PTDOS program on diskette; a blank diskette.
6. Disk System Test (cassette).
7. BOOTLOAD program in either of three forms:
   a. P.T. BOOTLOAD Personality Module.
   b. BOOTLOAD as recorded on the front of the Disk System Test cassette (item 6 above). This requires a Sol or a host computer with CUTS interface and CUTER monitor.
   c. BOOTLOAD listing. (Refer to PTDOS User's Guide, Section 8, Appendix B, "Getting Started with PTDOS.")
8. Helios II Disk Memory System Manual, including the PTDOS User's Guide.

*This section is oriented primarily with the assumption that the Helios is associated with a Processor Technology Sol system.

4.2 TERMINOLOGY, NUMBERING, AND CONFIGURATION

The terms used in this manual in relation to the drive configurations are illustrated in Figure 4-2 "Helios System Terminology."

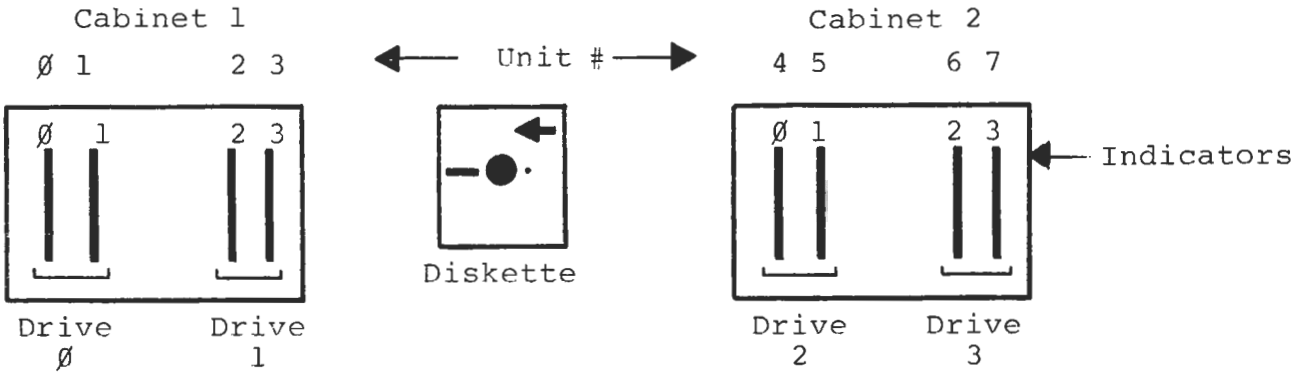


Figure 4-2 Helios System Terminology

(Model 2 contains only drive Ø, units Ø and 1. See 4.2.2 , Multi-Drive System Configuration.)

4.2.1 HELIOS TERMS (Refer to Fig. 4-2)

CABINET	The enclosure containing one or two dual drives.
DRIVE	The dual drive assembly; containing 2 slots to accept diskettes.
UNIT	The individual diskette slot with its accompanying drive mechanism, numbered by counting all the slots in the system (from Ø up to 7 inclusive).
SELECTED UNIT	The unit in the system selected by the PTDOS and indicated by the light on one of the indicator panels in the system (Ø up to 7 inclusive).
INDICATED UNIT	The individual diskette slot numbered by counting only the slots within a given cabinet. (Ø up to 3 inclusive).
DISKETTE	The floppy disk recording medium.

4.2.2 MULTI-DRIVE SYSTEM CONFIGURATION

A. Placement of Terminator Resistors

Four dual diskette drives can be operated with signal connectors in parallel on one signal cable (daisy chain). In a multi-drive system, the terminator resistor pack, which can occupy U1 on the drive Data and Interface PCB, must be installed only in the drive farthest electrically from the controller. All the other drives must have U1 vacant.

Similarly, resistors R12 through R15 on the indicator panel PCB must be installed only in the drive cabinet further electrically from the controller and must be removed from the board in the cabinet closer to the controller.

B. Selector DIP (Refer to Fig. 8-15, Selector DIPS ...)

The Helios system is capable of accommodating up to 8 units, as shown in Figure 4-2. Model 2 contains two units only. In systems containing more than two units, each pair of units must be able to identify itself to PTDOS as being units Ø-1, 2-3, 4-5, or 6-7.

On the large PCB on the right side of each drive (Data and Interface PCB) is a DIP socket, U11, which can receive a DIP device called a Selector. The Selector performs the unit identification function. If you are using the Model 2 alone, it is recommended that you do install the Selector if supplied with the unit (even though it will be non-functional), as a means of safe-keeping it. If Selector Ø-1 is not installed, the drive will respond to calls from the software to any unit, Ø through 7. If you add additional drives, install Selector Ø-1 in the left-hand drive (drive Ø of cabinet 1). Make sure the pin 1 designation on the Selector is aligned with the pin 1 designation on the socket U11, as with an ordinary IC.

Additional Selectors designated 2-3, 4-5, and 6-7 are available. If a second drive is added in the same cabinet, install a Selector 2-3 in it. The left-hand drive in a second cabinet should receive Selector 4-5 whether or not the first cabinet has a second drive identified 2-3. The right-hand drive in a second cabinet should receive Selector 6-7. This arrangement of unit identification is shown in Figure 4-2, "Helios System Terminology."

Refer to 7.12.2, E, Parallel Operation and Unit Selection for more information.

4.3 CARE AND USE OF DISKETTES

> NOTE:
>
> Use only Dysan diskettes (Dysan Part No. 101) or an approved equivalent such as Maxell. This diskette must have 32 sector holes (plus one index hole), which are visible through the small hole near the spindle hole.

4.3.1 PRELIMINARY HANDLING TIPS

The floppy disk diskette is a precision component and must be handled with reasonable care to avoid damage or accidental erasure. Proper care will assure longer life and greater reliability. The main concerns are dirt, foreign matter, mechanical damage, magnetic fields, and heat.

1. Store the diskette in its protective envelope at all times when not in use. Store in a vertical position. Store in a cool, dry place, out of direct sunlight. Do not leave it in a car or near sources of heat.

2. Do not bend or crease the diskette. Handle carefully, and never touch the area inside the rectangular window, or the magnetic surface containing the tracks inside the circular window. Fingerprints can destroy data and prevent the diskette from being written on.

3. Insert and remove the diskette from the drive carefully and gently.

4. Protect the area of the diskette which is exposed on both sides, through the area of the window, from contact with hands or other objects. A small crease from a fingernail or sharp object can render the diskette useless.

5. Avoid exposure to magnetic fields from magnets, transformers, etc. Avoid contact with all ferrous metals. Common tools, such as screwdrivers, often have megnetized tips which can erase valuable information stored on the diskette.

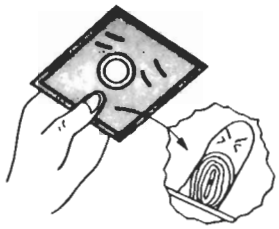
..3.2 LOADING AND UNLOADING THE DISKETTE

> CAUTION
>
> Do not execute the procedures in this section using a recorded diskette. You may practice using a blank diskette. This section is primarily for you to remember when you get to the operating instructions, Section 4.7.

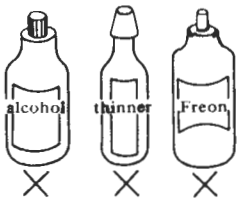
FLOPPY DISK HANDLING AND STORAGE

Handling precautions to protect against possible failure

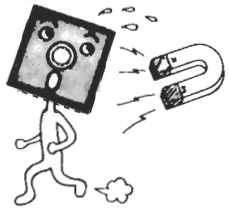
1. Do not touch the disk surface. Easily contaminated, and causes errors.



2. Do not use solutions: alcohol, thinner, Freon, to clean the disk.

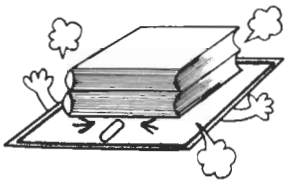


3. Do not use magnets or magnetized objects near the disk.
Data can be lost from a disk when exposed to a magnetic field.

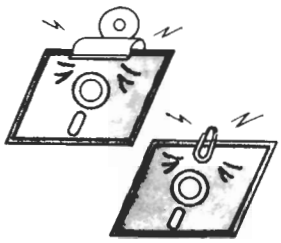


4. Do not bend or fold the disk.

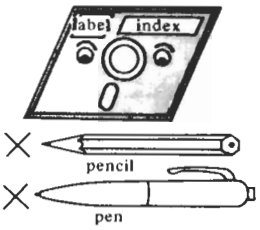
5. Do not place heavy objects on the disk.



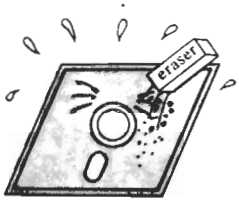
6. Do not use rubber bands or paper clips on the disk.



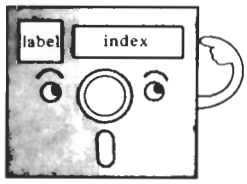
7. Do not write on a disk label with a pencil or a ball-point pen.
Use a fiber-tip.



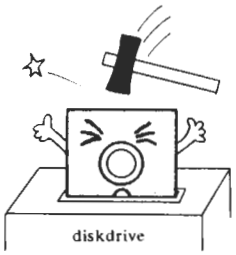
8. Do not use erasers.



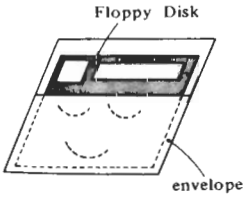
9. Put I. D. labels in a right place, never use them in layers.



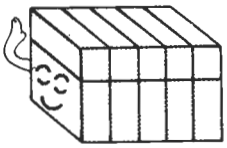
10. Insert carefully, by grasping upper edge and placing it into the drive.



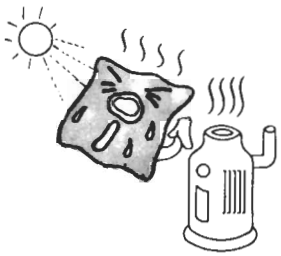
11. Keep disk in its envelope.



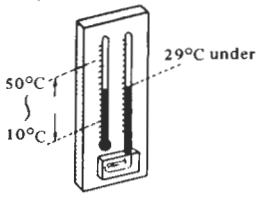
12. Store disk not for immediate use in their box, and set it up.



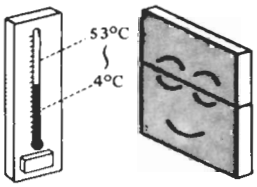
13. Do not expose the disk to excessive heat or sunlight.



14. Operating environment
10°C to 50°C (50°F to 122°F)
20% to 80% RH
less than 29°C (Wet bulb temperature)



15. Storage environment
4°C to 53°C (40°F to 127°F)
8% to 80% RH



16. Transportation
During transportation the disk shall be in its envelope, and in a protective box.
Temperature: −40°C to 53°C (−40°F to 127°F)
Relative humidity: 8% to 90% RH

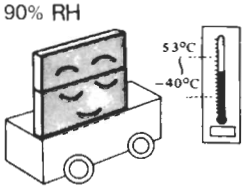


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Fig. 4-3 Floppy Disk Handling And Storage

DISKETTE CAUTIONS

A. Do not attempt to insert a diskette with the power to the drive turned OFF. Acceptance of the diskette by the drive is motorized.

B. Do not turn the drive power OFF with a diskette in the slot. Eject the diskette(s) before power-down.

C. Do not turn the computer power OFF with a diskette still in a slot. Eject the diskettes before computer power-down.

D. Do not try to pull out the diskette manually with the power to the drive turned off. The ejection of the diskette is motorized.

E. Do not run the drive with one diskette in and one ejected. Fully remove the ejected diskette. Otherwise, the revolving hub for the ejected unit may wear into the ejected or partially removed diskette.

1. The diskette should be approximately the same temperature as the drive while operating. If the diskette has been exposed to temperatures outside the recommended operating conditions given in Section 2, keep it at room temperature for about five minutes before inserting it in the drive.

2. Grasp the diskette on its edge opposite the notched edge (opposite the rectangular window with the rounded edges.) (Refer to Fig. 4-4, Diskette Orientation for Loading.)

3. Hold the diskette vertically on edge so that the label is in the upper right corner (on the left side of the diskette). The large notch should be in the bottom 1/4 of the diskette.

4. The direction of insertion into the diskette aperture is forward from the notched edge.

   Insert the diskette gently into the appropriate slot, until the front edge is flush with the face of the slot. There should be no resistance to the insertion. A sensing device in the drive will automatically close the carrier when the diskette is properly positioned. The drive will grab the diskette and spin it.

   If the diskette is inserted in the wrong orientation, it will cause no damage, but no data can be read or written on the diskette; if PTDOS is loaded, it will report, on the system output device, the error message: "Drive not Ready."

   The heads for both units read or write on the side of the diskette opposite the side with the label. Only this side is tested and initialized by the diskette manufacturer at the present time.

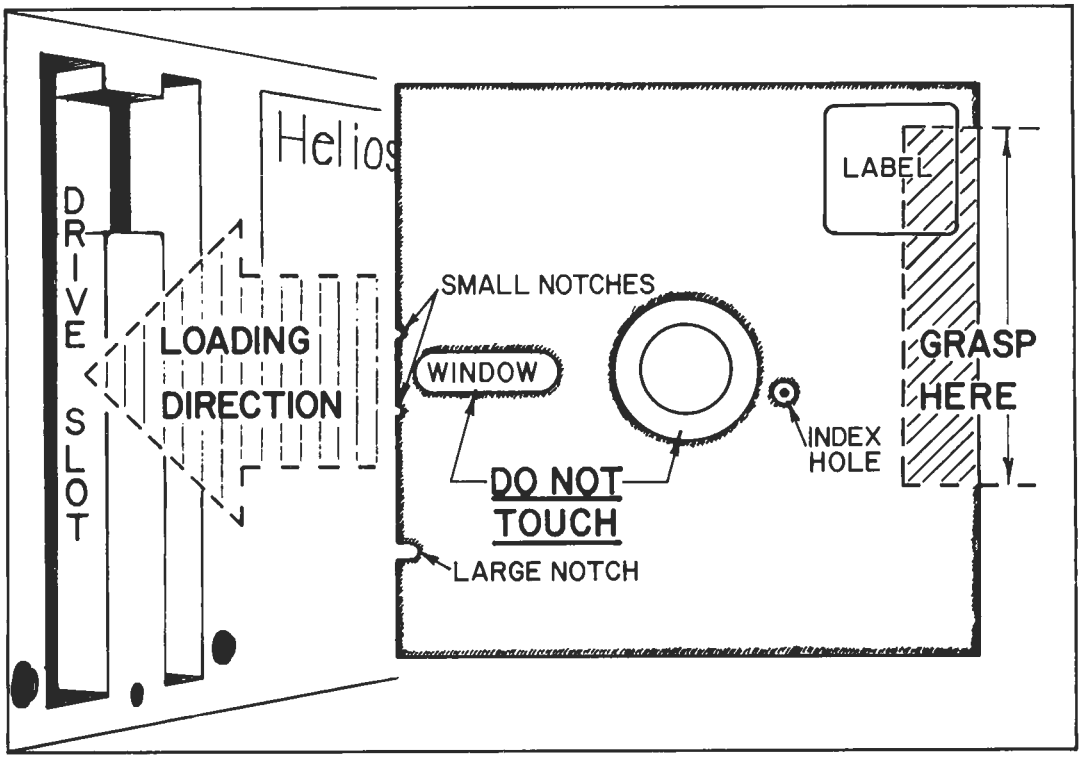


Fig. 4-4 Diskette Orientation for Loading

5. To eject diskette, apply power to the drive, and press the EJECT button next to the slot in which you have inserted the diskette. The diskette should eject automatically to where it can be easily removed from the drive. If the adjoining unit is revolving with a loaded diskette, remove the ejected diskette completely to avoid abrasion.

6. When you leave your Helios idling with power on for more than a few minutes, eject the diskette to save wear and tear on the diskette and the spindle and drive motor. This will also conserve energy.

4.3.3 WRITE PROTECTION

> CAUTION
>
> Helios II diskettes that have data written on them are not protected from being overwritten by the protect label. See explanation in the following paragraph.

The edge of the diskette, diagonally opposite the label, has an oval notch. In some floppy disk systems the diskettes are normally protected from being written upon unless this notch is covered over with a protect label. In the Helios system, the

diskettes are always unprotected mechanically but are protected by program control. Diskettes can be written on whether or not the notch is covered.

4.3.4 DISKETTE COMPATIBILITY WITH OTHER SYSTEMS

Diskettes containing data written by your Helios II may be used in any other Helios II system. Blank diskettes may be used in other floppy disk systems but written diskettes will not be compatible in format with other systems.

4.4 SETUP AND INSTALLATION

1. Assure that the ambient temperature is between 50° and 100°F (10°C to 38°C); room temperature (77°F, 25°C) is recommended.

2. Situate the disk drive unit in the working area so that there is easy access for inserting and removing diskettes.

3. Make sure the fan opening, on the rear panel, is unobstructed, allowing adequate air flow.

4. Assure that the power ON/OFF switches for both the Helios cabinet(s) and the host computer are OFF.

5. Locate a S-100 slot in the computer for the controller PCB. The slot should be located so that the formatter PCB can be plugged into an adjacent or nearby slot and connected with the flat signal cable, and so that the controller PCB can be connected via a flat signal cable to the disk drive. (Refer to Fig. 8-1, System Assembly, Interconnect Diagram.)

   Because of the heat dissipated by the controller PCB and because of the cable connections involved, the top slot (in the Sol) is recommended for the controller PCB and the second slot for the formatter PCB. (Cable connections are described in the following section.)

   Insert the formatter in the second slot (in the Sol) and the controller PCB in the top slot. This will allow for the interconnecting cable to lie flat in the space between the top PCB and the Sol cover.

> CAUTION
>
> Do NOT position the controller and formatter PCBs so that their connecting signal cable must be wedged between two PCBs. This may cause the signal cable to be punctured by the component leads and may also cause the boards to bow outward unless the cable is creased in a particular spot. For proper cable orientation, refer to Fig. 8-1, System Assembly, Interconnect Diagram.

NOTE

The formatter PCB receives only DC power from the S-100 backplane. DC power can also be supplied to the formatter PCB through its 5-pin P2. The formatter PCB, therefore, does not have to be plugged into the computer backplane to function in the Helios II system. Instructions for supplying DC power to the formatter PCB are paragraph 3.5, "Optional DC Power for the Formatter PCB."

4.4.1 CONNECTING THE CABLES

(Refer to Fig. 8-1, System Assembly, Interconnect Diagram.)

CAUTION

Take care to observe the correct polarity of the mating connectors. Triangular arrowheads are molded on matching ends of the connectors to indicate the polarity.

In addition to the arrowhead polarity indicators, there are two other aids in matching the polarity of the connectors. The pin numbers are molded (embossed) along their respective pin jacks on the face of the cable connectors. A colored stripe along one edge of the flat signal cable indicates the pin-1 signal line.

NOTE

The connectors on the ends of the signal cables are designed to mate with the connectors on the formatter and controller PCBs only one way. This is accomplished by the fact that Pin 15 of the P3 jacks on both PCBs are removed. Pin-31 of P2 on the controller PCB and J5 of the drive cabinet are also removed. Tiny polarizing plugs are inserted in the mating female connectors at the corresponding pin numbers.

1. Assure that the controller and formatter PCBs are positioned according to subsection 4.4, "Setup and Installation."

2. Select the controller/formatter interconnect cable (a flat signal cable about 10 inches long.)

   a. Orient the cable lengthwise (left to right) so that the colored stripe is up or away from you.

   b. Connect the left-hand connector to P3 of the formatter PCB, observing the proper pin polarity. The cable should be extending out from P3 (away from the computer). The color stripe should be on the side of the connector which is opposite the heatsink (to the right of the PCB looking from the rear of the Sol.) See Fig. 8-1, System Assembly, Interconnect Diagram.)

3. Observing the same pin polarity, connect the other end of the cable to P3 of the controller PCB, which is recommended to be placed above the formatter PCB.

4. Select from the kit the controller/cabinet signal cable (a flat 50-pin signal cable about 5 ft. long). Plug one end of this cable onto P2 of the controller PCB and the other end onto J5 on the rear panel of the drive cabinet.

5. Assure that both PCBs are securely plugged into the backplane.

6. Fold the loop of the controller/formatter cable down flat on top the controller PCB.

7. Replace the computer's cover.

8. Assure that the AC linecord is plugged into the 3-pin receptacle at the lower right-hand corner of the rear panel of the Helios cabinet.

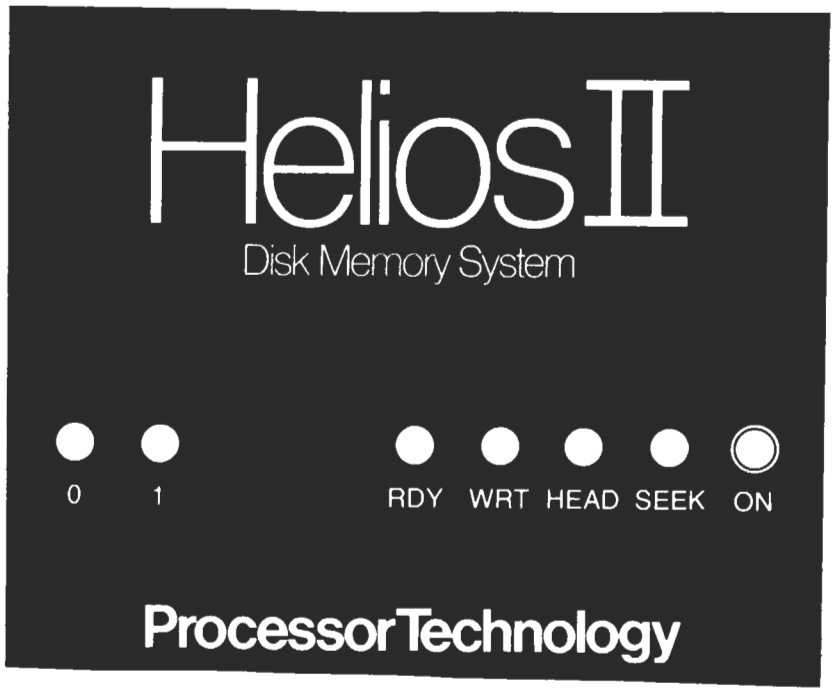


Fig. 4-5 Helios II Indicator Panel, Model 2

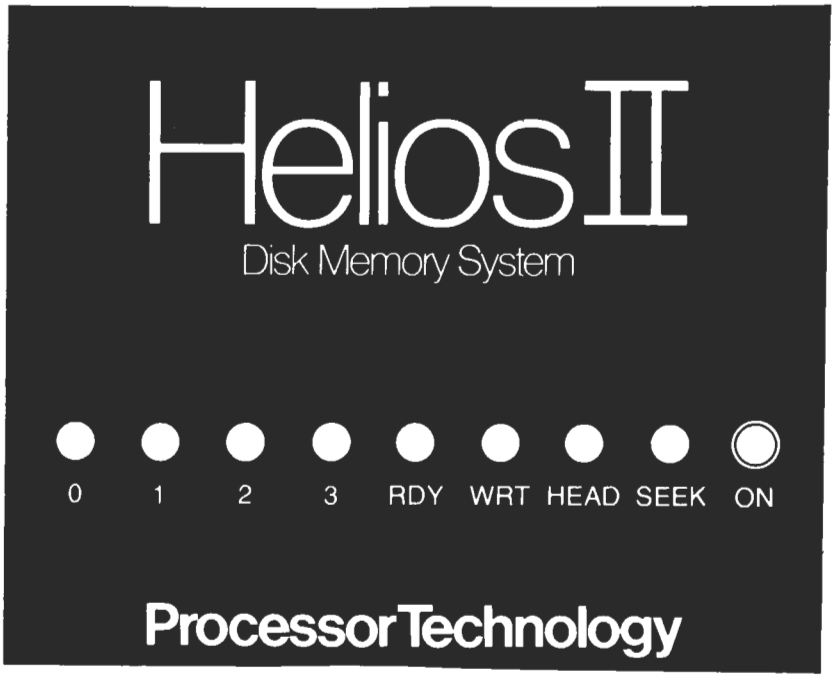


Fig. 4-6 Helios II Indicator Panel, Model 4

4.5 INDICATORS (Refer to Fig. 4-5 and 4-6, Helios II Indicator Panels and Fig. 4-2, Helios System Terminology.)

In the Helios II, Model 2, there are 7 indicator lights on the front panel. They consist of small round windows back-lighted by LED's (Light Emitting Diodes).

LEGEND	POSITION	DESCRIPTION
ON	Far right (Both Models)	The ON LED glows when AC power is applied to the drive and the power key switch is ON.
Ø	Far left (Both Models)	The Ø (zero) LED glows to indicate that the left-hand unit of the left-hand dual drive is selected by the system.
1	Second from left (Both Models)	The 1 (one) LED glows to indicate that the right-hand unit of the left-hand dual drive is selected by the system. Note: the system selects only one unit at a time. Normally unit Ø is ON when the system is initialized. If the system by mistake selects a unit not in your configuration, no indicator will light.
2	Third from left (Model 4)	The 2 LED glows to indicate that the left-hand unit of the right-hand dual drive is selected by the system.
3	Fourth from left (Model 4)	The 3 LED glows to indicate that the right-hand unit of the right-hand dual drive is selected by the system.

ACTION INDICATORS

READY	Fifth from right	The selected unit is ready and its drive is rotating at speed. The diskette is positioned properly.
WRITE	Fourth from right	The system is writing on the diskette.
HEAD	Third from right	The selected head is loaded.
SEEK	Second from right	(SEEK COMPLETE) When the light is OFF, the selected unit is seeking the track requested by the system. When light is ON, the selected unit is on the last track requested.

4.6 CONTROLS

> CAUTION
>
> The Controls sections is to familiarize you with the controls only. For operating instructions, refer to subsection 4.7, "Operating Instructions."

The operator controls the Helios II system primarily through the console keyboard. See the PTDOS User's Manual, in this binder, for keyboard commands. The controls on the front panel of the disk drive cabinet are: key switch and two eject buttons for each dual drive.

KEY SWITCH (Refer to Fig. 4-1 "Helios II Front Panel.")

The key switch locks the AC power to the drive either ON or OFF. Its purpose is to protect the drive from unwanted access by locking the AC power OFF or to preserve power by locking the AC power ON. The key can be removed in either position. Two keys are provided for the lock.

KEY POSITION	FUNCTION
ON	To lock the drive power ON, turn the key clockwise and remove key.
OFF	To lock the drive power OFF, turn the key counterclockwise and remove key.

EJECT BUTTONS

To eject a diskette, hold the appropriate eject button in momentarily, with the power ON.

4.7 OPERATING INSTRUCTIONS

> CAUTION
>
> These instructions assume your Helios II is tested according to Section 5, "Testing and Troubleshooting." The PTDOS program can be erased from the diskette by an untested system. As soon as you have qualified your system according to Section 5 and you are familiar with the system, use the DISKCOPY command to produce a backup diskette, in case the PTDOS program is accidentally erased.

1. Assure the cables are connected as described in subsection 4.4.1, "Connecting the Cables."

2. Turn on AC power to the computer.

3. Turn on AC power to the disk drive using the keyswitch.

4. Initialize the computer operating system (OS). The OS prompt character should appear to indicate the OS is ready.

5. Insert a diskette containing PTDOS in unit Ø. (See instructions in subsection 4.3, "Care and Use of Diskettes."

6. If your computer is a Sol equipped with the BOOTLOAD Personality module (a Helios II accessory), load the PTDOS from the diskette by typing: BO (from SOLOS Command Mode)

   Press: RETURN

> Bootload is a short program which bootstraps a longer bootload program off the diskette. The longer bootload in turn loads the PTDOS itself and transfers control to it. The PTDOS is loaded into RAM in the computer. For the listing and additional information, refer to PTDOS User's Guide, Section 8, Appendix B, "Getting Started with PTDOS."

7. If your computer is other than a Sol, load and execute the program BOOTLOAD from the cassette containing the Disk System Test. Bootload is on the front part of the tape.

   Both BOOTLOAD and the Disk System Test are in CUTS format which requires the CUTS interface module with the CUTER operating system.

8. When PTDOS has been successfully loaded, it presents "PTDOS" on the output device, with the current version number, release date, and other system information. On a second line it presents an asterisk as the prompt character: *

   When presented, the prompt character indicates that the Command Interpreter (CI) program within PTDOS is waiting for a command.

> CAUTION
>
> Do not procede further without completely assimilating PTDOS User's Guide, Section 8, Appendix B, "Getting Started with PTDOS."

NOTES

CONTENTS

SECTION 5 TESTING AND TROUBLE-SHOOTING

CONTENTS (Continued)

SECTION 5 TESTING AND TROUBLE-SHOOTING

5.0 SCOPE OF THIS SECTION

Subsection 5.1, "Introduction," through 5.5, "Controller Transfer/DMA Test/Trouble-shooting Procedure," are concerned with the Disk System Test. The remaining sections contain basic trouble-shooting and electrical checkout procedures.

The Disk System Test subsections are organized as follows:

5.1, "Introduction to the Disk System Test," describes the overall characteristics of the Test. It categorizes its component tests according their uses, shows their inter-relationships, and gives a brief idea of how they are exercised.

5.2, "Disk System Test, Description and Preliminary Instructions," devotes a separate subsection to each test in order to familiarize the user. This subsection can be used as references in time of need during the tests.

5.3, "Disk System Test Requirements and System Configuration," gives the different requirements for both a Sol system and non-Sol systems.

Finally the Operating Instructions for the Test are presented in 5.4. Recommended alternate procedures for the test are given. An annotated printout of the actual test frames is provided.

5.1 INTRODUCTION TO DISK SYSTEM TEST

The Disk System Test is the second program recorded on a cassette supplied with the Helios II.

The Test is divided into 8 parts. These parts are categorized by their two major applications:

1. Qualifying Tests
   - a. Seek Test
   - b. Automatic Write/Read Test

   } Initialize diskette

2. Diagnostic/Trouble-shooting Tests

   (I/O Ports test) → Part 1 - Input/Output Test

   (DMA Circuits test)
   - Part 2 - Controller/DMA Test (Initializes diskette)
   - Part 3 - Header Write Test
   - Part 4 - Header Read Test
   - Part 5 - Data Write Test
   - Part 6 - Data Read Test

5.1.1 QUALIFYING TESTS

Only the Qualifying Tests must be performed on a newly installed system before the diskette containing PTDOS is loaded. Each Helios II system has been completely tested at the factory by a similar test before shipment to the customer. Even so, to protect your PTDOS diskette from possible faults in the system which may have developed during aging, shipping, and handling, the Seek Test and Automatic Write/Read Test should be run before you load the diskette containing PTDOS for the first time.

These two tests should also be performed whenever the system is:

1. Modified, repaired or parts replaced.

2. After preventative maintenance procedures such as the cleaning of the write/read heads.

3. After shipping and/or re-installation.

A system which has not been qualified by these tests may contain an undetected fault which could destroy valuable data or even erase an entire diskette.

A recommended procedure for performing the qualifying tests is given in 5.4.1, Recommended Test Procedures.

A recommended procedure for performing a complete system checkout is given in 5.4.1, Recommended Test Procedures.

5.1.2 DIAGNOSTIC/TROUBLE-SHOOTING TESTS

The diagnostic/trouble-shooting tests, Parts 1 through 6, need be run only if the system has failed to qualify during the Automatic Write/Read Test and Seek Test. Although limited to a certain extent by interdependency, parts 1 through 6 are randomly accessible to provide a flexible trouble-shooting tool. Error handling, repeat, and re-entry options are built into the tests. Parts 3 through 6 may be stepped through manually or run automatically. Within the automatic option there are also various error-handling options.

Part 1 checks the operation of the output ports on the controller PCB. Parts 2 through 6 check the circuits which perform direct memory access (DMA).

5.1.3 S-100 BUS COMPATIBILITY

The Helios II Disk System Test is a SOLOS/CUTER compatible program. This compatibility allows the program to be loaded and run in either a Processor Technology Sol or any other S-100 system which has the CUTER operating system installed. The program is loaded into memory using the XEQ command. The program is controlled through the SOLOS/CUTER console input device.

NOTE:

To aid users who must make I/O patches, a listing of the I/O routines used by the Disk System Test is included in the Appendix, Section 9.

5.2 DISK SYSTEM TEST, DESCRIPTION AND PRELIMINARY INSTRUCTIONS

This subsection contains descriptions of each test. The actual operating instructions are in subsection 5.4. These descriptions do contain some test operating information which can be previewed now and then referred to just before or during the corresponding test.

The first frame of the Disk System Test is the introduction (frame 1). (Refer to the printout of the frame* in the Test Operating Instructions, 5.4.2, Disk System Test Frames.) Typing "P" advances the program to the next frame.

Frame 2 presents a list of entry points to the test program. These are the starting points of the various parts of the test. They enable the user to reach a certain part of the test without stepping through all the preceding parts. This capability is very useful for trouble-shooting. For example, the Automatic Write/Read Test would be entered from this point by typing "A."

The controller cannot write or read data to or from a blank diskette. It must first "initialize" the diskette. Certain tests initialize the diskette as part of the test. Initializing is the function described as "erasing." (Refer to 7.10.2, K, The Erase Function." It is briefly defined as writing a primitive empty format on the diskette. The initializing is done when the test program announces, "Wait a moment while the disk is being erased," as in frame 14. In each of the following test descriptions, a caption reminds you of the prerequisite conditions for the test, such as an initialized diskette or another test. The list of tests in 5.1, Introduction, includes notes as to which of the tests initialize the diskette.

5.2.1 QUALIFYING TESTS, PRELIMINARY INFORMATION

A. Seek Test

(This test initializes a blank diskette.)

This test checks the head positioning function of the drive. The test runs about 5 minutes. If an error occurs, an error message will be displayed. After an error, typing "P" will return to the beginning of the Disk System Test. If no

*A frame is the extent of a page of data presented on the screen of the video monitor at one time, or the corresponding lines printed on the teleprinter; although the two forms of output do not always coincide.

error occurs after 5 minutes, the message "SEEK TEST COMPLETE" will be presented. After this message, typing "P" will return to the start of the Disk System Test.

B. Automatic Write/Read Test

(This test initializes a blank diskette.)

The Automatic Test performs parts 3 through 6 of the Disk System Test, automatically, keeping count of the number of passes through these 4 parts of the test. It also counts errors.

During the automatic tests, the drive first makes one test pass of each track in sequential order, starting from the outside track. When the drive reaches the innermost track, it steps the head at random from track to track to make each pass.

One of four display options can be selected within the automatic test by typing:

D Displays the results of each test part, but takes no special action when an error occurs.

E Displays the results of each test part, and stops and presents the repeat-options when an error occurs.

O Stops and displays only when an error occurs. This option does not present the repeat-options.

N Runs the test with no display until a "G" is typed.

When the automatic test is running, typing a "G" will stop the tests and generate a report as shown in Fig. 5-1, "Automatic Test Report Format." The report indicates the number of passes through the test parts, the number of errors encountered, and whether the errors occurred during a header transfer or during a data transfer. After the report has been presented, typing "P" will return the program to the start of the Disk System Test.

```
<<  DRIVE & CONTROLLER TEST REPORT  >>
        [HEXADECIMAL VALUES

                                  HEADER      DATA
NUMBER OF TESTS  . . 0006
WRITE ABORTS  . . . . . . . . . 0000        0000
NO ERROR FLAGS - BAD DATA!. . . 0000        0000
READ ABORTS . . . . . . . . . . 0000        0000
NO TRANSFER COMPLETE  . . . . . 0000        0000
CRC ERROR . . . . . . . . . . . 0000        0000
WRITE DATA MISSES (SOME OK). . . . . . . . 0002

TYPE 'T' TO RESTART TEST, LEAVE COUNT UNCHANGED
TYPE 'C' TO CLEAR COUNT AND RESTART TEST
?
```

Fig. 5-1 Automatic Test Report Format, Printout

5.2.2 DIAGNOSTIC/TROUBLE-SHOOTING TESTS, PRELIMINARY INFORMATION

A. Input/Output Test (Test Part 1)

This test checks the operation of the output ports on the controller PCB. The output ports are used to setup a transfer of data between memory and diskette. The Input/Output Test operates in the manual mode only.

Start with the Input/Output test (I/O Test) for a thorough checkout of the Helios system. The Input/Output Test uses the numeric keys on the keyboard to exercise each bit of the controller output ports. During the I/O tests, a voltage measurement instrument (scope, logic probe, etc.) should be used to monitor the signal at the test points indicated on the controller PCB. When the bit being tested is a Ø, the voltage should be less than 0.5 V or a logic probe should indicate a low level. When the bit being tested is a 1, the voltage should be at least 4 volts. A logic probe should indicate a high.)

COMMAND PORT TEST PATTERN BITS

During frames 4 through 8, there is a pattern of bits in the lower left-hand portion of the frame. Each bit shows a Ø or a 1 to indicate the status of certain test functions defined in the table below. Each bit is individually controlled by the corresponding numeric keys 1 through 8 on the console keyboard. Pressing the key toggles the bit (changes its state); that is, if the bit is Ø, striking the key will change it to 1, and vice versa. Striking the Ø key will return the pattern of bits to their initial condition at the beginning of each frame, which is not always all zeros. Striking the 9 key will print out the pattern on a printer connected to the serial interface.

Frame 3 presents the pattern of bits so you may become familiar with the operation of the keys, before their actual functions are activated. In frames 4 through 8, the functions are activated. Each of frames 4 through 8 instructs you to exercise the various functions in conjunction with an oscilloscope or logic probe. Note that in frame 9, and in further frames, the functions of the numeric keys are progressively redefined. Refer to the table below only for frames 4 through 8. The table may be helpful when the frame which explains the needed key function is not being displayed.

Table 5-1 Command Port Test Pattern Bits

KEY	FUNCTION
1	Step when Ø
2	Direction: Ø = Toward center of disk 1 = Toward Edge of disk
3 4	Drive Selection: KEY 3 / KEY 4 / DRIVE # Ø / Ø / 3 1 / Ø / 1 Ø / 1 / 2 1 / 1 / Ø
5	Restore head to outer disk limit.
6	Load left head
7	Load right head
8	Select unit: Ø = Right unit selected 1 = Left unit selected

> NOTE:
>
> For convenience in running test parts 2 through 6, a blank diskette should be installed in each unit of the dual drive being tested. These diskettes will be erased.

B. Controller/DMA Test (Test Part 2)

(This test initializes the diskette.)

This test exercises the port which initiates actions of the controller. When this test requests a unit for test, type a "Ø" to test the left-hand unit of the disk drive; type a "1" to test the right-hand unit. (Refer to Figure 4-2, "Helios System Numbering/Terminology/Configuration.") This test consists of an oscilloscope checkout of the formatter and controller PCBs. This checkout procedure is printed in Section 5.5, "Controller Transfer/DMA Test/Trouble-shooting Procedure." A dual-trace oscilloscope with triggered sweep is necessary.

C. Header Write Test (Test Part 3)

(REQUIRES PRIOR INITIALIZATION OF DISKETTE)

This test is also run as the first part of the automatic test. It checks the system function of writing the header which precedes and identifies each block of data on the diskette. If there are no aborts during this operation,

the test is considered successful. After this test and also after parts 4, 5, and 6, repeat-options are presented. To select one of these options type from the following table as required:

1	To repeat this test once.
R	To repeat the test until "S" is typed.
B	To repeat this write/read test combination until "S" is typed.
P	To continue

D. Header Read Test (Test Part 4)

(MUST BE PRECEDED BY HEADER WRITE TEST)

Part 4 reads a header. Until this part of the test, the data in the header has not been checked. If the data is correct and no errors occur, this test is considered successful. The repeat options are again presented, described in "Part 3."

E. Data Write Test (Test Part 5)

(REQUIRES AN INITIALIZED DISKETTE)

Part 5 writes a 4K data block on the diskette following the header. If no aborts occur, the test is considered successful. The repeat-options described in "Part 3" are again presented.

F. Data Read Test (Test Part 6)

(MUST BE PRECEDED BY DATA WRITE TEST (Test Part 5)

Part 6 reads the data block written during part 5. When this part is completed, the repeat-options are again presented.

5.2.3 DISK SYSTEM TEST ERRORS

A. Automatic Write/Read Errors

NO TRANSFER COMPLETE	The transfer length counter had not reached Ø at a time when this should have occurred.
DATA WRITE MISSES	A Data Write Miss is an Abort Error 5. (See Below.)

B. Errors During Parts 3, 4, 5, and 6

ABORT (An "ABORT" error message may be caused by one of the following:)

1. The S-100 signal $\overline{\text{POC}}$ (P1, pin-99) went low during the DMA transfer.

2. The formatter was out of sync with the diskette when the transfer was requested.

3. Memory was not ready when a DMA transfer was required.

4. The leading edge of the sector hole after the index hole was detected during a transfer.

5. A request to write data was given to the controller too late after a header had been read and checked.

CRC ERROR

The data which has been read from the diskette does not compare with the data which has been written on it. The data is in serial form.

BAD DATA

The data read from the diskette and transferred to memory does not match the data which was written on the diskette from memory.

5.3 DISK SYSTEM TEST: REQUIREMENTS AND SYSTEM CONFIGURATION

5.3.1 Sol SYSTEM REQUIREMENTS AND CONFIGURATION

1. Helios II system installed in a Sol. (Installation instructions are contained in Sec. 5.4, "Test Operating Instructions."

2. A contiguous block of 16K of memory beginning at address Ø.

3. Video monitor connected to the Sol video output or a serial output device connected to the Sol serial interface connector.

4. Cassette player connected to the Sol ACI (Audio Cassette Interface).

5. An oscilloscope (preferably dual-trace) and a voltage measuring instrument such as a VOM (Volt/Ohm Meter) or logic probe.

6. A blank diskette (32 sector hole type).

7. Cassette containing the Disk System test.

5.3.2 OTHER S-100 SYSTEMS — REQUIREMENTS AND CONFIGURATION

1. Helios II system installed in a host computer. (Installation Instructions are contained in Sec. 5.4, Test Operating Instructions.)

2. At least 16K of contiguous memory beginning at address Ø.

3. At least 3K of contiguous memory for the CUTER operating system.

4. CUTER operating system loaded into the host computer at address 4ØØØ (hex) or higher. The CUTER operating system must be interfaced with a keyboard input device and, either the Processor Technology VDM 1, or a serial output device on pseudo port 1. (Refer to SOLOS/CUTER User's Manual, P. T. To aid users of non-standard systems, the SOLOS/CUTER Interface specifications are included in the latest edition of the SOLOS/CUTER User's Manual.)

5. Processor Technology CUTS cassette interface installed in the host computer and connected to a cassette player.

6. An oscilloscope (preferably dual-trace) and a voltage measuring device such as a VOM (Volt/Ohm Meter) or a logic probe.

7. A blank diskette (32 sector hole type).

8. Cassette containing the Disk System test.

5.4 TEST OPERATING INSTRUCTIONS

(Steps 1 through 11 comprise the System Test Checklist referred to in the beginning of the Disk System Test.)

( ) 1. Be sure you have read all of Section 4, Operating Instructions.

( ) 2. Setup the Helios II system and connect the cables as in Section 4.4, Setup and Installation.

( ) 3. Turn ON AC power to the computer.

( ) 4. Turn ON AC power to the Helios II drive unit.

( ) 5. Eject any diskette(s) written with data you wish to preserve.

( ) 6. On the controller PCB, check P1, pins 1 and 51 with a VOM. They should be a minimum of +7.25 VDC, typically +8 VDC. These pins are the output of the unregulated +8 VDC supply.

( ) 7. On the controller PCB, the top right corner are two regulator IC's (U54 and U55). With a VOM check the output leg of each of these. It should be a minimum of +5 VDC. Looking at the IC with the legs toward you and with the legend on the IC in reading position, the output leg is pin-3, counting from the left.

( ) 8. On the controller PCB verify that a jumper has been installed between FX and C. (Refer to Fig. 8-6, Controller PCB, Assembly.) FX is the augat pin just below U6. It is connected to the trace coming from U6-6. C is the augat pin between U8 and U9 (near pin-1 of U8). It is connected by a trace to U23-5. (This step configures the system for the standard PTDOS.)

( ) 9. On the formatter PCB, on the top right corner is another regulator IC (U31). Verify that the output of this IC is a minimum of +5 VDC.

( ) 10. Insert a blank diskette in unit Ø. Verify that the disk drive grips the diskette and that the spindle is turning after the diskette is accepted. Eject the diskette and verify that the drive responds to the eject button.

( ) 11. Insert a blank diskette in unit 1 and make the same observations as in the previous step.

( ) 12. Setup the cassette recorder and the video monitor as in the Sol Systems Manual, "Monitor and Cassette Recorder Connections."

( ) 13. a. Set the controls on the cassette player. (For the Sol, refer to: Sol Systems Manual, "Command Mode Operation.")

b. Insert the Disk System Test cassette and rewind to the beginning.

( ) 14. Initialize the SOLOS or CUTER program to the command mode — On Sol, by pressing: MODE SELECT

) 15. When the system displays the prompt character >

Type: XEQ DISKT
On the Sol keyboard, Press: RETURN (CR) Carriage Return

The tape should be moving, indicating that the computer is loading the program.* This should take about 3 minutes. If the program is loaded into memory correctly, the computer will stop the tape and display the message: DISKT T (followed by a number). The XEQ command has automatically begun execution of the program. The program is now waiting for input from the SOLOS/CUTER console input device.

In Sol systems this will be the keyboard. In other S-100 systems this will be the default input pseudo-port selected by sense switches two and three when CUTER is started up; that is, the console keyboard.

( ) 16. Before the test can proceed you must select either video or serial output as follows:

For the Sol or other systems which have a VDM-1 installed, select video output for the test by typing: V

OR: If your system doesn't have a VDM-1, hopefully you will have an output device such as a teleprinter which is serially interfaced. To select the serial output option type: S

( ) 17. The Disk System Test Introduction frame should now be displayed or printed depending on the output option selected. (See 5.4.2, "Disk System Test Frames, frame 1.")

*DISKT (Disk System test) is the second program on the tape. The first is "BOOTLOAD," which is bypassed by the command: XEQ DISKT.

Follow the instructions presented on your output device by the test program which you select according to the guidelines in the following section, 5.4.1, Recommended Test Procedure. Refer to 5.2, "Disk System Test, Description and Preliminary Instructions," as an aid in understanding the particular test part you are about to run or are running.

18. Resetting Disk System Test Without Reloading

During certain parts of the test, an option to reset to the beginning of the test is presented on the output device.

All other times:

a. Press: ESCAPE

This resets the system back to SOLOS/CUTER command mode. The SOLOS/CUTER prompt character should appear.

If the SOLOS/CUTER prompt character is not displayed, indicating that escape is not possible at the time:

For Sol only, press simultaneously:

UPPER CASE and REPEAT

(This clears only the system RAM. The Disk System Test is still in memory and does not have to be reloaded.)

For non-Sol systems, begin program execution at the start of the CUTER program.

The SOLOS/CUTER prompt character should appear.

b. Type: EX 3

c. Press: RETURN

d. For video output, type: V

For serial output, type: S

5.4.1 RECOMMENDED TEST PROCEDURES

A. To Qualify a System after Shipping, Modification, Repair, or Maintenance

1. Load unit Ø with a blank diskette in good condition.

2. Call up the Disk System Test according to the operating instructions in section 5.4.

3. After the introductory frame 1 has appeared, type: P

4. In frame 2 where the test options are presented, select the Seek Test by typing: S

5. When the Seek test is completed (about 5 minutes) return to the start of the Disk System Test program by typing: P

6. When the program has returned to the start, in frame 2 where the test options are presented, select the Automatic Write/Read Test by typing: A

   Let the test run for 8 hours minimum. No errors should occur.

7. After unit Ø has passed the above test, test the other unit(s) in the system using the same procedure.

   If significant errors or a major problem is encountered during the above tests, return to the start of the test and select the test which pertains to the problem. If the problem is unknown, follow the thorough diagnostic procedure in B.

NOTE

Seek write and read errors may be caused by factors in the system other than the diskette drive, namely: a bad diskette, a faulty memory, or even the host computer. Therefore, it is recommended that you use the Complete System Checkout procedure which follows in heading B to attempt to diagnose the problem. If it is determined that the diskette, memory boards, the controller and formatter PCBs, the cable and PCB connections, and host computer are all operating without error, the probability is that the seek and/or write/read errors are being caused by an alignment problem(s) in the diskette drive assembly. The system must be returned to an authorized dealer to correct such problems.

CAUTION

Some numeric keys are active during parts of the test in which they are not called for. Do not type numeric keys unless called for in the test instructions. To do so may cause unexpected actions to occur.

B. Complete System Checkout.

1. Load unit Ø with a blank diskette in good condition.

2. Call up the Disk System Test according to the operating instructions in section 5.4.

3. When the introductory frame 1 has appeared, type: P

4. In frame 2 where the test options are presented, start with the I/O test by typing: 1

   (Select unit Ø as the unit under test when called for in frame 4.)

5. When the I/O test is completed, the program will proceed to part 2, Controller/DMA test, then part 3, Header Write test through part 6, Data Read test, and finally the Seek test. The program then returns to the start.

6. When the program has returned to start, select the Automatic Write/Read test (A) and let the system run for an hour or more.

7. After testing unit Ø as above, test the other unit(s) in the system using this procedure.

C. Copy the Disk System Test to Diskette

To speed up the loading of the test for future use, it is convenient to have a copy of it on diskette. This can be done by using the IMAGE command of the PTDOS when both the PTDOS and the test are in memory (refer to PTDOS User's Guide).

Caution: Do not copy the test to the diskette containing the PTDOS. Use a separate diskette.

5.4.2 DISK SYSTEM TEST FRAMES (For Recommended Test Procedure)

A. Manual Test

Frame 1 Introduction

```
                PROCESSOR TECHNOLOGY HELIOS II
                       DISK SYSTEM TEST
                        (REVISION _)
            COPYRIGHT (C) 1977 PROCESSOR TECHNOLOGY CORP.
            +=+=+=+=+=+=+=+=+=+=+=+=+=+=+=+=+=+=+=+=+=+=+=+

   >>>-----> REMOVE DISKS CONTAINING DATA YOU WANT <-----<<<
   >>>-----> TO PRESERVE                          <-----<<<

      WHEN YOU HAVE COMPLETED THE SYSTEM TEST CHECK LIST

   TYPE 'P' TO CONTINUE -?
```

Frame 2

```
            TYPE '1' FOR PART 1 - INPUT/OUTPUT TEST
            TYPE '2' FOR PART 2 - CONTROLLER/DMA TEST
            TYPE '3' FOR PART 3 - HEADER WRITE TEST
            TYPE '4' FOR PART 4 - HEADER READ TEST
            TYPE '5' FOR PART 5 - DATA WRITE TEST
            TYPE '6' FOR PART 6 - DATA READ TEST
            TYPE 'S' FOR SEEK TEST
            TYPE 'A' FOR AUTOMATIC WRITE/READ TESTS
            TYPE 'ESC' TO RETURN TO SOLOS/CUTER
```

Frame 3

```
              +++ DISK I/O PORT TEST +++
 THE NUMERIC KEYS 1 THRU 8 ARE USED TO GENERATE A TEST PATTERN
 FOR THE I/O TESTS. THE Ø KEY INITIALIZES THE PATTERN.
 THE 9 KEY PRINTS THE PATTERN ON A PRINTER CONNECTED TO THE
 SERIAL INTERFACE.
  IN THE LOWER LEFT OF THE SCREEN ARE TWO GROUPS OF FOUR Ø'S,
 WHICH REPRESENT THE EIGHT BITS OF THE TEST PATTERN. KEY 1
 CONTROLS THE FIRST BIT ON THE LEFT. KEY 2 CONTROLS THE 2ND. BIT
 FROM THE LEFT.  ...KEY 8 CONTROLS THE 8TH. BIT. EACH TIME YOU
 STRIKE ONE OF THESE KEYS, THE CORRESPONDING BIT WILL CHANGE
 TO THE OPPOSITE STATE. STRIKE KEY 1. THE LEFT-MOST BIT WILL
 CHANGE FROM Ø TO 1. EXPERIMENT WITH THIS PATTERN GENERATOR,
 THEN TYPE 'P' TO CONTINUE.
   1 2 3 4   5 6 7 8  KEYS
   Ø Ø Ø Ø   Ø Ø Ø Ø
   1 Ø Ø Ø   Ø Ø Ø Ø
   1 1 Ø Ø   Ø Ø Ø Ø
   1 1 Ø Ø   Ø 1 Ø Ø
   Ø Ø Ø Ø   Ø Ø Ø Ø
```

Frame 4 NOTE: If key 3 comes up as a "Ø" on your copy of the Disk System test cassette, toggle it to a "1," before exercising key 8.

THE UNIT Ø SELECTED LIGHT SHOULD BE ON.

KEY 8 CONTROLS THE SELECTION OF THE LEFT OR RIGHT UNIT

WHEN THE DISPLAY INDICATES Ø, THE RIGHT UNIT IS SELECTED.
WHEN THE DISPLAY INDICATES 1, THE LEFT UNIT IS SELECTED

THIS SELECT SIGNAL ORIGINATES AT PIN 2 OF U31 ON THE DISK CONTROLLER BOARD.

EXERCISE THE UNIT SELECTION LOGIC. THEN TYPE 'P' TO CONTINUE

1 Ø 1 1 1 1 1 1
1 Ø 1 1 1 1 1 Ø
1 Ø 1 1 1 1 1 1

Frame 5

WHEN BIT 1 IS Ø THE HEAD MECHANISM WILL STEP FROM TRACK TO TRACK. BIT 2 CONTROLS THE STEP DIRECTION:

Ø = TOWARD THE CENTER OF THE DISK
1 = TOWARD THE EDGE OF THE DISK

WHEN THE HEAD REACHES EITHER LIMIT IT WILL STOP.*

STEP ORIGINATES AT PIN 3 OF U21. IT IS A VERY NARROW PULSE
DIRECTION ORIGINATES AT PIN 12 OF U31.

EXERCISE THE STEP LOGIC USING KEYS 1 AND 2
THEN TYPE 'P' TO CONTINUE

1	2	3	4	5	6	7	8 ← BIT #
1	Ø	1	1	1	1	1	1
Ø	Ø	1	1	1	1	1	1
1	Ø	1	1	1	1	1	1
1	1	1	1	1	1	1	1
Ø	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1

*NOTE

In this test, the operator takes the place of the controller. If the head is allowed to remain at either extreme of its range of movement for several seconds, it may restore to the middle of the disk. This is not necessarily an indication of a defective drive. When the head mechanism reaches an extreme, either change its direction or reset key 1 to 1.

Frame 6

INSERT A BLANK DISKETTE INTO UNIT 1 AND UNIT Ø (If you have only one diskette, insert it into the UUT, Unit Under Test.)
THE READY LIGHT SHOULD COME ON. USE KEY 8 TO SELECT UNIT 1.
THE READY LIGHT SHOULD REMAIN ON.

KEY 6 CONTROLS THE UNIT Ø HEAD. KEY 7 CONTROLS THE UNIT 1 HEAD
WHEN THE DISPLAY INDICATES Ø THE HEAD WILL LOAD

THE SIGNAL FOR HEAD Ø ORIGINATES AT PIN 15 OF U31
THE SIGNAL FOR HEAD 1 ORIGINATES AT PIN 5 OF U31

EXERCISE THE HEADS THEN TYPE 'P' TO CONTINUE

1 Ø 1 1 1 1 1 1
1 Ø 1 1 1 Ø 1 1
1 Ø 1 1 1 1 1 1
1 Ø 1 1 1 1 Ø 1
1 Ø 1 1 1 1 1 1

Frame 7

USE KEYS 1 AND 2 TO MOVE THE HEAD TOWARD THE CENTER OF
THE DISKETTE. WHEN THE INSIDE LIMIT IS REACHED, SET
BIT 1 TO 1

NOW STRIKE KEY 5. THE HEAD WILL QUICKLY RESTORE TO THE OUTER
LIMIT

THE RESTORE SIGNAL ORIGINATES AT PIN 6 OF U1Ø

WHEN THIS CHECK IS COMPLETE, TYPE 'P' TO CONTINUE

1 Ø 1 1 1 1 1 1
Ø Ø 1 1 1 1 1 1
1 Ø 1 1 1 1 1 1
1 Ø 1 1 Ø 1 1 1
1 Ø 1 1 1 1 1 1

Frame 8

KEYS 3 AND 4 CONTROL DRIVE SELECTION AS FOLLOWS:

KEY 4	KEY 3	DRIVE #
Ø	Ø	3
Ø	1	2
1	Ø	1
1	1	Ø

KEY 4 CONTROLS THE SIGNAL ON PIN 1Ø OF U31
KEY 3 CONTROLS THE SIGNAL ON PIN 7 OF U31

CHECK THE DRIVE SELECTION LOGIC IF NECESSARY
THEN TYPE 'P' TO CONTINUE

```
1 Ø 1 1  1 1 1 1
1 Ø Ø Ø  1 1 1 1
1 Ø 1 Ø  1 1 1 1
1 Ø Ø 1  1 1 1 1
```

Frame 9

KEYS 1 THRU 8 NOW CONTROL THE LOW ADDRESS COUNTER.

KEY	SIGNAL
1	PIN 3,U24
2	PIN 2,U24
3	PIN 6,U24
4	PIN 7,U24
5	PIN 3,U25
6	PIN 2,U25
7	PIN 6,U25
8	PIN 7,U25

CHECK EACH SIGNAL THEN TYPE 'P' TO CONTINUE -?

```
Ø Ø Ø Ø  Ø Ø Ø Ø
1 Ø Ø Ø  Ø Ø Ø Ø
1 1 Ø Ø  Ø Ø Ø Ø
1 1 1 Ø  Ø Ø Ø Ø
1 1 1 1  Ø Ø Ø Ø
1 1 1 1  1 Ø Ø Ø
1 1 1 1  1 1 Ø Ø
1 1 1 1  1 1 1 Ø
1 1 1 1  1 1 1 1
```

Frame 10

KEYS 1 THRU 8 NOW CONTROL THE HIGH ADDRESS COUNTER.

KEY	SIGNAL
1	PIN 3,U26
2	PIN 2,U26
3	PIN 6,U26
4	PIN 7,U26
5	PIN 3,U27
6	PIN 2,U27
7	PIN 6,U27
8	PIN 7,U27

CHECK EACH SIGNAL THEN TYPE 'P' TO CONTINUE -?

Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø
1	Ø	Ø	Ø	Ø	Ø	Ø	Ø
1	1	Ø	Ø	Ø	Ø	Ø	Ø
1	1	1	Ø	Ø	Ø	Ø	Ø
1	1	1	1	Ø	Ø	Ø	Ø
1	1	1	1	1	Ø	Ø	Ø
1	1	1	1	1	1	Ø	Ø
1	1	1	1	1	1	1	Ø
1	1	1	1	1	1	1	1

Frame 11

KEYS 1 THRU 8 NOW CONTROL THE LOW TRANSFER LEN. COUNTER.

KEY	SIGNAL
1	PIN 3,U28
2	PIN 2,U28
3	PIN 6,U28
4	PIN 7,U28
5	PIN 3,U29
6	PIN 2,U29
7	PIN 6,U29
8	PIN 7,U29

CHECK EACH SIGNAL THEN TYPE 'P' TO CONTINUE -?

Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø
1	Ø	Ø	Ø	Ø	Ø	Ø	Ø
1	1	Ø	Ø	Ø	Ø	Ø	Ø
1	1	1	Ø	Ø	Ø	Ø	Ø
1	1	1	1	Ø	Ø	Ø	Ø
1	1	1	1	1	Ø	Ø	Ø
1	1	1	1	1	1	Ø	Ø
1	1	1	1	1	1	1	Ø
1	1	1	1	1	1	1	1

Frame 12

KEYS 1 THRU 4 NOW CONTROL THE 4 BITS OF THE HIGH TRANSFER LENGTH COUNTER

KEY	SIGNAL
1	- PIN 3,U30
2	- PIN 2,U30
3	- PIN 6,U30
4	- PIN 7,U30

CHECK EACH SIGNAL THEN TYPE 'P' TO CONTINUE -?

```
Ø Ø Ø Ø  Ø Ø Ø Ø
1 Ø Ø Ø  Ø Ø Ø Ø
1 1 Ø Ø  Ø Ø Ø Ø
1 1 1 Ø  Ø Ø Ø Ø
1 1 1 1  Ø Ø Ø Ø
```

Frame 13

>> CONTROLLER TRANSFER/DMA TEST <<

```
BE SURE A DISKETTE IS INSERTED IN EACH UNIT.
THEN TYPE THE # OF THE UNIT YOU WANT TO TEST (Ø-7)  IT'S NOT READY!
BE SURE A DISKETTE IS INSERTED IN EACH UNIT.
THEN TYPE THE # OF THE UNIT YOU WANT TO TEST (Ø-7)
 TESTING UNIT Ø
KEYS 1 THRU 4 NOW CONTROL THE TRANSFER COMMAND PORT.

KEY 1 = ERASE WHEN Ø
KEY 2 = READ WHEN 1 / WRITE WHEN Ø
KEY 3 = TR. HEADER WHEN 1 / TR. DATA WHEN Ø
KEY 4 = ENABLE TRANSFER WHEN Ø

USING THESE KEYS IT IS POSSIBLE TO CHECK OUT THE CONTROLLER
AND FORMATTER BOARDS. SEE THE TEST INSTRUCTIONS FOR THESE STEPS. *
WHEN THE LAST CHECK IS COMPLETED TYPE 'P' TO CONTINUE -?
 1 1 1 1  1 1 1 1
```

*5.5, Controller Transfer/DMA Test Trouble-shooting Procedure

Frame 14

```
WAIT A MOMENT WHILE THE DISK IS BEING ERASED


HEADER  WRITE TEST:  OK

TYPE '1' TO REPEAT THIS TEST ONCE
TYPE 'R' TO REPEAT THIS TEST UNTIL 'S' IS TYPED
TYPE 'B' TO REPEAT THIS WRITE/READ TEST COMBINATION
         UNTIL 'S' IS TYPED
TYPE 'P' TO CONTINUE -?
```

Frame 15

```
HEADER  READ TEST:   OK   DATA GOOD


TYPE '1' TO REPEAT THIS TEST ONCE
TYPE 'R' TO REPEAT THIS TEST UNTIL 'S' IS TYPED
TYPE 'B' TO REPEAT THIS WRITE/READ TEST COMBINATION
         UNTIL 'S' IS TYPED
TYPE 'P' TO CONTINUE -?
```

Frame 16

```
DATA WRITE TEST:     OK

TYPE '1' TO REPEAT THIS TEST ONCE
TYPE 'R' TO REPEAT THIS TEST UNTIL 'S' IS TYPED
TYPE 'B' TO REPEAT THIS WRITE/READ TEST COMBINATION
         UNTIL 'S' IS TYPED
TYPE 'P' TO CONTINUE -?
```

Frame 17

```
DATA READ TEST:      OK   DATA GOOD


TYPE '1' TO REPEAT THIS TEST ONCE
TYPE 'R' TO REPEAT THIS TEST UNTIL 'S' IS TYPED
TYPE 'B' TO REPEAT THIS WRITE/READ TEST COMBINATION
         UNTIL 'S' IS TYPED
TYPE 'P' TO CONTINUE -?
```

B. Automatic Test, Frame 1

```
BE SURE A DISKETTE IS INSERTED IN EACH UNIT. (Or only the UUT)
THEN TYPE THE # OF THE UNIT YOU WANT TO TEST (Ø-7)
 TESTING UNIT Ø


WAIT A MOMENT WHILE THE DISK IS BEING ERASED


                  <<  AUTOMATIC TESTS  >>

TEST PARTS: 1.  WRITE RANDOM HEADER
            2.  READ AND COMPARE HEADER
            3.  READ HEADER, WRITE DATA BLOCK
            4.  READ AND COMPARE DATA BLOCK

                   > DISPLAY OPTIONS <

TYPE 'D'  FOR DISPLAY ON, NO STOP ON ERRORS
TYPE 'E'  FOR DISPLAY ON, STOP ON ERRORS
TYPE 'O'  STOP AND DISPLAY ERRORS ONLY
TYPE 'N'  FOR NO DISPLAY, NO STOP
DURING TEST TYPE: 'G' TO STOP AND GENERATE A REPORT
LC
  HEADER  WRITE TEST:  OK

HEADER  READ TEST:   OK   DATA GOOD


DATA WRITE TEST:     OK

DATA READ TEST:      OK   DATA GOOD


HEADER  WRITE TEST:  OK

HEADER  READ TEST:   OK   DATA GOOD


DATA WRITE TEST:     OK

DATA READ TEST:      OK   DATA GOOD
```

Automatic Test, Frame 2

```
HEADER  WRITE TEST:  OK
HEADER  READ TEST:   OK   DATA GOOD

DATA WRITE TEST:     OK
DATA READ TEST:      OK   DATA GOOD

HEADER  WRITE TEST:  OK
HEADER  READ TEST:   OK   DATA GOOD

DATA WRITE TEST:     OK
DATA READ TEST:      OK   DATA GOOD

HEADER  WRITE TEST:  OK
HEADER  READ TEST:   OK   DATA GOOD

DATA WRITE TEST:     ----------------> READ FILE ID ERROR

DATA WRITE TEST:     ----------------> READ FILE ID ERROR

DATA WRITE TEST:     OK
DATA READ TEST:      OK   DATA GOOD

HEADER  WRITE TEST:  OK
HEADER  READ TEST:   OK   DATA GOOD
```

5.5 CONTROLLER TRANSFER/DMA TEST/TROUBLE-SHOOTING PROCEDURE

Use these procedures for trouble-shooting, if a problem can be traced to controller functions.

This section contains instructions for a signal-by-signal test of the Controller transfer/DMA function. The Controller is tested in Section 5.5.1 and the Formatter in 5.5.2. This test may be reached by loading the Disk System Test as described in Section 5.4, Test Operation Instructions. In frame 2 select "Controller/DMA Test" by typing "2." At frame 13 select units Ø (left) or 1 (right). All testing in Sections 5.5.1 and 5.5.2 is done in frame 13.

5.5.1 CONTROLLER PCB

Using a dual-trace oscilloscope, make the following checks on the controller PCB. Most of the checks are to be made on IC pins, for which a "DIP clip" is very useful. Be very careful not to short adjacent pins on the ICs. In the first step "Check $\overline{\text{TRANSFER COMMAND}}$ (U42-14)" means "Put the probe of the oscilloscope on pin 14 of U42, with the return lead of the oscilloscope connected to zero volts, to observe the signal called $\overline{\text{TRANSFER COMMAND}}$." To perform these tests you must be in frame 13 of the Disk System Test, per previous instructions in this Section. When frame 13 first appears, the bit pattern in the lower left-hand portion of the screen is initialized at 1111. Various instructions below call for modifying this pattern using the numeric keys on the keyboard. Make only the changes which are called for, and check to see that the pattern matches the pattern in the column to the left of the test instructions below before proceding to the instructions. When the instructions modify the bit pattern, the new pattern is shown at the beginning of the next line. For purposes of trouble-shooting, Table 7-1, Distribution of Helios II Functions, and Table 8-1, Numerical Pin-to-Pin Assignments, Controller P3/Formatter P3, may be useful. Figures 8-6 and 8-7, the assembly drawings of the formatter and controller PCBs, can help in locating ICs.

STEP NO.	CURRENT BIT PATTERN KEYS 1-4	TEST INSTRUCTIONS
( ) 1.	1111	Check $\overline{\text{TRANSFER COMMAND}}$ strobe (U42-14). There should be a string of sharp negative-going pulses.
( ) 2.	1111	Check $\overline{\text{ERASE}}$ (U22-15). It should be at a TTL high level. Set key 1
	Ø111	to Ø. $\overline{\text{ERASE}}$ should go low. Leave key 1 at Ø.
( ) 3.	Ø111	Check $Ø_2$ (U6-8). There should be a positive pulse every 500 ns.

( ) 4. Ø111 Check $\overline{\text{CLOCK Ø}}$ (U14-12). Also check at the same time: $\overline{\text{CLOCK 2}}$ (U14-11), and $\overline{\text{CLOCK 4}}$ (U14-10). Sync the oscilloscope on U9-14. Each of these three signals should be a 500 nsec negative pulse, occurring the in sequence listed, at 1 µs. intervals.

( ) 5. Ø111 Check INDEX (U50-4).
There should be a negative pulse every 166 msec (every diskette revolution).

( ) 6. Ø111 Check SELECTED DISC READY (U50-6).
This signal is normally low. Eject the diskette whose select light is on. The signal should go high.

( ) 7. Ø111 Check $\overline{\text{SELECTED HEAD LOADED}}$ (U15-9).
This signal is normally low. On the S-100 edge-connector of the Controller PCB, jumper between pin 3 (XRDY) and pin 50 (Ø volts) for two seconds but not more than five seconds. After about one second the signal should go high, and you should hear the head loading mechanism click.
WARNING: Do not ground pin 2, a power supply pin.

( ) 8. Ø111 Check $\overline{\text{RSECT}}$ (U10-12).
There should be a negative pulse every 10 ms. If no pulses are found, trace the index and sector signals through the sector reset logic on the Formatter PCB.

( ) 9. Ø111 Check $\overline{\text{WRITE}}$ (U39-7).
It should be low. Set key 1 to 1. $\overline{\text{WRITE}}$ should
1111 go high. Leave key 1 set to Ø with $\overline{\text{WRITE}}$ low.
Ø111 Also check WRITE (U39-6) which has the inverse signal.

( )10. Ø111 Check TC (U33-4).
Set key 1 to 1, then back to Ø. TC should go low then high again. Leave key 1 set to Ø.

( )11. Ø111 Check $\overline{\text{MAIN CLOCK}}$ (U11-4).
It should be identical to $\overline{\text{CLOCK 4}}$, tested in Step 4 above.

( )12. Ø111 Check $\overline{\text{CROSSOVER}}$ (U19-5).
There should be negative pulses.

( )13. Ø111 Check $\overline{\text{SYNC ERROR}}$ (U17-2).
It should be high with no pulses.

( )14. Ø111 Set key 1 to 1. Confirm that keys 2, 3, and 4
1111 are set to 1.

( )15. 1111 Check $\overline{\text{RMC}}$ (U14-1).
It should go negative for periods of approximately 3 usec.

( )16. 1111 Check $\overline{\text{RCLOCK}}$ (U11-3). It should be negative pulses of .9 µs duration, at 4 µs intervals.
Check MAIN CLOCK (U9-4), using the other trace. It should be the inverted form of $\overline{\text{RCLOCK}}$ (U11-3).
Check MAIN CLOCK (U9-5). It should be the same as MAIN CLOCK (U9-4).

( )17. 1111 Sync the oscilloscope on $\overline{\text{TRANS COMM}}$ (U42-14).
Display the waveform of $\overline{\text{TRANSFER}}$ (U22-10).
It should be high with no pulses.

( )18. 1111 This step is a likely point for a board error to cause a system crash since it involves repeated DMA transfers. To initiate DMA transfers, set key 4 to Ø, and leave it at Ø until
1110 Step 34. If there is no crash, procede.

( )19. 1110 Check $\overline{\text{TRANSFER}}$ (U22-10).
There should be negative pulses of up to 11 ms duration.

( )20. 1110 Check $\overline{\text{DMAOFF}}$ (U20-9).
It should have positive pulses of about 1.3 ms duration. Check DMAOFF (U20-10).
It should be a complementary signal.

( )21. 1110 Sync on $\overline{\text{DMAOFF}}$ (U20-9).
display HOLD (U2-6).
1.1 ms after the start of $\overline{\text{DMAOFF}}$, there should be a positive pulse of about 25 µs duration.

( )22. 1110 Check CRC ERROR (U33-13) and CRC CHECKED (U33-9).
Both should start low. CRC CHECKED goes high near the end of DMAOFF (U20-10), but CRC ERROR should remain low.
Sync on HOLD (U2-6).
Check DMASYNC (U18-11).
This should be a burst of about 14 positive pulses coinciding with HOLD (U2-6). Each pulse should be .5 µs in duration, at 1.5 µs intervals.

( )23. 1110 Check PHLDA (U1-4).
It should look like HOLD, but occur slightly later.
Check $\overline{\text{BUS TRANSFER}}$ at U40-3 and at U40-11.
They should be identical to HOLD (U2-6), but inverted.

( )24. 1110 Check $\overline{\text{IRF}}$ (U11-13).
It should be high for about 12 ms surrounding HOLD, and low otherwise.

( )25. 1110 Check $\overline{\text{ORE}}$ (U11-14).
It should be a train of positive pulses of approximately 400 ns duration, during HOLD (U2-6).

( ) 26. 111Ø Check $\overline{\text{TEST}}$ (U16-1).
It should be a train of negative pulses of approximately 500 nsec duration, during HOLD (U2-6).

( ) 27. 111Ø Check BUMP (U28-14) and $\overline{\text{BUMP}}$ (U36-2).
Both should be identical to $\overline{\text{TEST}}$ (U16-1).

( ) 28. 111Ø Check $\overline{\text{ABORT SI}}$ (U17-8) and $\overline{\text{TCSI}}$ (U17-6).
They should be high with no pulses.

( ) 29. 111Ø Check $\overline{\text{NORMAL}}$ (U16-6) and $\overline{\text{NORMAL R}}$ (U24-14).
They should have negative pulses during HOLD (U2-6).

( ) 30. 111Ø Check FIFOPL (U11-7).
It should be low with no pulses.

( ) 31. 111Ø Check $\overline{\text{PWR}}$ (U13-12).
There should be a train of about 16 negative pulses of approximately 200 nsec duration.

( ) 32. 111Ø Check the FIFOs, U52 and U53, with the following procedures. They are normally hot to the touch.

a) Check DI Ø-7 (U52 pins 3 through 6 and U53 pins 3 through 6). All eight pins should be positive with negative pulses.

b) Check QØ through Q3 (U52 pins 18 through 21 and U53 pins 18 through 21). All eight pins should be high with no pulses.

c) Check each of the following signals on the FIFOs, U52 and U53. Check the pins shown below on each FIFO.

SIGNAL	PIN NO.	CONDITION
DS	7	Positive pulses, each 3 usec long, during HOLD (U2-6).
CPSI	8	Short positive pulses, 3 usec apart.
IESB	U53-9	Burst of 16 usec pulses, starting when HOLD (U2-6) goes high.
IESA	U52-9	Low with no pulses.
TTS	10	Negative pulse at the beginning of HOLD (U2-6).
$\overline{\text{MR}}$	11	High during HOLD (U2-6).
TOP	13	Positive pulses during HOLD (U2-6).
$\overline{\text{TOS}}$	14	Positive pulses during HOLD (U2-6) of very short duration.

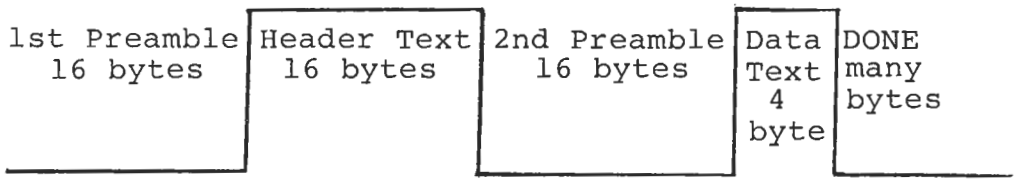
SIGNAL	PIN NO.	CONDITION
$\overline{\text{OESA}}$	U-52-15	Low with no pulses.
$\overline{\text{OESB}}$	U53-15	Positive pulses during HOLD (U2-6) of very short duration.
$\overline{\text{CPSO}}$	16	Low during HOLD (U2-6).
EO	17	Low during HOLD (U2-6).

( ) 33. 111Ø Check the status driver inputs:
TC (U51-4) should be low.
SREADY (U51-2) should be low during HOLD (U2-6) and go high 500 usec after the start of HOLD (U2-6).
ABORT (U51-10) should be low during HOLD (U2-6).
CRC ERROR (U51-6) should be low with no pulses.

( ) 34. 111Ø Perform the following sequence of keystrokes in the order given, in preparation for the next test. This sequence erases the selected track.

Set key 4 to 1 for a bit pattern of 1111.
1111 Set key 2 to Ø.
1Ø11 Set key 1 to Ø then back to 1.
1Ø11 Set key 2 to 1. Final bit pattern is 1111.

( ) 35. 1111 Sync on $\overline{\text{RSECT}}$ (U10-12).
Display TEXT (U12-2).
It should exhibit the following waveform:



( ) 36. 1111 Set key 4 to Ø. This will read the header off
111Ø the diskette into memory. The waveform should remain the same. Leave key 4 at Ø.

( ) 37. 111Ø Set key 3 to Ø. This will read the data text off
1ØØ the diskette into memory. The waveform should remain the same. Set key 3 back to 1.

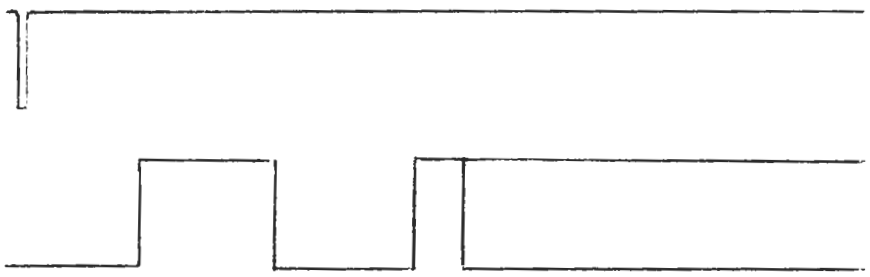
( ) 38. 111Ø Set key 2 to Ø. This will write the header text
1Ø1Ø on the diskette. The first preamble and data text portions of the waveform should remain the same, but the rest of the waveform may jitter.

Set key 2 to 1.

111Ø The original waveform of Step 35 should return.

( ) 39. 111Ø Set key 3 to Ø.
11ØØ Set key 2 to Ø.
1ØØØ This will write data on the diskette.
The waveform should be as follows:

$\overline{\text{RSECT}}$



Reset the keys for a bit pattern of 1111.

( ) 40. 1111 Repeat the keystroke sequence of Step. 34.
1111 Repeat Step 35.

( ) 41. 1111 Check ABORT (U51-1Ø).
Set key 1 to Ø. Wait one second. Set key 1 to 1.
1111 ABORT should be low.
Set key 3 to Ø.
11Ø1 ABORT is alternately high and low.
Set key 3 to 1.
1111 ABORT should be low.

This concludes the test of the controller PCB.
Procede to test the formatter PCB in the next section.

5.5.2 FORMATTER PCB

This section contains a signal-by-test of the Formatter PCB, similar to the test of the Controller PCB above. Follow the general instructions given in Sections 5.5 and 5.5.1 above.

STEP NO.	CURRENT BIT PATTERN	TEST INSTRUCTIONS
( ) 1.	1111	Set key 1 to Ø.
( ) 2.	Ø111	Sync on INDEX (U15-15). Display SECTOR (U14-12). It should have 32 negative pulses per INDEX pulse.
( ) 3.	Ø111	Check $\overline{\text{RSECT}}$ (U16-6). It should have negative pulses every 10 msec. If not, trace INDEX and SECTOR signals through the sector reset logic.
( ) 4.	Ø111	Check five outputs of the Bit Counter (BC), U13. Figure 5-2, Bit Counter Timing, shows the action of this counter. It is clocked by $\overline{\text{MAIN CLOCK}}$ (U13-2) which pulses as each bit is transferred. There are four outputs: Q_A, Q_B, Q_C, and Q_D, and a carry output TC. A four output counter normally has 16 states, but in this counter 8 of the states have been surpressed, so that 8 states remain. If the four outputs of the counter are added, and represented in hexadecimal notation, the eight counts are, in sequence: Ø, 9, A, B, C, D, E, F; Ø, as shown in Figure 5-2, Bit Counter Timing. Sync on the negative-going edge of Q_D (U13-11). Display Q_D (U13-11), and adjust the time base so that a complete cycle is visible. While displaying Q_D, with the other trace check the other signals shown in Figure 5-2. Each signal should have the transitions shown.

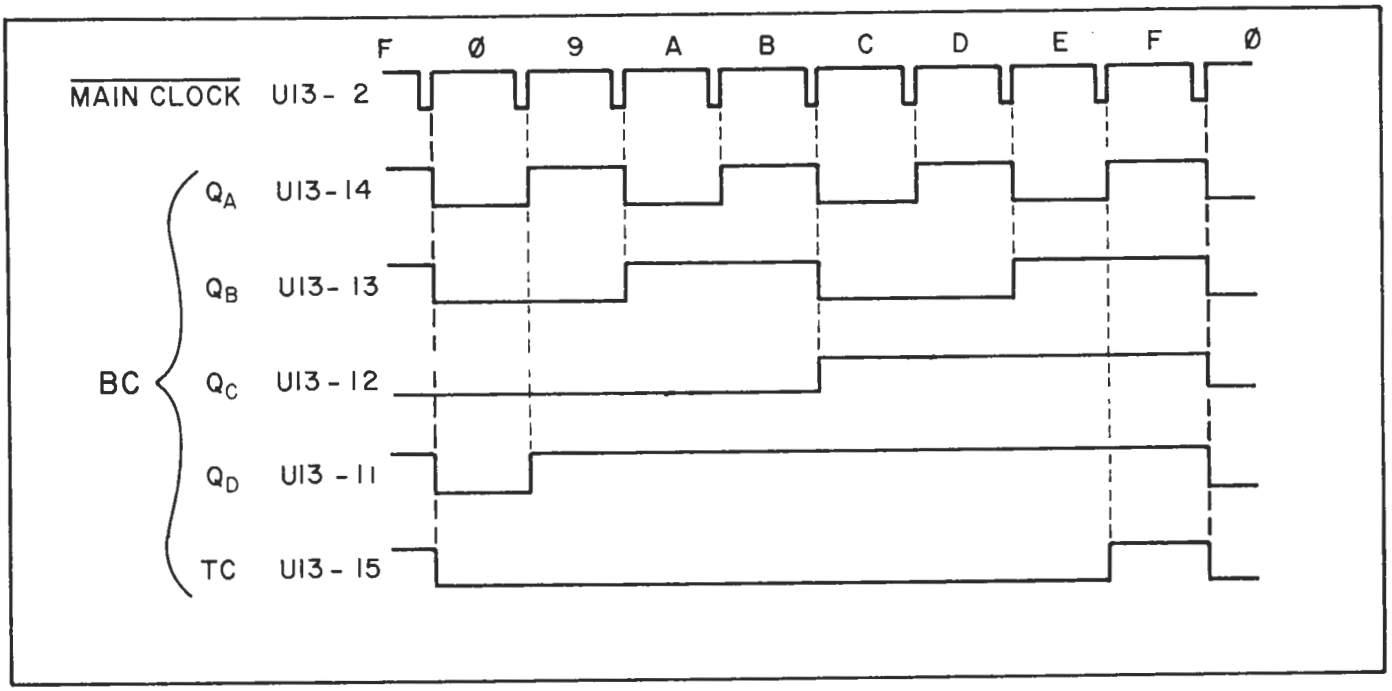


Figure 5-2. Bit Counter Timing

( ) 5. Ø111 Set key 2 to Ø.
ØØ11 Check the Punctuation Counter (PC), and signals decoded from PC, referring to Figure 5-3, Formatter Timing During Erase. This diagram shows various signals derived from BCTC (U13-15), which appears as the bottom signal on Fig. 5-2, and the top signal on Figure 5-3. The horizontal dimension of Figure 5-3 is divided into the five components of the data block of each sector on the diskette: 1st Preamble, Header, 2nd Preamble, Data, and Done. The pattern of these five elements repeats. "Done" may be envisioned as a period of long duration, about 8 msec., extending off the right-hand side of the diagram, with all signals except BCTC (U13-15) inactive. The tail end of the Done period is shown again on the left-hand side of the diagram. PC is a 16 state counter during the 1st Preamble, Header, and 2nd Preamble intervals. During the Done interval, states 1 through C are surpressed. The states of PC are shown in hexadecimal notation at the top of the diagram. The IC and pin number on which each signal may be found is shown immediately to the left of each signal.

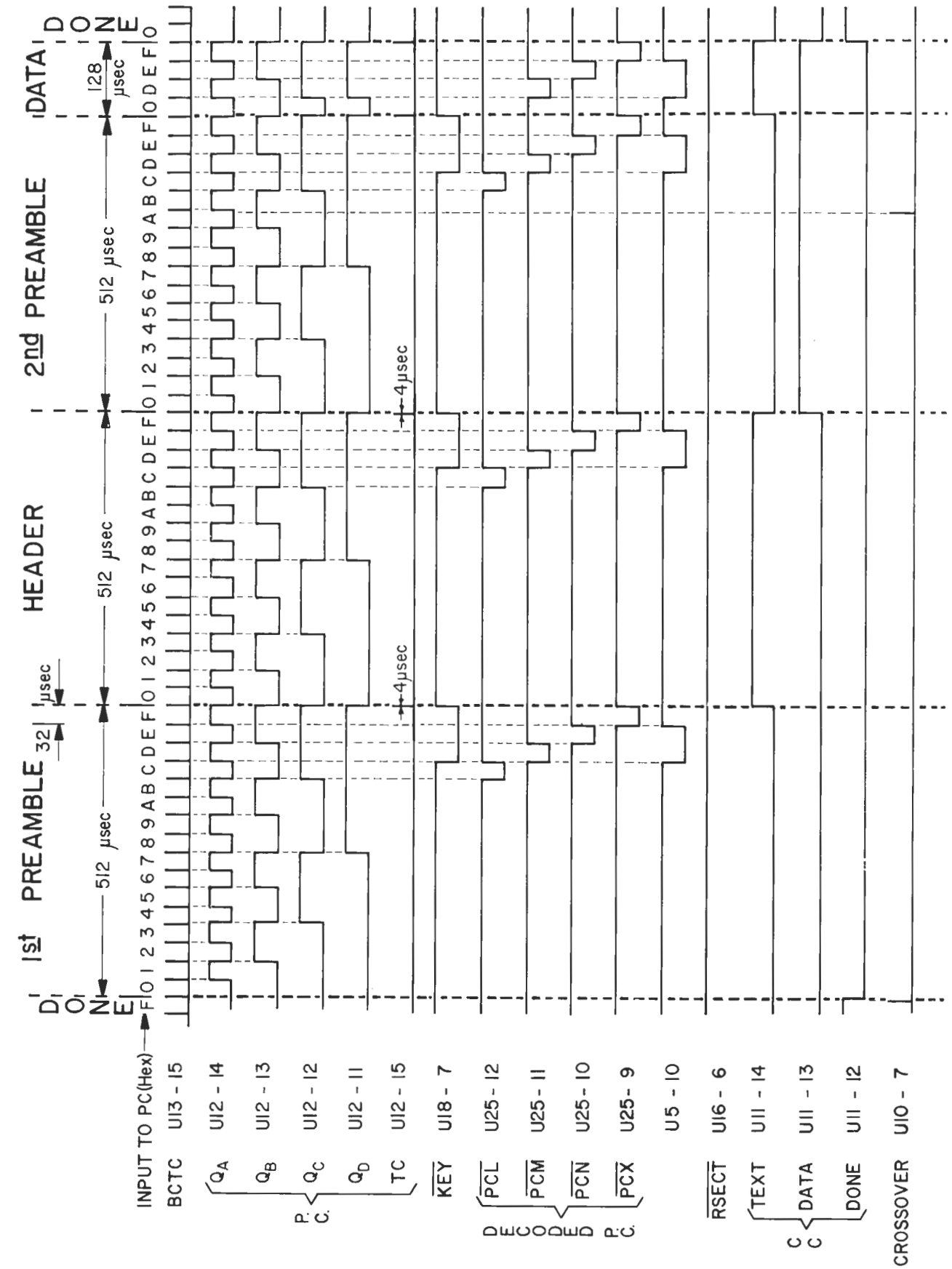


Fig. 5-3 Formatter Timing During Erase

Sync on the negative-going edge of $\overline{\text{RSECT}}$ (U16-6), the fifth signal from the bottom, in Figure 5-3. Display BCTC (U13-15), and adjust the time base so that 16 pulses of BCTC are visible, so details within the 1st Preamble may be examined. Still displaying BCTC, with the other trace examine signals Q_A through U5-10 in sequence. Check each signal to make sure its transitions are as shown in Figure 5-3, by displaying it over BCTC and counting pulses.

( ) 6. ØØ11 With the same oscilloscope arrangement, readjust the time base for a .2 msec per division, to display the entire pattern of Figure 5-3,"Formatter..." With one trace, display $\overline{\text{PCX}}$ (U25-9). Check it against the diagram. With the other trace, examine CC signals TEXT (U11-14), DATA (U11-13), and DONE (U11-12). Check each signal so make sure its transitions are as shown, by comparing against $\overline{\text{PCX}}$. Also check CROSSOVER (U10-7), the bottom signal on Figure 5-3. Look for a very sharp pulse coinciding with $\overline{\text{RSECT}}$ (U16-6), and another sharp pulse at the A to B transition of BCTC. Check $\overline{\text{CROSSOVER}}$ (U2-12), not shown in Figure 5-3. It should be the complement of CROSSOVER (U10-7).

( ) 7. ØØ11 Sync on the positive-going edge of DATA (U11-13). Display DATA (U11-13), and adjust the time base to display its complete positive period (640 usec). Now move the same probe to display BCTC (U13-15). Approximately 22 positive pulses should be visible. This arrangement will be used to display the details of the 2nd Preamble and Data intervals, on the right-hand side of the diagram. With the other trace, display each of the signals Q_A through U5-10 in sequence. Check each signal to make sure its transitions are as shown, by displaying it over BCTC and counting pulses.

( ) 8. ØØ11 Sync on $\overline{\text{RSECT}}$ (U16-6). Display TEXT (U11-14). Note the waveform. With the bit pattern set as it has been, ØØ11, the Controller and Formatter have been writing data blocks in each sector on the diskette. Since no data has been written in these blocks, all data bytes have been FF.

Set key 1 to 1. Also set key 2 to 1.

1111 This causes the controller and formatter to read data blocks from the diskette. The waveform should remain essentially the same, although it

may jitter slightly. If so, skip to Step 29. If the waveform does not remain essentially the same, there is a problem in the read or syncronization logic, which may be located in Steps 9-20 which follow.

( ) 9. 1111 Check SEPARATED CLOCK (U6-11). It should be a train of positive pulses, .2 usec wide, at 4 usec intervals.

( )10. 1111 Sync on the positive-going edge of TEXT (U11-14). Check the signal at U17-4.
It should be a train of negative pulses 2.45 usec wide, at 4 usec intervals.

( )11. 1111 Sync on the negative-going edge of $\overline{\text{RSECT}}$ (U16-6). Set the time base of about .2 msec per division. Display $\overline{\text{RMC}}$ (U28-7).
It should have 4 usec wide negative pulses at 512, 1024, 1536, and 1664 usec, ± 6.6%, measured from $\overline{\text{RSECT}}$. There may be one additional intermittant pulse elsewhere.

( )12. 1111 With the same sync and time base, and still displaying $\overline{\text{RMC}}$ (U28-7), display RDATA (U29-10). During the interval just before the first $\overline{\text{RMC}}$ and between the second and third $\overline{\text{RMC}}$, RDATA should be mostly low. During the interval between the first and second $\overline{\text{RMC}}$, and between the third and fourth $\overline{\text{RMC}}$, RDATA should be mostly high.

( )13. 1111 Sync on the positive-going edge of RDATA (U29-10). Display RDATA (U29-10).
It should be a train of positive pulses, 3 usec wide, at 4 usec intervals. Some pulses may be missing.

( )14. 1111 With the other trace, display $\overline{\text{RDATA}}$ (U29-9). It should be identical to RDATA (U29-10) but inverted.

( )15. 1111 Sync on and display $\overline{\text{RCLOCK}}$ (U17-12). With the other trace, display MAIN CLOCK (U4-10). It should be identical to $\overline{\text{RCLOCK}}$ (U17-12), but inverted.

( )16. 1111 Move the trace from MAIN CLOCK (U4-10) to $\overline{\text{MAIN CLOCK}}$ (U4-9). It should be identical to $\overline{\text{RCLOCK}}$ (U17-12) which is also displayed.

( )17. 1111 Sync on the negative-going edge of $\overline{\text{RSECT}}$ (U16-6). Set the time base for about .2 msec per division. Display $\overline{\text{SYNC}}$ (U27-8).

It should have .9 usec wide pulses at 512, 1024, 1536, and 1664 usec, ± 6.6%, measured from RSECT.

( )18. 1111 With the same sync and time base, display SYNC ERROR (U1-11). It should be high with no pulses.

( )19. 1111 Sync on the negative-going edge of RSECT (U16-6). Set the time base for about .2 msec per division.

Figure 5-3 shows timing during erase only. We are now reading rather than erasing, but some signals shown in Figure 5-3 are still as shown, and may be checked.

With one trace, display BCTC (U13-15). With the other trace, display PCL (U25-12). It should be as shown in Figure 5-3. Move the probe from PCL to KEY (U18-8). It too should be as shown in Figure 5-3.

( )20. 1111 With the same sync and time base, move the probe on BCTC (U13-15) to PCL (U25-12). Move the other probe from KEY (18-7) to PCQA (U12-14). This signal, and the other signals tested in this step may not be as shown in Figure 5-3. The period that PCL is low is one byte in duration (32 usec). Three "PCLs" should be visible.

( ) a) Check PCQA (U12-14). It should be low during the first PCL, and high during the following byte.

( ) b) Check PCQB (U12-13). It should be low during the first PCL, and also low during the following byte.

( ) c) Check PCQC (U12-12). It should be high during the first PCL, and also high during the following byte.

( ) d) Check PCQD (U12-11). It should be high during the first PCL, and low during the following byte.

( ) e) Check PCQA (U12-14) again. It should be low during the third PCL, and high during the following byte.

( ) f) Check PCQB (U12-13) again. It should be low during the third PCL, and also low during the following byte.

( ) g) Check PCQC (U12-12) again.
It should be high during the third $\overline{\text{PCL}}$, and low during the following byte.

( ) h) Check PCQD (U12-11) again.
It should be high during the third $\overline{\text{PCL}}$, and also high during the following byte.

If there is a problem discovered in the above substeps, check the $\overline{\text{PULL 8}}$ and $\overline{\text{PULL 4}}$ circuitry. If there is no problem, set keys 1 and 2 to Ø and repeat Step 8. Then continue at Step 21.

( )21. ØØ11or 1111 111Ø Set the bit pattern to 111Ø.
Sync on the negative-going edge of $\overline{\text{DMAOFF}}$ (U27-1), and display it. It should have a positive pulse of about 2 msec duration.
Set bit 4 back to 1.

( )22. 1111 Sync on $\overline{\text{RSECT}}$ (U16-6).
Set the time base for about .2 msec per division.
Display TEXT (U11-14).
It should be as shown in Figure 5-3, "Formatter Timing During Erase."

( )23. 1111 111Ø Still displaying the same waveform, set key 4 to Ø.
Header (the second main interval shown in Figure 5-3) is being read from diskette to memory.
The waveform should remain the same.

( )24. 111Ø 11ØØ 111Ø Set key 3 to Ø.
Data (the fourth interval in Figure 5-3) is being read from diskette to memory.
The waveform should remain the same.
Set key 3 back to 1.

( )25. 111Ø 1Ø1Ø 111Ø Set key 2 to Ø.
Header is being written on diskette.
The 1st Preamble and Data should remain the same.
The rest of the waveform will jitter.
Set key 2 back to 1.
The same stable waveform should return.
Set key 2 back to Ø.

( )25. 1Ø1Ø 1ØØØ Set key 3 to Ø.
Data is being written on the diskette.
The basic waveform should remain, but on alternate traces, the second high pulse displayed will remain high until the end of the sweep instead of going low.

This concludes the signal-by-signal checkout of the Controller and Formatter PCBs. If you have performed these tests as part of the overall Disk System Test, you may type "P" to proceed to frame 14.

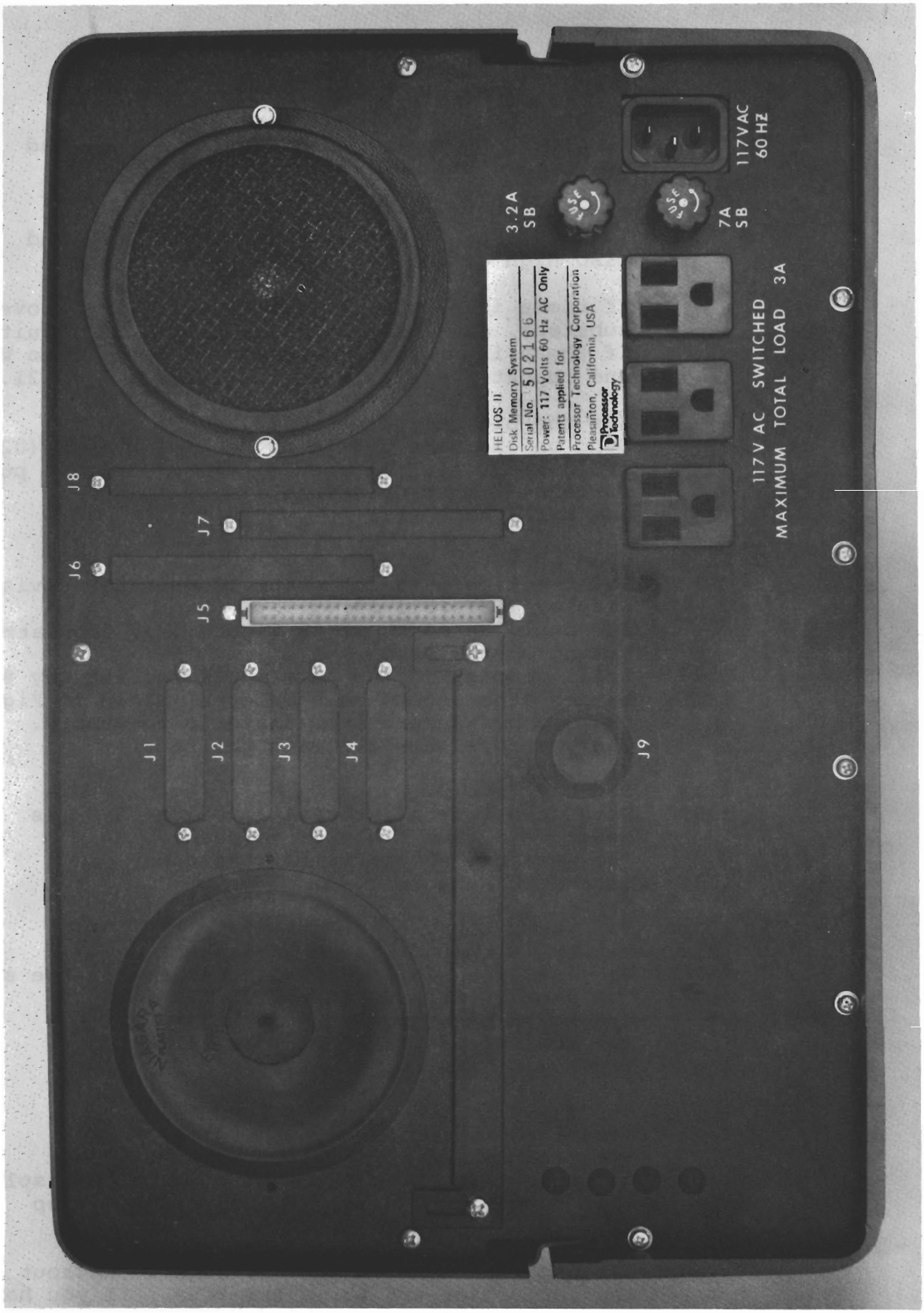


Fig. 5-4 Helios II Rear Panel, Outside View

5.6 BASIC TROUBLE-SHOOTING PROCEDURES

5.6.1 CIRCUIT BOARDS CHECKOUT

( ) 1. Visually check the Helios PCBs for solder brides (shorts).

> **CAUTION**
>
> Obviously constructed solder bridges may be board modifications by the factory.

( ) 2. Check the board to insure that the +5 volt bus is not shorted to ground: Using an ohmmeter, measure between pins 1 and 50; there should be no continuity (no short circuit).

3. If visual inspection reveals any defects, or you measure a short in the above test, and you cannot easily correct the problem, return the board to your authorized dealer for repair or replacement.

5.6.2 CHECKING CONNECTOR CONTACTS ON DISKETTE DRIVE

On the top edge of the data and interface PCB of the diskette drive assembly are a number of plug connectors for various cables internal to the drive assembly. The connectors tend to work loose especially during shipping. Make sure all these connectors are securely in place.

5.6.3 USE OF GROUND CONNECTION ON PCBs

Use the ground TP (Test Point) at pin 50 on the S-100 connector P1 of formatter and controller PCBs for connecting ground for testing.

5.6.4 SIMPLE VISUAL CHECK FOR +5 VDC SUPPLY

If the ON LED does not light when AC power is applied to the drive and the power keyswitch is ON, check the +5 VDC output of the Regulator PCB. If +5 VD is being supplied, and the other LEDs glow as required, the LED itself may be defective.

5.7 ELECTRICAL CHECKOUT OF REAR PANEL

(Refer to Fig. 8-10, System Wiring Diagram.)

5.7.1 SIMPLE PRELIMINARY CHECK

Does the fan(s) operate when AC power is applied and the keyswitch is ON?

Does an AC test lamp light when plugged into the auxiliary AC receptacles?

If not, use the checkout procedure in the following subsection.

5.7.2 CONTINUITY CHECKOUT OF REAR PANEL WIRING

Equipment Required: VOM (Volt/Ohm Meter)

( ) 1. Disconnect the AC linecord.

( ) 2. Turn the keyswitch ON.

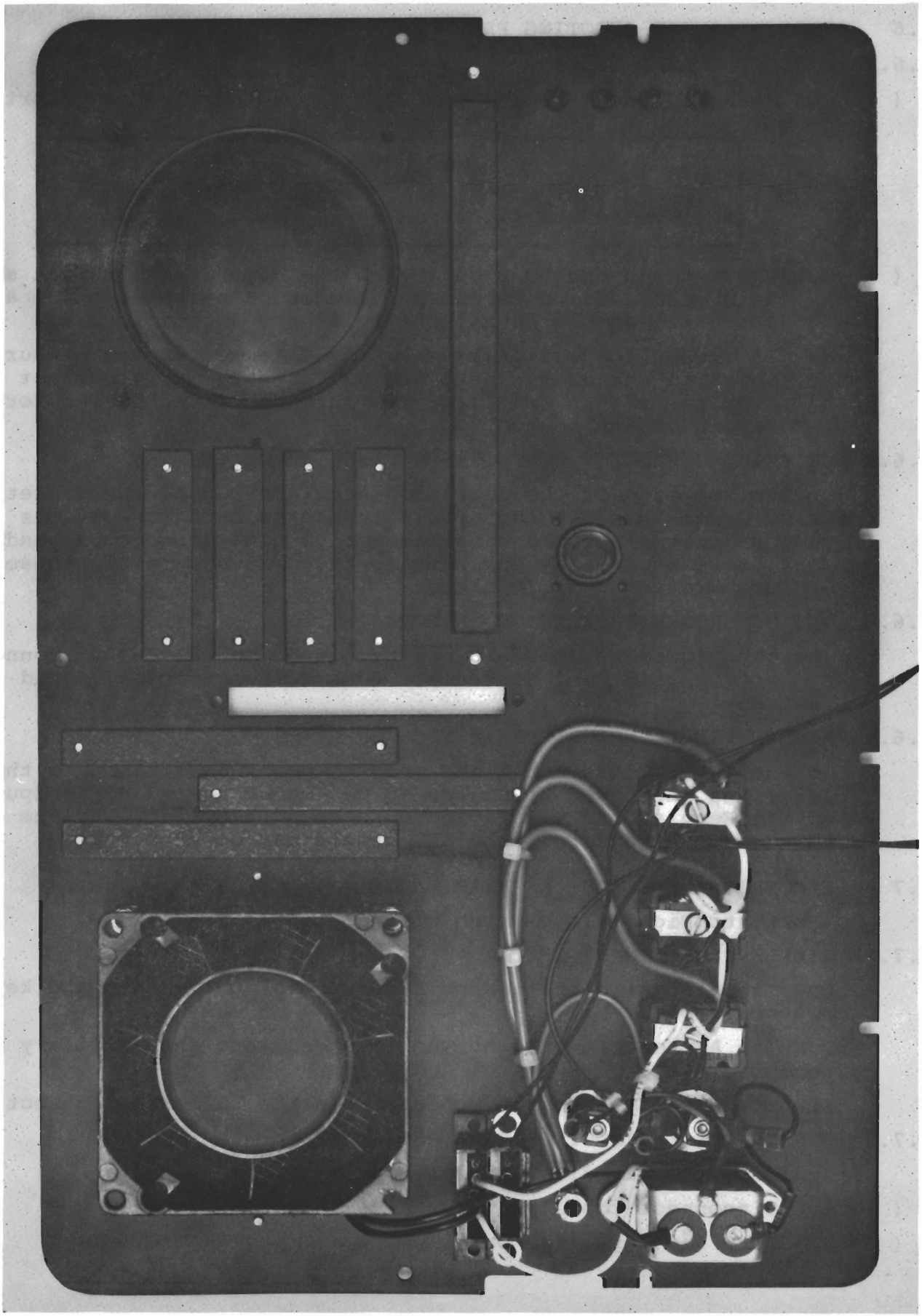


Fig. 5-5 Helios II Rear Panel, Inside View

3. With an ohm meter, set the scale to the lowest range (ohms x 1), measure continuity between ground of the AC input plug (Figure 5-6A, AC Input Plug) and the ground pin of the switched AC receptacles (Figure 5-6B, Switched AC Receptacle). There should be continuity (zero ohms) between these pins. If not, check the actual wiring against the System Diagram, Fig. 8-10.

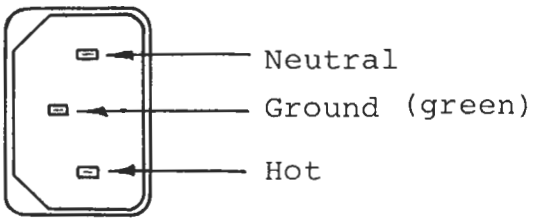


Figure 5-6A, AC Input Plug

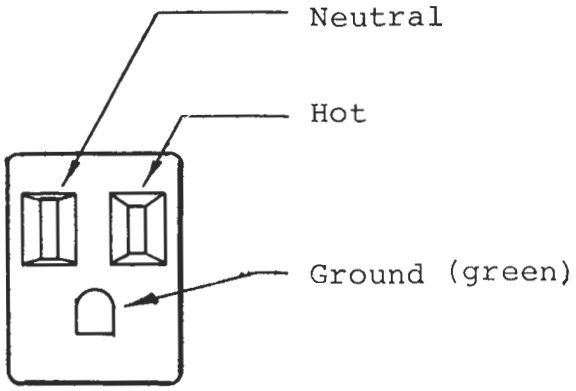


Figure 5-6B, Switched AC Receptacle

( ) 4. With one of the meter leads still on ground of the AC input plug (Fig. 5-6A, AC Input Plug), check for continuity between the hot and neutral pins of each of the switched AC receptacles. There should be no continuity (infinite ohms using the highest range on an ohm meter.) If not, check the wiring against the System Wiring Diagram, Fig. 8-10.

( ) 5. Move the test lead to the hot pin of the AC input plug (Figure 5-6A, Input Plug).

   a. Set the meter to the lowest scale (ohms x 1).

   b. With the other lead, test for continuity between hot pin of the AC input plug and the hot pin in each switched AC receptacle (Figure 5-6B, Switched AC Receptacle). There should be continuity (zero ohms).

   c. If there is no continuity, check for one or more of the following:

      1. Errors in the wiring harness (System Wiring Diagram, Fig. 8-10.

      2. Wires for the keyswitch may be shorted together.

      3. Check to see that good fuses are installed.

( ) 6. Move one test lead to the neutral pin of the AC input plug (Figure 5-6A).

   a. Set the meter on the lowest scale.

b. Check for continuity between the neutral pin of the AC input plug and the neutral pin of each of the switched AC receptacles (Figure 5-6B). There should be continuity.

c. If there is no continuity, check the wiring of the AC Interconnect Cable Assy (Fig. 8-10, System Wiring Diagram.).

( ) 7. Finally, check for continuity among all pins of the AC input plugs (Figure 5-6A). There may be some resistance (approximately 600 ohms) between the hot and neutral because the fan is in the circuit. Check for the following:

Neutral to Ground	Open (infinite resistance)
Neutral to Hot	Approximately 600 ohms
Ground to Hot	Open

5.8 ELECTRICAL CHECKOUT OF REGULATOR PCB

(Refer to Fig. 8-8, Regulator PCB Assembly Drawing, Fig. 8-13, Regulator PCB, Schematic, and Fig. 8-10, System Wiring Diagram.)

CAUTION: Do not check voltages until step 7.

Equipment Required: Voltmeter

( ) 1. Be sure the keyswitch is in OFF position. (Turn keyswitch to counter-clockwise.)

( ) 2. Be sure fuses are in fuse holders.

( ) 3. With keyswitch in OFF position, connect the AC powercord to the AC receptacle on the rear panel.

( ) 4. Plug AC linecord into the 117 VAC outlet.

( ) 5. Inspect the 10-pin connector on the regulator power cable (8 wire) to assure it is wired as shown in Table 5-2, Disk Drive Power Connector Wiring.

> CAUTION
>
> The red (+5 VDC) and white (GND) supplying DC to the indicator panel PCB must be kept apart during the test. If the +5 V touches ground, it will short the 5 V supply.

( ) 6. Turn keyswitch ON.

( ) 7. Measure the voltages at the 10-pin female connector of the regulator PCB wiring harness, at the points indicated in the wiring table. The voltage must be as given in Table 5-2.

Table 5-2 Disk Drive Power Connector Wiring

PIN #	COLOR	VOLTAGE
1	None	NA
2	Red	+5VDC ±.25V
3	Blue	+8VDC Unregulated (7.0V-14.0V)
4	Polarizing key	NA
5	Yellow	+24 VDC ±2.4V
6	White	Ground
7	White	Ground
8	White	Ground
9	White	Ground
10	Green	-5VDC ±.5V

( ) 8. Measure the voltage between the red and white leads supplying DC to the indicator panel PCB. It should be +5 VDC.

> NOTE:
>
> Do NOT take voltage measurements at any other points in the power supply, even though they may be more accessible. It is important that the indicated voltages be available at the connector.

( ) 9. If the power supply fails any of the preceeding test, locate and correct the cause before proceeding.

NOTES

CONTENTS

SECTION 6, MAINTENANCE

NOTES

SECTION 6 MAINTENANCE

6.0 INTRODUCTION

> WARNING
>
> This section contains or refers to routine cleaning, inspections, checks, and tests which the user should perform regularly as specified. The Helios diskette drive is a complex electromechanical device; repair and adjustment is complicated and sensitive. All problems other than those solved by the following cleaning procedures must be referred to the authorized selling dealer.
>
> Repair and readjustment of drives which have been worked on by unauthorized persons, and problems caused by improper adjustment or repair, are not covered under warranty.

Reliability

The Helios diskette drive is designed and constructed to provide a useful life of five years or 15,000 hours, whichever occurs first, before a factory overhaul or replacement is required. Repair or replacement of parts is permitted during the lifetime of the unit.

1. Mean Time Between Failures (MTBF)

   Following an initial period of 200 hours, MTBF should exceed 4,000 hours provided the proper preventative maintenance procedures are followed. The following expression defines MTBF:

$$\text{MTBF} = \frac{\text{Operating Hours}}{\text{No. of Equipment Failures}}$$

   Operating hours mean total "power on" hours less any maintenance time. Equipment failures mean any stoppage or substandard performance of the equipment because of equipment malfunction. Equipment failure excludes down-time or substandard performance caused by operator error, adverse environment, power failure, controller failure, cable failure, use of a defective diskette or other failure not caused by the diskette drive. To establish a meaningful MTBF, operating hours must be greater than 2,500 hours and include all sites where the diskette drives are used. Equipment failures are defined as those failures requiring repairs, adjustments, or replacements on an unscheduled basis, i.e., emergency maintenance required because of hardware failure or substandard performance.

2. Mean Time to Repair (MTTR)

Mean time to repair should be less than 20 minutes and is defined as the time for an adequately trained and competent servicemen with a full contingent of spare parts to diagnose and correct a malfunction.

6.1 RECOMMENDED USER CLEANING

(Refer to Sec. 2 for recommended operating conditions.)

6.1.1 AIR FILTER(S)

(Refer to Fig. 8-5, Rear Panel Assembly, Exploded.)

The metal mesh filter screen and the plastic foam filter element, which comprise the cleanable portions of the Helios air filter, should be inspected and cleaned regularly, as often as required by environmental conditions. Clean as follows:

1. Turn off AC power to the Helios Cabinet. (The fan should not be running without the filter installed.)
2. Remove the screws holding the plastic filter frame.
3. Remove the filter frame.
4. Remove the metal filter screen and the foam filter element.
5. Immerse the screen and the foam element separately in a solution of hot water and mild detergent.
6. Rinse in clear warm water.
7. Wring dry the foam filter element.
8. Dry the parts with compressed air or allow sufficient time to drain and air dry.
9. Put the screen against the outside of the rear panel; put the foam element next, then replace filter frame.

6.1.2 OUTSIDE SURFACES OF THE HELIOS CABINET

(Clean as often as required.)

> CAUTION
>
> Do not use acetone or similar solvent. Acetone will melt the indicator panel screen and probably the paint.

1. Use a damp cloth or sponge to clean dust off the painted metal cabinet surfaces. For stubborn spots, use a mild detergent solution with the cloth or sponge.

2. To clean the plexiglass indicator panel screen, use a cloth or sponge moistened in clean warm or cool water. For stubborn spots, use windex solution, ammonia solution, or 95% isopropyl alcohol solution. (Isopropyl alcohol, called for in this and following procedures, is available at most pharmacies.)

> CAUTION
>
> In any of the cleaning operations, do not use audio/video head cleaner or alcohol with olive oil added.

6.1.3 DRIVE ASSEMBLY SURFACES (Perform as required.)

1. Interior and Exterior Surfaces

   Clean interior and exterior surfaces with a cloth dampened in a solution of 95% isopropyl alcohol.

2. Drive Belt, Drive and Driven Pulleys

   Clean drive belt, drive and driven pulleys with cloth or sponge dampened in a solution of 95% isopropyl alcohol. For small belts and pulleys and hard-to-reach places, use pipe cleaners or cotton swabs (Q-tips).

> CAUTION
>
> Protect the disk drive at all times from dust and dirt which could accumulate and interfere with optical and mechanical components, causing read errors.

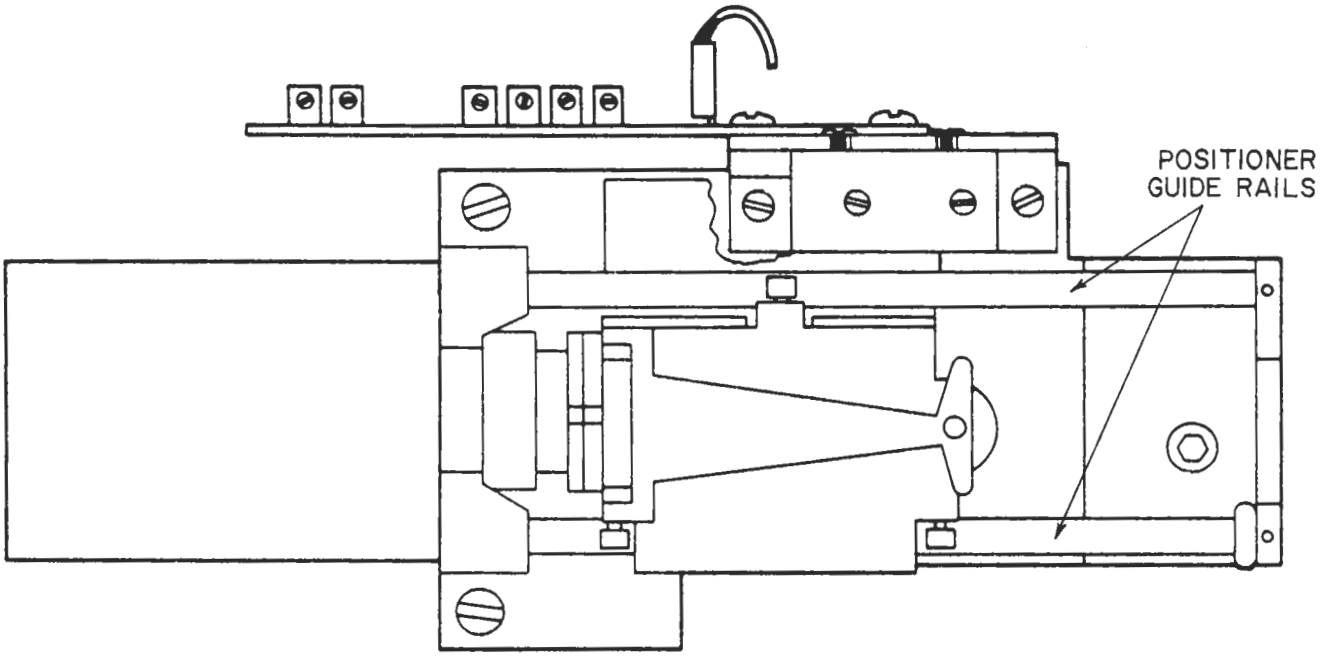


Figure 6-1 Positioner Tracks (Unit Ø).

6.1.4 Positioner Guide Rails (Refer to Fig. 6-1, Positioner Tracks, Unit Ø).

Clean the positioner guide rails with a dry, lint-free cloth, quarterly or as required.

6.2 RECOMMENDED USER CHECKS, INSPECTIONS AND TESTS (Perform Quarterly)

6.2.1 READ/WRITE SYSTEM CHECKS (Quarterly)

1. Examine read/write head for scratches, wear and oxide deposits. Clean if dirty; refer to 6.3.1, Cleaning Read/Write Heads. Worn heads must be replaced by an authorized dealer.
2. Examine pressure arm pad for wear and contamination. (Unit Ø)

6.2.2 QUARTERLY DRIVE SYSTEM TEST

Run the Disk System test (Refer to Section 5, Testing and Trouble-shooting) to verify proper operation of diskette drive or to detect errors which may occur.

6.3 SPECIAL CLEANING PROCEDURES

6.3.1 CLEANING READ/WRITE HEADS

(Perform in conjunction with 6.2.1, Read/Write System Checks.)

1. The unit Ø head is accessible when the top cover of the Helios cabinet is removed. To access the unit 1 head, remove the drive assembly from the Helios cabinet as follows:
   a. Remove the bezel assembly. (Refer to 3.4, Re-Installing the Diskette Drive Assembly, and reverse the procedure.)
   b. Remove the drive assembly reversing the procedure in 3.4, Re-Installing the Diskette Drive Assembly.
   c. Remove the two PCB mounting screws in the lower corners of the Data and Interface PCB.
   d. Lift up the PCB on its hinges to access the head.
   e. Examine pressure arm pad for wear and contamination at this time (unit 1). Worn heads must be replaced by an authorized dealer. Examine unit 1 head at this time.
2. Clean the read/write heads with a lintless gauze wrapped around a clean wooden spatula (popsicle stick or tongue depresser) after moistening the gauze in a solution of 95% isopropyl alcohol. Do not use audio/video head cleaner.
3. After cleaning with alcohol-wetted gauze, clean the head with a dry gauze in the same manner to pick up any residue left when the alcohol evaporates. No residue of lint or alcohol is allowed to remain on the head.
4. Reassemble the drive in the cabinet according to 3.4, Re-Installing the Diskette Drive Assembly.

> CAUTION
>
> After cleaning the heads, perform the Disk System test as in 5.4.1, Recommended Test Procedures, before loading the PTDOS from diskette.

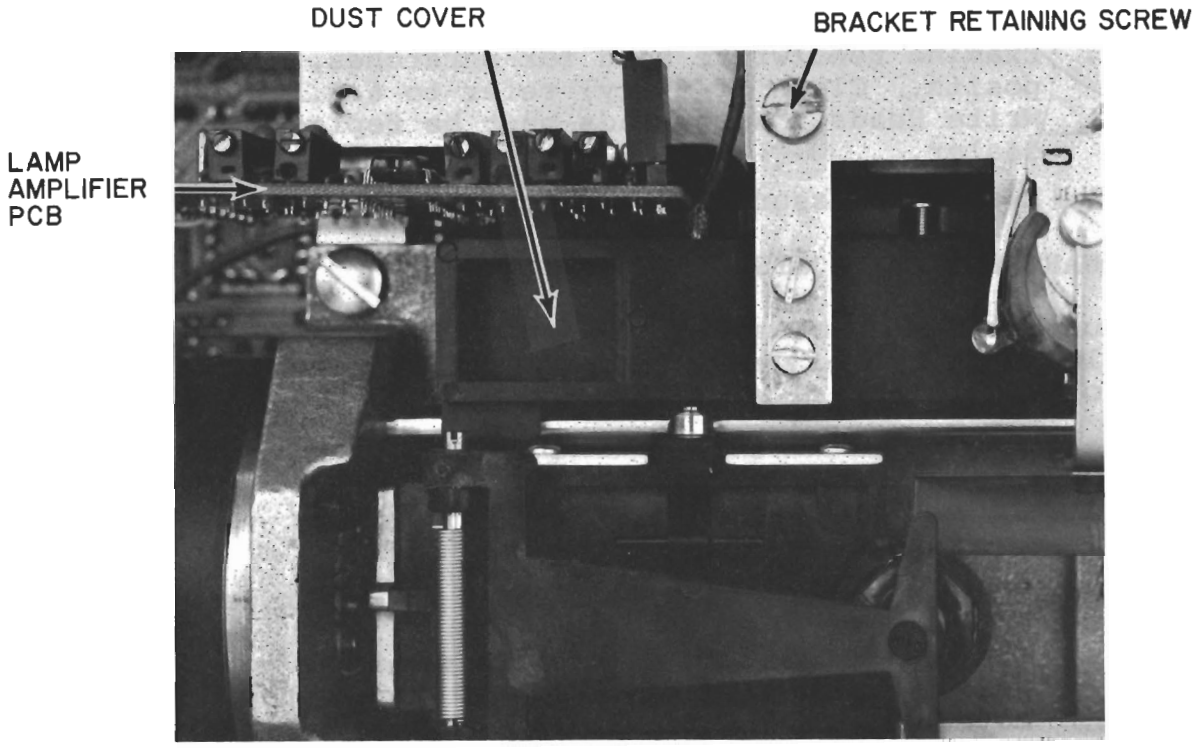


Fig. 6-2 Location of Positioner Scale, Unit Ø

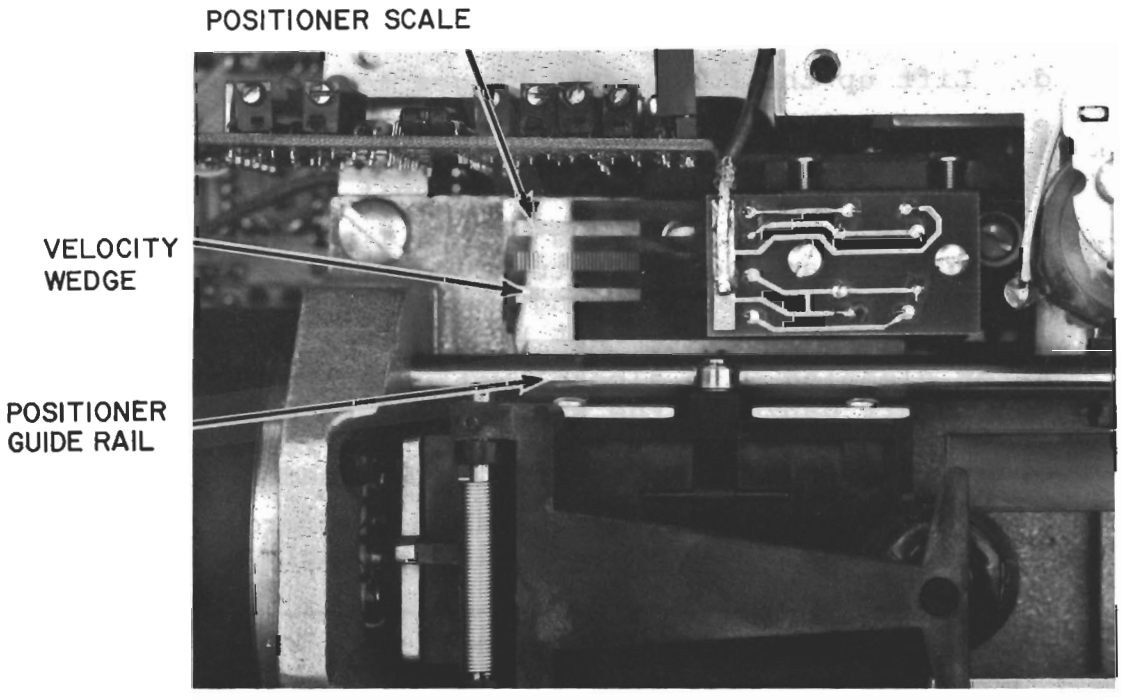


Fig. 6-3 Positioner Scale, Dust Cover Removed

6.3.2 POSITIONER SCALE SURFACES (Refer to Fig. 6.2, "Location of Positioner Scale" and Fig. 6.3, "Positioner Scale, Dust Cover Removed.")

> CAUTION
>
> Do not attempt to adjust the transducer adjustment screws. Do not touch the positioner scale with your fingers or tools. Both the mechanical alignment and the optical cleanliness of the positioner scale are extremely critical.

The positioner scale is a glass plate engraved with a row of precision slots. It is mounted on the carriage which holds the read/write head, below the small horizontally-mounted PCB. It is enclosed by a plastic, rectangular dust shield. Do not remove this dust shield and do not clean the positioner scale surfaces unless a symptom, such as consistent seek errors, indicates that the scale may be dirty. If so clean as follows:

1. The dust shield is held in position over the positioner scale by a small metal bracket which is attached to the dust shield by two 4-40 screws. The bracket is in turn attached to the drive case by a large screw. Remove this screw completely to remove the dust shield.
2. Remove the dust shield.
3. Inspect the scale for foreign particles. If particles are present, use a dry cotton swab to brush off the particles.
4. After cleaning, visually examine the scale for foreign particles again to see if they have been removed. Foreign particles on the clear area of the velocity wedge are particularly detrimental to positioner performance.
5. You will have to slide the carriage back and forth to see all the scale. If the scale is contaminated by film of tobacco smoke or a scum of a substance which cannot be removed by a dry brushing, a cotton swab dampened in 95% isopropyl alcohol can be used as a final resort. Do not use alcohol to which olive oil has been added. Do not use audio/video head cleaner.
6. Replace the dust shield.

> CAUTION
>
> If the air in which the drive is operating contains large amounts of dust, humidity, tobacco smoke, or corrosives, the cleaning intervals may be shorter than the nominal 3 months suggested.
>
> CAUTION
>
> Do not clean diskettes.

6.4 REPLACING DEFECTIVE DIP DEVICES

> **CAUTION**
>
> Do not replace a device thought to be defective on a PCB which is still on warranty. This will void the warranty.

1. Do not replace a DIP device unless found to be defective in the course of troubleshooting the PCB in Section 5, Testing and Troubleshooting.

2. Before replacing a device, read Section 3.2.3, Integrated Circuits, and Section 10.1, Parts List Update Table.

CONTENTS

SECTION 7 THEORY OF OPERATION

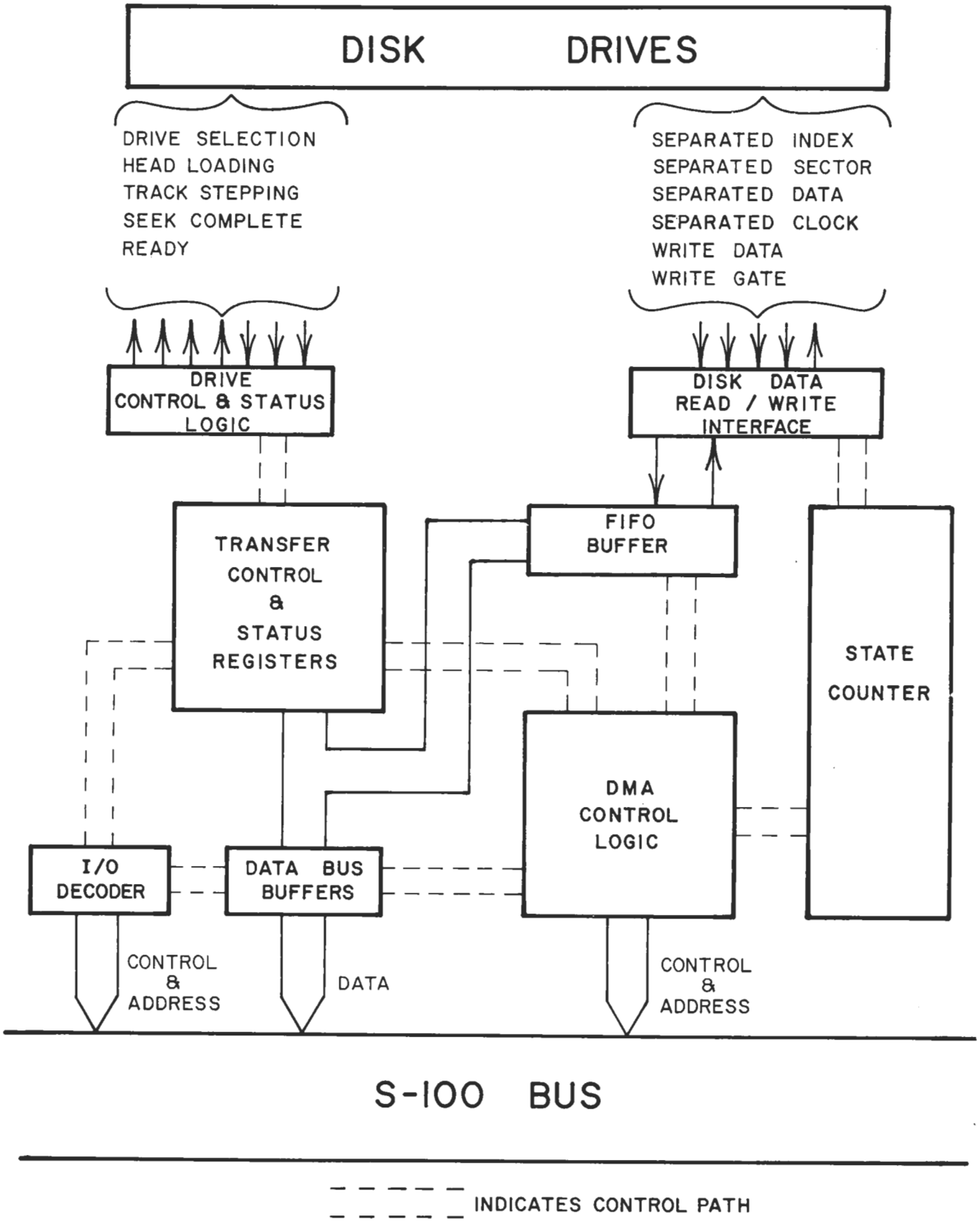


Fig. 7-Ø Controller/Formatter Simplified Block Diagram

SECTION 7 THEORY OF OPERATION

7.0 SCOPE

This section describes the operation of the Helios II hardware. For a discussion of software refer to the PTDOS manual. Discussion of details of operation is abandoned at the boundaries of the IC devices. For a discussion of the internal operation of integrated circuits, etc., refer to the device manuals published by the device manufacturers.* For a discussion of the dual disk drives and their signal definitions, refer to Section 7.12, Diskette Drive, Theory of Operation. For a discussion of the 8080 microprocessor and its signal definitions, refer to the Intel manual, 8080 Microcomputer Systems User's Manual. For a discussion of the S-100 bus, refer to the Processor Technology manual, Sol Systems Manual. S-100 bus signals used by the controller are described briefly in Table 7-7.
For a general overview of the Helios system, refer to Section 1, Introduction, and Fig. 1-1, Helios II System, Generalized Block Diagram.

7.1 GENERAL FUNCTIONAL DESCRIPTION OF THE Helios SYSTEM

Communication between the disks and the host computer can be thought of as being of two kinds: control, and data transfer. Data transfer and storage are the purposes of the floppy disk system. Control communication is the means by which data transfer is described and executed. In the Helios II system, data transfer is done via Direct Memory Access (DMA).

7.2 DISTRIBUTION OF FUNCTIONS

(Refer to Fig. 7-Ø, Controller/Formatter Simplified Block Diagram.)

Table 7-1, Distribution of Helios II Functions, lists the functions which must be performed by a floppy disk system, and indicates the parts of the system which are responsible for each.

Fig. 8-16, Pin-to-Pin Signal Flow Diagram, shows all the signals among the major subsystems, by name and pin number. It also shows the direction of travel of the signals and groups them by general functions such as clocks, controls, status, error reports and data.

Fig. 8-17, System Block Diagram, attempts to group the circuits found on the schematics into functional blocks. It groups signals by their connectors and their direction of travel in the system. It shows the major signals among the functional blocks within a PCB.

*Note: Pin configurations for ICs used in the Helios are given in the Appendix, Section 9.

Table 7-1 Distribution of Helios II Functions

FUNCTIONS:	Software	Controller	Formatter	Disk Drive
Disk insertion, retention, ejection				X
Disk rotation and speed control				X
Track selection (mechanical)				X
Head loading (mechanical)				X
Index and sector sensing (optical)				X
Index and sector separation				X
Clock and data recording (magnetic)				X
Clock and data reading (magnetic)				X
Clock and data separation				X
Read data conditioning			X	
Read clock conditioning			X	
Sector control			X	
Format control			X	
Write signal generation			X	
Redundancy checking			X	
Interfacing to CPU (Via I/O Port)		X		
Interfacing to memory (Via DMA)		X		
Transfer address storage and counting		X		
Transfer length storage and counting		X		
Disk Drive Selection and Control		X		
Write clock generation		X		
Ready reporting		X		X
Error reporting		X	X	
Data buffering		X		
Serial/Parallel and Parallel/Serial Conversion		X		
Head load Management	X	X		
Track Management	X			
Sector Management	X			

7.3 COMPUTER I/O PORTS ASSIGNED TO TRANSFER AND CONTROL OF TRANSFER

Control communication for DMA transfers is done via input and output commands addressed to ports FØ through F7. No other S-100 devices in the system may use ports numbered FØ through F7. Refer to Table 7-2, Input/Output Port Assignments.*

To transfer data the CPU must describe the transfer via the various output ports, execute the transfer via port F1, and periodically examine the progress of the transfer by input via port FØ until it is judged to be complete, or defective.

Ports F3 and F4 are used to output 16 bits (only 12 used) which specify the number of bytes in the transfer. Ports F5 and F6 are used to output 16 bits which specify the starting address of memory to be used in the transfer. Port F7 is used to output control bits to the disk drives. These bits specify unit selection, head loading, and track selection. Port F1 defines the transfer as read (from disk) or write (to disk), and as header (identification) or data block (the data itself). Port F1 also defines when or whether to execute the transfer. Tables 7-3 through 7-5 show the bit assignments for ports FØ, F1 and F7.

TERMINOLOGY NOTE

The term "binary" is used to signify a flipflop. "FF" is an abbreviation of "flipflop."

The term "DMA controller" means those portions of the controller logic which have been identified as "DMA transfer" and "hold sequence" logic.

"Disk drive" is taken to mean "diskette drive." Similarly, "diskette is sometimes referred to as "disk."

*For test purposes, primarily, individual controllers can be jumpered to respond to ports EØ through E7 instead.

Table 7-2 Input/Output Port Configuration

PORT #	FUNCTION	DIRECTION RELATIVE TO COMPUTER
FØ	Status	Input
F1	Transfer command	Output
F2	Spare	-
F3	Transfer length, low order byte	Output
F4	Transfer length, high order byte	Output
F5	Transfer address, low order byte; clears the status register	Output
F6	Transfer address, high order byte	Output
F7	Drive Command	Output

Table 7-3 Port FØ Status Bit Assignments

BIT	SIGNAL NAME	ACTIVE STATE		SIGNIFICANCE
Ø	TC	high	=	transfer complete
1	SREADY	high	=	ready
2	ABORT	high	=	error
3	CRC ERROR	high	=	error
4	CRC CHECKED	high	=	check complete
5	$\overline{\text{DISK READY}}$	low	=	ready
6	$\overline{\text{SEEK COMPLETE}}$	low	=	done
7	$\overline{\text{INDEX}}$	low	=	index hole present

Table 7-4 Port F1 Transfer Command Bit Assignments

BIT	SIGNAL NAME	ACTIVE STATE		SIGNIFICANCE
Ø	$\overline{\text{ERASE}}$	low	=	erase
1	R/$\overline{\text{W}}$	high	=	read
		low	=	write
2	$\overline{\text{TR DATA}}$	high	=	header
		low	=	data
4, 5, 6, 7	Don't care, ever			

Table 7-5 Port F7 Drive Command Register Bit Assignments

BIT	SIGNAL NAME	ACTIVE STATE		SIGNIFICANCE
Ø	$\overline{\text{STEP}}$	low	=	Do step
		high	=	Do not step.
1	$\overline{\text{INWARD}}$	low	=	away from track Ø
		high	=	toward track Ø.
2	$\overline{\text{DRIVE SELECT 1}}$	low	=	select unit 2, 3, 6, or 7
		high	=	select unit Ø, 1, 4 or 5
3	$\overline{\text{DRIVE SELECT 2}}$	low	=	select unit 4, 5, 6, or 7 (cabinet 2)
		high	=	select drive Ø (units Ø & 1) and drive 1 (units 2 & 3) (the drives in cabinet 1)
4	$\overline{\text{RESTORE}}$	low	=	go to track Ø
		high	=	not active
5	$\overline{\text{LOAD HEAD Ø}}$	low	=	load head of unit 0, 2, 4 or 6
		high	=	not active
6	$\overline{\text{LOAD HEAD 1}}$	low	=	load head of unit 1, 3, 5, or 7
		high	=	not active
7	$\overline{\text{SELECT DISK 1}}$	low	=	select units 1, 3, 5 or 7
		high	=	select unit 0, 2, 4 or 6

7.4 DISK RECORDING FORMAT

7.4.1 OVERVIEW

(Refer to Figs. 7-1, 7-2, and 7-3.)
Helios II uses a combination of hard sectoring and soft sectoring techniques to provide a recording format with variable block length and optimum utilization of disk capacity.

There are 77 tracks per disk. Each recorded block lies entirely within a single track.

Data is recorded on the disk in 8-bit bytes serially by bit, at a rate of 250K bits/second, the most significant bit first. The recording technique consists of a stream of clock pulses combined with data pulses which are written midway between clock pulses. A binary Ø is represented by a pair of clock pulses with no data pulse between them. A binary 1 is represented by a pair of clock pulses with a data pulse at the midpoint. The clock pulses are normally written continuously since they are used for synchronization at the bit level. Missing clocks are not a normal occurrence, but are intentionally created to help identify the various parts of a block recorded on the disk. Refer to Fig. 7.2 and 7.3.

There are 32 "hard sector marks"* per revolution of the disk. There is one index mark which lies midway between two of the hard sector marks. The hard sector mark immediately after the index mark is sector mark Ø.

Only 16 of the hard sector marks are used. These are the alternate ones, starting with sector mark Ø. These 16 are numbered Ø through 15. The other 16 are completely ignored.

A block is a recording of data prefixed by some identification. All recording is done in blocks. A block always begins on a sector mark and always ends on a sector mark. Its length may be as short as 1 sector mark interval (1/16 revolution) or as long as 13 sector mark intervals.

Blocks may begin on any sector mark and may end on any sector mark, but must observe the following rule: No block may cross sector mark Ø. Stated another way, sector mark zero must be the start of some block, and the end of some block.

Each sector as yet unrecorded with data is primitively formatted by the system into blocks one sector interval long. The optimum packing scheme available to the software (highest density) is two blocks per track each 8 sectors long.

7.4.2 FORMAT WITHIN A BLOCK

(Refer to Fig. 7-1, Format Within A Block.)

A block is made up of 5 parts. These are: preamble of header (16 bytes), header (16 bytes), preamble of data (16 bytes), data (variable length), and postamble (variable length). The

*"Hard Sector mark" means physical holes are formed in the diskette to provide a reference for the electro-optics.

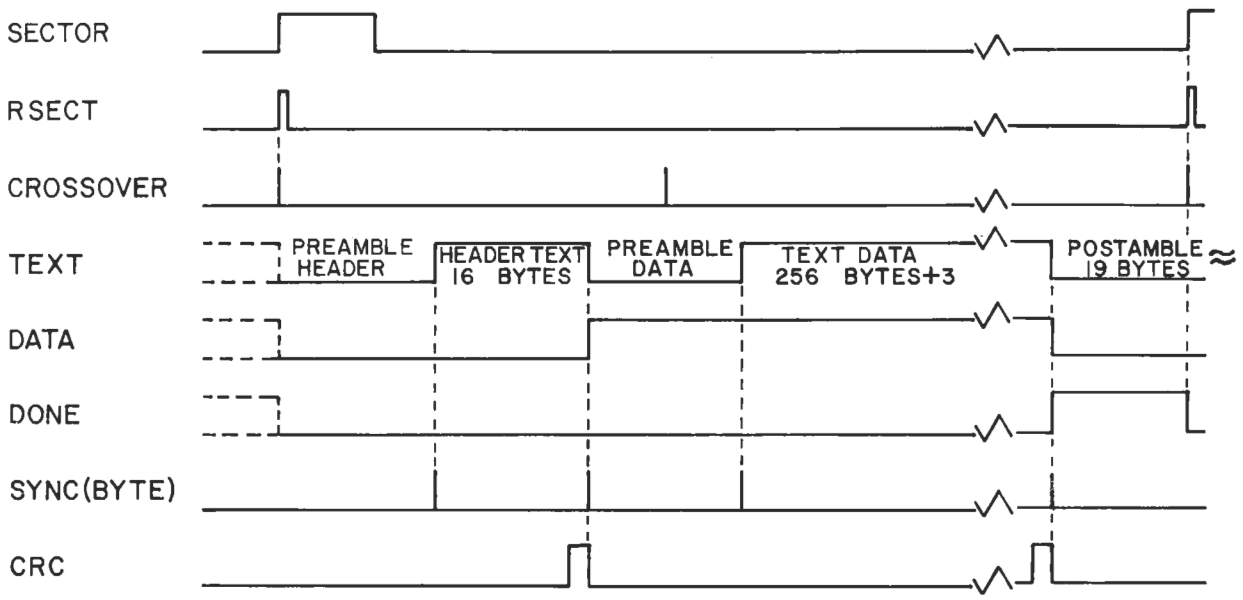


Fig. 7-1 Format within A Block

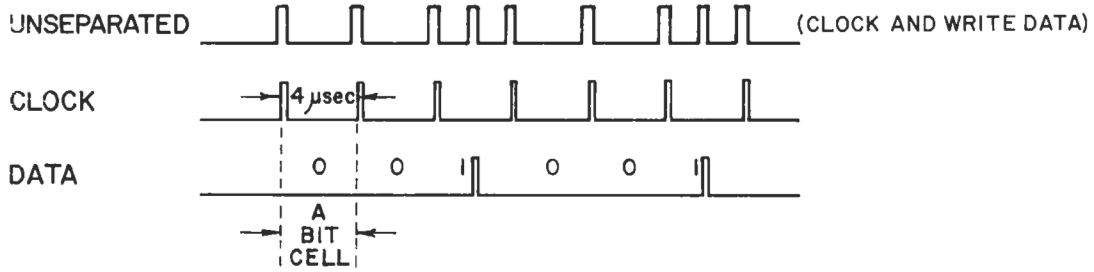


Fig. 7-2 Normal Stream of Clock/Data

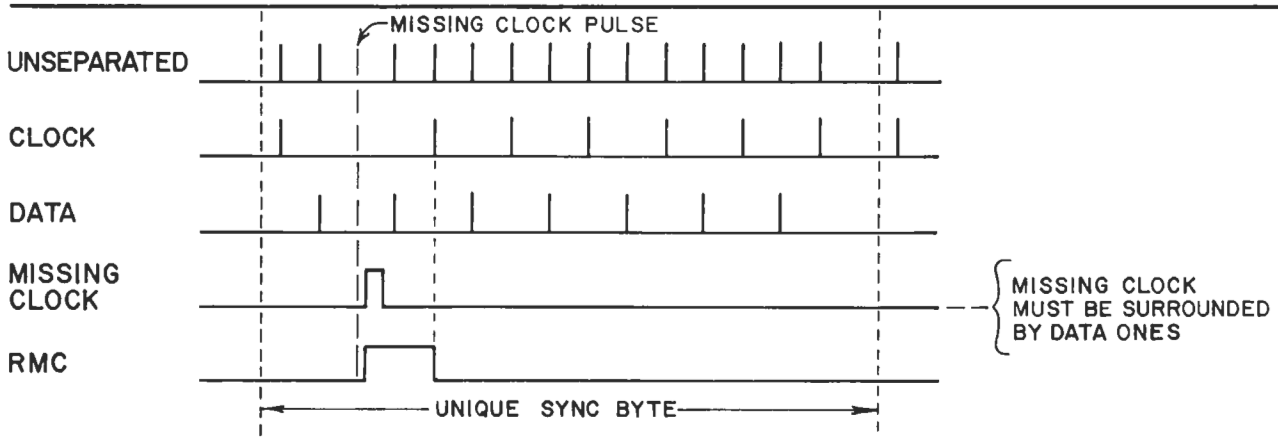


Fig. 7-3 Unique Sync Byte

data part contains the actual memory image. The header contains identification and other information about the data. The postamble is whatever is left over before the next sync mark.

"Sync mark" is described in the following paragraphs.

Starting at a sector mark the preamble of header is 15 bytes recorded as zeros, followed by 1 sync byte. The header is recorded as 13 bytes of ID., 2 bytes of CRC, and 1 sync byte. The preamble of data is recorded as 11 bytes of zeros before CROSSOVER, 4 bytes of zeroes after CROSSOVER, and 1 sync byte. Data is recorded as a variable number of bytes followed by 2 bytes of CRC and one sync byte. The postamble is recorded as zeros until the next sector mark.

The pulses of the signal SYNC (sync mark) in Fig. 7-1, Format Within A Block, are generated by single bytes which mark the boundaries of the various parts of a block. These bytes contain the data FE_{16} and are made unique by suppressing the second of the 8 clocks which normally accompany a byte. (Refer to Fig. 7-2, Normal Stream of Clock/Data and Fig. 7-3, Unique Sync Byte.)

7.4.3 PROVISIONS FOR VARIATIONS IN DISK SPEED

A block is written in two sections; these parts are written at two different times. The boundaries between these two recordings are called crossovers. Within each recording, clocks and data bits are recorded continuously in a coherent pattern. At each crossover there will be a discontinuity due to variations in disk rotary speed at the times the crossovers occur. At each such discontinuity, the circuitry which separates clock and data will lose synchronism. The Preambles provide time for this circuitry to regain synchronism, and as a tolerance for variation in disk rotary speed and sector detector timing.

7.5 CYCLICAL REDUNDANCY CHECKING

Cyclical redundancy checking is a technique for detecting errors in the recorded data as they are read. Helios II provides cyclical redundancy checking in hardware. The pulses marked CRC in Fig. 7-1, Format within a Block, are 2 bytes where the redundancy data is recorded.

7.6 SIGNAL FLOW AND SIGNAL IDENTIFICATION IN THE Helios SYSTEM

For an overall picture of the signal flow in the Helios system, refer to Fig. 8-16, Pin-to-Pin Signal Flow Diagram. For numerical pin-to-pin assignments between the controller and formatter, see Table 8-1. For numerical pin-to-pin assignments among the controller, drive and indicator panel, see Table 8-2. For numerical pin-to-pin assignments and functional descriptions of signal between the controller and the S-100 backplane, see Table 7-7. For functional block diagrams of the controller/formatter, see Figs. 7-Ø and 8-17. Schematic diagram for the controller, formatter, indicator panel and regulator PCBs are in Section 8, Drawings. Schematic diagrams for PCBs internal to the diskette drive assembly are in the Helios II Service Manual.

7.7 GENERAL DESCRIPTION OF CONTROLLER FUNCTIONS

(Refer to Fig. 7-Ø, Controller/Formatter Block Diagram and Fig. 8-11, Controller PCB, Schematic.)

The controller is the heart of the Helios system and acts as a processor taking over control of the S-100 bus to transfer data directly to/or from memory (although in close coordination with the CPU). This not only provides for fast loading and unloading of the memory but also leaves the CPU free for other tasks, by buffering the relatively slow moving diskette drive.

7.7.1 CLOCKS

The Clock Generator/Multiplexer on the block diagram represents the functions of the controller clock circuitry.

Helios II uses the S-100 Phase 2 clock (Φ2) when writing on diskette, and uses a clock signal resulting from reading the disk ($\overline{\text{RCLOCK}}$) at other times. $\overline{\text{RCLOCK}}$ has a period of about 4 µs, but varies with disk rotary speed. Φ2 has a period of .5 µs (crystal controlled) and is counted by a modulo-8 counter and

and decoded into 4 signals called $\overline{\text{CLOCK Ø}}$, $\overline{\text{CLOCK 2}}$ and $\overline{\text{CLOCK 4}}$. These signals are .5 µs pulses at 1 µs intervals. Each has a repetition period of 4 µs.

The clock multiplexer selects either $\overline{\text{RCLOCK}}$ or $\overline{\text{CLOCK 4}}$ to produce MAIN CLOCK. $\overline{\text{RCLOCK}}$ originates on the formatter PCB. (Refer to 7.8.1, Data and Clock Conditioners.)

7.7.2 I/O PORT DECODER

The I/O Port Decoder on the block diagram represents the functions of I/O Port Decoder logic and circuitry.

I/O instructions controlling data transfers is done by input/output. The necessary ports are decoded here. Seven outputs of this decoder activate various data connections as requested. We will examine these. For port assignments refer to Table 7-2, I/O Port Configuration.

F7 - The DISK COMMAND STROBE causes control information destined for the disk drives to be taken from the DO bus, and latched into the disk command register. Disk command buffers drive the lines of the disk control cables between Controller P2 and the diskette drive P1.

F6 - The INITIAL ADDRESS, HIGH ORDER BYTE STROBE causes the high half of the initial address to be taken from the DO bus and latched into the high half of the address counter.

The initial address is the first address to be used in a forthcoming transfer of data.

F5 - The INITIAL ADDRESS, LOW ORDER BYTE STROBE causes the low half of the initial address to be taken from the DO bus and latched into the low half of the address counter.

F4 - The TRANSFER LENGTH, HIGH ORDER BYTE STROBE causes the high 4 bits of the transfer length to be taken from the DO bus and latched into the transfer length counter. The transfer length is the number of bytes to be moved in such a transfer.

F3 - The TRANSFER LENGTH, LOW ORDER BYTE STROBE causes the low 8 bits of the transfer length to be taken from the DO bus and latched into the transfer length counter.

F1 - The TRANSFER COMMAND STROBE causes the transfer command (4 bits) to be taken from the DO bus and latched into the transfer command register. The transfer command causes the transfer of data to occur. All the other ports merely describe features of a transfer.

FØ - The STATUS REPORT STROBE causes the 8 status bits to be enabled onto the DI bus. This is an input to the CPU, while all the other ports are used as outputs. Four of the status bits which are reports on the progress of a DMA transfer are latched in the status register as they

occur. This register is cleared by the INITIAL ADDRESS, LOW ORDER BYTE STROBE.

7.7.3 STATUS MULTIPLEXER

The status signals SELECTED HEAD LOADED and SELECTED DISK READY are selected by the Status Multiplexer. This selection is based on the disk command register bit SELECT DISK 1. This bit determines left/right selection within one dual drive.

The status signal SREADY means that the controller is ready.

7.7.4 DMA HOLD SEQUENCE LOGIC (DMA TRANSFER)

The DMA transfer logic controls the details of moving data between memory and disk. To perform such a transfer, the DMA controller, with permission from the CPU, suspends the operation of the CPU and puts itself in the place of the CPU, interacting with the S-100 bus as required to accomplish the appropriate memory operations.

DMA operations are done in bursts of about 12 bytes. The exact number varies, but 12 is typical. DMA operations proceed at 1.5 µs per byte.

7.7.5 FIFO DATA BUFFER

A FIFO data buffer (two 9403 ICs) performs the temporary storage and serial/parallel and parallel/serial conversions necessary to interface the serial-by-bit format of the disk to the byte burst format of the memory.

7.8 GENERAL DESCRIPTION OF FORMATTER FUNCTIONS

(Refer to Fig. 7-Ø, Controller/Formatter Block Diagram and Fig. 8-12, Formatter PCB, Schematic.)

7.8.1 DATA AND CLOCK CONDITIONERS

The signals -SEPARATED CLOCK and -SEPARATED DATA originate at the data separator in the selected disk drive. The data conditioner latches the data bits to form the signal RDATA and its inverse. The clock conditioner is a oneshot which extends each clock pulse to .9 µs. $\overline{\text{RCLOCK}}$, P3, Pin 22 goes to the controller board where it passes through a multiplexer (except when writing) and returns to this board as MAIN CLOCK.

7.8.2 MISSING CLOCK DETECTOR

The missing clock detector monitors MAIN CLOCK for gaps and supplies the signal MISSING CLOCK if a MAIN CLOCK pulse is missing. MISSING CLOCK is a short pulse. $\overline{\text{RMC}}$ is a latched version of it. These signals are used for sync detection and CRC checking. MISSING CLOCK is ORed with SEPARATED CLOCK by the clock conditioner.

7.8.3 SYNC DETECTOR

The sync detector recognizes the special sync byte by examining every byte containing a missing clock. (Refer to Fig. 7-1,

"Format Within a Block" and Fig. 7-3, "Unique Sync Byte.") It generates a signal called SYNC when a sync byte is found. It generates a signal called SYNC ERROR if a sync search exceeds its limit without finding a sync byte.

7.8.4 SECTOR/INDEX LOGIC

The signals -SEPARATED SECTOR and -SEPARATED INDEX originate in the selected disk drive. They are used by the sector reset logic to generate a formatter reset signal RSECT and an error report $\overline{\text{OVERINDEX}}$.

7.8.5 STATE COUNTER LOGIC (Refer to Fig. 7-4, State Counter Logic.)

A. The State Counter

Format is generated, interpreted and controlled by a 12 bit state counter. When writing on disk, this counter generates the format. When not writing, this counter uses the read signals to keep itself in step with the format passing the read head. If no head is loaded, if the head is off track, or no disk loaded, etc., the formatter is not be able to keep itself in step with read format. In such a case it is said to be "out of sync." The signal SYNC ERROR (from the Sync Detector) is a report of this.

The state counter is reset to its initial condition by RSECT at a sector mark.

The state counter is divided into 3 sections. The first of these is called the bit counter (BC). It counts 8 bits per byte. The second section is called the punctuation counter (PC). It counts the number of bytes in each section of a block. (The sections are: preamble of header, header, etc.) Sixteen is a typical number of bytes. The third section is called the construction counter (CC). It counts the 5 sections of a block.

B. The State Decoders and Jump Logic

The state decoders and the jump logic generate the signals needed to control the variable features of the state counter, and generates the format signals needed by the rest of the formatter and by the controller.

7.8.6 CRC GENERATOR/DETECTOR AND WRITE MULTIPLEXER

The CRC generator and detector generates the two check bytes at the end of each message when writing, and makes the check on each message when reading.

The write multiplexer generates the write signal for the disk drives by selecting data bits, and clocks, and suppressing "missing clocks" in the correct sequence.

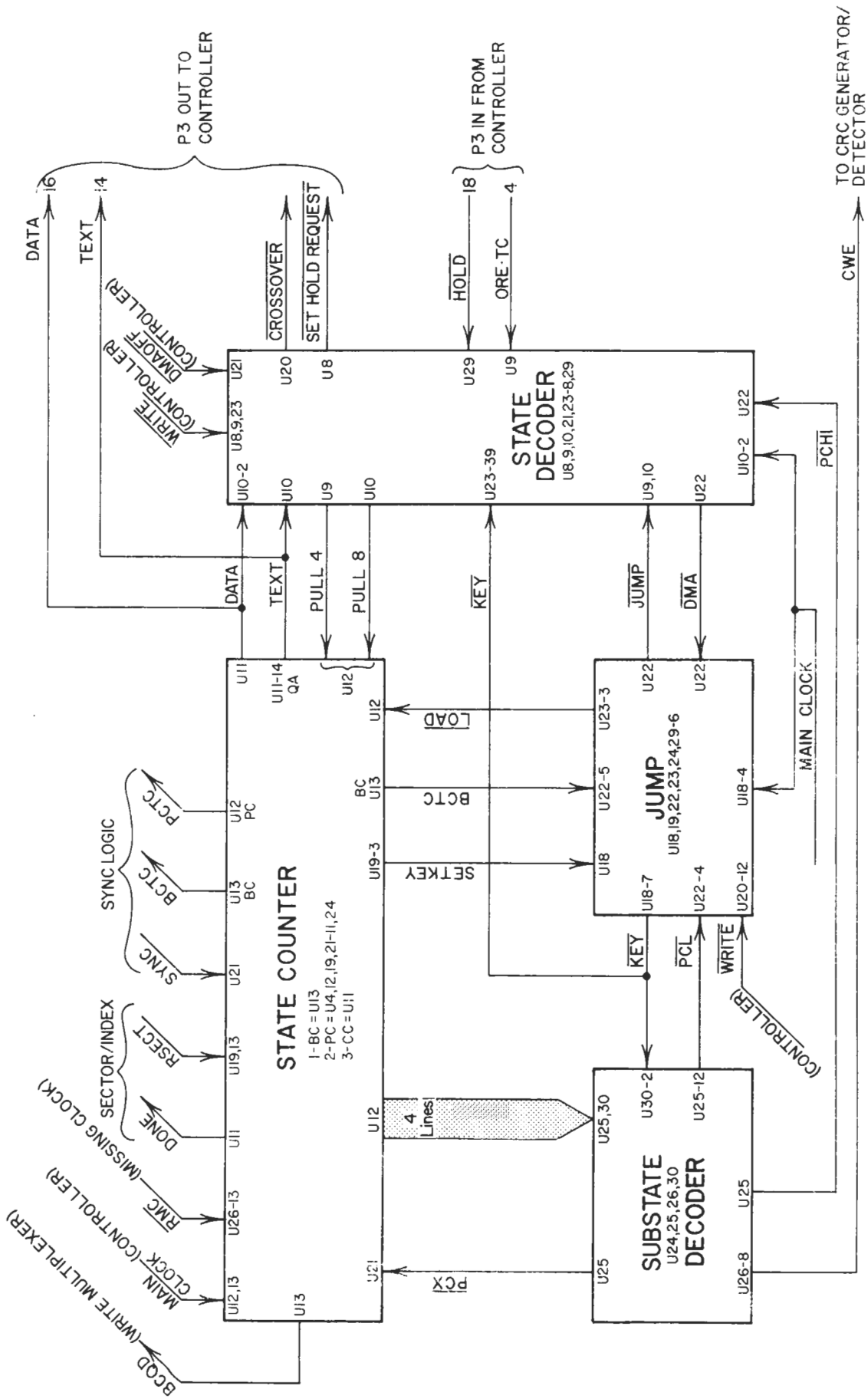


Fig. 7-4 State Counter Logic, Block Diagram

7.9 DC POWER REQUIREMENTS

7.9.1 CONTROLLER PCB (Refer to Fig. 8-11, Controller PCB, Schematic.)

The controller power supply requires an unregulated DC voltage in the range 7.5 volts to 10 volts at 1.6 amps. The controller has 2 on-board regulators and a heat sink. It requires forced air cooling.

U54 and U55 are +5 volt integrated regulators. They supply two SEPARATE +5 volt lines which supply the various ICs in two groups.

> CAUTION
>
> Do not connect these two +5 volt lines together. To do so may overload one of the regulators, or may cause them to oscillate.

C8 is an electrolytic capacitor across the unregulated supply. It provides local energy storage to minimize the effects of any short disturbances on the unregulated supply and to prevent oscillation of the regulators.

C9 and C23 are electrolytic capacitors across the two regulated supplies. They provide regulation at high frequencies beyond the range of the regulators, and take part in preventing oscillation by the regulators.

The remaining capacitors across the power supplies are ceramic capacitors. They provide regulation at still higher frequencies which are beyond the effective range of electrolytic capacitors. They are distributed about the board so as to minimize the effects of inductance of the circuit traces as impedance common to more than one device.

7.9.2 FORMATTER PCB (Refer to Fig. 8-12, Formatter PCB, Schematic.)

The power supply of the formatter is similar to that of the controller. It requires only 0.6 amps, and has only 1 regulator. It requires no heat sink other than the board itself. Its unregulated supply may be obtained from the S-100 bus, or from the external supply connector P2. The formatter does not use any S-100 bus signals, and P2 makes it possible to mount it somewhere other than in an S-100 bus connector. (Refer to 3.5, Optional DC Power for Formatter PCB.)

7.10 FUNCTIONAL CIRCUIT ANALYSIS OF THE CONTROLLER

(Refer to Fig. 8-11, Controller PCB Schematic and Fig. 8-17, System Block Diagram.)

7.10.1 COMMUNICATION OF CONTROL AND STATUS

A. Clock Generator/Multiplexer

The clock signal Φ2 (S100-24) is inverted by the Schmidt trigger U7-4. This signal is counted by U5. The first three outputs of this counter repeat their pattern every eight counts. These eight states can be numbered Ø through 7. U14 decodes states Ø, 2 and 4 to form the signals $\overline{\text{CLOCK Ø}}$ at U14-12, $\overline{\text{CLOCK 2}}$ at U14-11, and $\overline{\text{CLOCK 4}}$ at U14-10. The two inverters (U6-12 and U6-10) provide delay to prevent decoding spikes at the outputs of U14.

$\overline{\text{RCLOCK}}$ (P3-22) originates in the formatter. It is derived from a clock signal read from disk. Multiplexer U11-4 selects and inverts $\overline{\text{CLOCK 4}}$ when writing on disk, or $\overline{\text{RCLOCK}}$ when not writing, to form MAIN CLOCK. Buffer U9-5 drives P3-36 to send MAIN CLOCK to the formatter.

The clock signals just described are used throughout the system.

B. I/O Port Decoder

1. Data transfer by Helios II is controlled by input and output operations addressed to ports FØ through F7. Refer to Table 7-2, I/O Port Configuration, for the details of these port assignments. U42 decodes 8 port strobe signals from the 3 lowest order S-100 address lines (U42 pins 1, 2 and 3) when allowed by enable signals (U42 pins 4, 5 and 6).

2. Address A3 (S-100 pin 31) drives U42-5, enabling U42 when low.

3. Address A4 (S-100 pin 30) is inverted by the Schmidt trigger U7-12, applied to selector pin EX and inverted again by inverter U6-6 whose output is applied to selector pin FX. Normally selector pin C will be jumpered to selector pin FX to chose ports FØ through F7. The user may chose to cause this board to respond to input and output to ports EØ through E7 by moving the jumper so that it connects selector pin C to selector pin EX. This makes it possible to operate two controllers in the same S-100 computer.* Processor Technology software assumes the board is wired C to FX. Selector pin C drives U23-5 enabling if high. Address A5 (S100 pin 29) enables U23-4 if high. Address A6 (S100 pin 82) enables U23-1 if high. Address A7 (S100 pin 83) enables U23-2 if high. If all 4 inputs to the gate U23-6 are high, then U23-6 will be low, and will enable U42-4.

*This feature can be used for test purposes. The present PTDOS cannot operate with 2 controllers. One controller handles up to 4 dual drives.

4. The 5 inputs to U42 just discussed cause the selection of one or none of the 8 outputs. The activation or strobing of the output is done by the signal at U42-6. This signal is described next.

5. U8-6 is a 4-input andgate with inverted output. It has hysteresis inputs for noise immunity. U8-1 is driven by PDBIN, S-100 bus pin 78. U8-2 is driven by SINP, S-100 bus pin 46. SINP identifies an input cycle, and PDBIN describes the time during which input data is to be enabled to the DI bus. U8-5 is driven by $\overline{\text{PHLDAR}}$. It is used here to prevent any port strobes from ocurring as an unintended result of a DMA transfer. No input/output activity is intended during DMA transfers.

6. U8-4 is driven by Φ2. In some machines, PDBIN and SINP deliver noise pulses due to crosstalk with other signals. Use of Φ2 here suppresses this noise while allowing normal operation. This use of Φ2 has caused malfunction in some systems using the Z80 microprocessor, and can be disabled by inserting U8 with pin 4 bent under so that it makes no connection.

   When these 4 inputs are all high, U8-6 will be low.

7. U8-8 is a gate similar to U8-6. It produces output strobes. U8-9 is wired always enabled. U8-10 is driven by $\overline{\text{PHLDAR}}$ to prevent port strobes during DMA transfers. $\overline{\text{PWR}}$, S-100 bus pin 77, is inverted by the hysteresis inverter U7-2, which in turn drives U8-12. SOUT, S-100 bus pin 45 drives U8-13.

   When these 4 inputs are all high, U8-8 will be low.

8. U21-6 is an OR gate with inverted inputs. It is driven by U8-6 and U8-8. If either of these signals goes low, U21-6 will go high. U21-6 drives U42-6, the strobe input of the port decoder. Note that the port decoder does not distinguish between inputs and outputs. To avoid errors, the software sends inputs or outputs as are appropriate to the particular port assigned to the selected function.

C. Internal Data Bus

The 8 bits of the S-100 data output bus DO-Ø through DO-7 are copied onto an internal data bus by the 8 receivers of U47 and U48. This internal bus is used throughout the controller wherever access to DO bus data is needed.

D. Disk Command Logic (Output Port F7)

1. The signal $\overline{\text{DISK COMMAND}}$ is produced by the I/O Port Decoder at U42-7. It is applied to the inverter input U6-3. The signal DISK COMMAND is produced at inverter output U6-4, and is applied to U21-1 enabling gate U21-3. If DO-Ø (S-100 pin 95) is low, U21-2 is high, and a low pulse will occur at U21-3. This is applied to buffer

input U46-12. Buffer output U46-11 produces the signal -STEP (P2-36). This is the step command to the disk drive.

2. The signal DISK COMMAND is also applied to the clock input U10-4 of a binary, and to the clock input U31-9 of a 6 bit latch. These 7 binaries make up the disk command register. The rising edge of the signal DISK COMMAND causes this register to store the 7 bits of data DO-1 through DO-7.

   The meanings of these 7 bits are given in Table 7-5, Disk Command Register Bit Assignments.

3. The buffer U9-7 and the 6 buffers of U32 drive these signals onto 7 pins of P2. These 7 signals and -STEP all go to the disk drive. Refer to 7.12, Drive Theory of Operation, for the definitions of these signals. Note that PerSci documentation defines them as active low signals. Wherever these signals appear on Processor Technology documentation they are prefixed with a minus sign.

E. Address Counter (Output Ports F6 and F7)

1. U24, U25, U26 and U27 form the address counter. A starting address can be loaded into the address counter in two halves by executing output instructions. OUT F5 is executed with the low order half in the accumulator. The processor executes an output operation, placing the accumulator contents on the DO BUS and F5 on the low half (also on the high half) of the address bus. The port decoder responds to these signals, as previously described, by producing a negative pulse at U42-10. The low half of the starting address appears on the internal data bus which drives the input pins of the address counter. U42-10 drives the parallel load inputs of the low half of the address counter (U24-11, U25-11) low, causing these two devices to store the 8 bits at their data inputs. This is the low half of the starting address. Execution of OUT F6 with the high half of the starting address in the accumulator, will store the high half of the starting address in U26 and U27.

2. When a DMA transfer is in progress, the address counter is incremented each time a byte is transferred. Its contents represent the memory address with which the DMA Controller is interchanging data.

3. During each hold sequence within a DMA transfer, the signal $\overline{\text{BUSTR}}$ causes the address drivers U43, U44, U45 and U46 to place the contents of the address counter on the address bus by forcing low their disable inputs (pins 1).

F. Transfer Length Counter (Output Ports F3 and F4)

1. U28, U29 and U30 form the transfer length counter. The length (in bytes) of a transfer being described is stored in this counter in two steps. This is done by the same method which stores the starting address in the address counter. OUT F3 and OUT F4 cause this transfer by producing a negative pulse at U42-12, and U42-11 respectively.

2. When a DMA transfer is in progress, the transfer length counter is decremented each time a byte is transferred. Its contents represent the number of bytes yet to be transferred.

3. U30-13 (zero count) is used by the DMA controller to determine whether more bytes are needed to complete the specified length of the transfer.
4. Note that the high order "half" of the transfer length consists of only 4 bits.

G. Transfer Command Register and Logic (Output Port F1)

The ports described thus far are all output ports, and describe the features of a DMA transfer which may occur in the future. The remaining output port, F1, is the transfer command port. It causes transfers to happen.

1. Input Selection and Outputs U22-10 and 12

   a. U42-14 produces the transfer command strobe. U22 is the transfer command register. It is a 74LS298. It contains four 2-input multiplexers, each with an output latch. Latching occurs on the negative-going edge of the signal at pin 11. Input selection is controlled by pin 10.

   b. The register has been cleared to all outputs high. This signifies "do nothing." Pin 12 being high drives pin 10 high selecting the B-inputs. These are driven by the internal data bus. A transfer command port strobe on U42-14 drives U21-13 negative, causing U21-11 to drive U22-11 positive. When this strobe is REMOVED, the data present on the B-inputs will be latched to the outputs. Output pin 12 will copy DO bus bit 3 (DO 3) at one of its B-inputs. If anything is to happen, this bit will be LOW. (These 4 bits are all active low.) Pin 12 now drives pin 10 low which selects the A-inputs (pins 3, 4, 9 and 7). The 4 bits latched here represent a transfer pending. The transfer will actually happen at some later time when the disk has reached the correct rotary position.

   c. The binary U20-6 is clocked at pin 4 by MAIN CLOCK. It holds a slightly delayed copy of the signal of U22-12, which changes only on leading edges of MAINCLOCK.

d. The signal $\overline{\text{CROSSOVER}}$ is a pulse which describes the times (disk positions) at which it is proper to start or stop writing on disk. All DMA transfers start and end at a $\overline{\text{CROSSOVER}}$ pulse. $\overline{\text{CROSSOVER}}$ originates on the formatter PC assembly, and comes to the controller at P3-30.

e. U19-4 is an andgate with inverted inputs. If a transfer is pending, U20-6 is low, enabling U19-6. Each low pulse on $\overline{\text{CROSSOVER}}$ at U19-5 causes a high pulse at U19-4 if U19-6 is low.

f. The signal DATA is low if the read/write head of the disk is in a header region and is high if the head is in a data block region. It originates on the formatter assembly, and comes to the controller at P3-16. It drives U40-9.

2. Output U22-13

a. U22-13 is the bit of the pending transfer command which determines whether the controller is to transfer a header or a data block. It is high for a header, low for a data block. It drives U40-10. U40-8 is an exclusive orgate. U40-8 will be high if both inputs indicate header, or if both indicate data; U40-8 will be low in the remaining 2 cases.

b. U18-6 is an andgate with inverted output. U18-6 will pulse low if U19-4 pulses high when U40-8 is high. U18-6 describes a crossover time at which a transfer is requested and the head is in the region described (header or data).

c. DMAOFF is a binary whose output is normally high. Its output is low for the time that a DMA transfer is occurring. DMAOFF is clocked by the trailing (rising) edge of $\overline{\text{CROSSOVER}}$. The J and $\overline{\text{K}}$ inputs of DMAOFF (U20-14 and U20-13) are wired together and driven by U18-6. This is effectively a "type D" flipflop. The result is that DMAOFF is clocked high at every crossover except the selected one, at which time it is clocked low, and remains low until the next crossover.

d. The low pulse at U18-6 drives U21-12 low, causing a high pulse at U21-11. The trailing edge of this pulse causes the transfer command register to sample its A-inputs (all tied high) to its output latches. This amounts to a reset to all high. High at U22-12 means "do nothing." U22-12 drives U22-10 high returning selection to the inputs driven by the internal bus.

e. The negative pulse at U18-6 also enables U19-9. U-19-10 is an andgate with inverted inputs (U19-8, U19-9).

3. Output U22-14

a. U19-8 is driven by U22-14, which is low if the pending transfer is to be a write to disk and is high if a read from disk is indicated. If low, the low pulse at U18-6 causes a high pulse at U19-10 ($\overline{W}$) which drives U39-2 and U39-3. These 2 pins are the D input of a type D flipflop WRITE (U39-6). WRITE is clocked by the trailing (rising) edge of $\overline{CROSSOVER}$. WRITE normally is clocked to a low at every crossover time, but is clocked to a high instead, if U19-10 is high as described above. Once high, it will remain high until the next crossover.

b. DMAOFF and WRITE and their complements $\overline{DMAOFF}$ and $\overline{WRITE}$ are used throughout the controller and formatter.

c. The low pulse of U18-6 is used to clear the FIFO (first in first out) memories (U52 and U53).

4. Output U22-15

U22-15 is the fourth and final bit of the transfer command register. It must be high (inactive) during normal transfer commands as described above. It is used alone to cause an entire track to be cleared and written to a primitive format. Its operation is described more fully at 7.10.2, K, The Erase Function.

All of the output ports have now been discussed.

H. Status Reporting (Input Port FØ)

Port FØ is an input port. Execution of the command IN FØ will cause a low pulse at U42-15 (I/O Port Decoder). This drives low the disable inputs* (the two #1 pins) of the status drivers (U50, U51), enabling them to drive the DI bus with the 8 bits of the controller status. The processor puts this status into the accumulator. These 8 bits contain the only reports from the disk and controller to the processor.

For the meanings of these bits refer to Table 7-3, Port FØ Status Bit Assignments.

Four of these 8 bits are latched by U33 of the Data Transfer Status Logic. Any output to port F5 clears this latch to all low.

I. Headload Timing

1. The status strobe U42-15 drives U15-1 of the Drive Status Logic. This circuit is a one shot of approximately 1 second duration. Its inverted output U15-4 drives U32-15 low. This enables U32-11 and U32-13 to

*These drivers have inverted inputs.

load the heads if the disk drive is indicated by the appropriate bits in the disk command register U31.

2. A negative edge at U15-1 fires the oneshot, or renews its timeout to one second if already fired. The effect of this is to unload the heads if there is no activity at port FØ for 1 second or longer. This reduces head and disk wear without burdening the software with long timeouts.

   In early revisions of the controller this function was performed by port F5.

3. C1, Q1, R7 and R8 are discrete components required to establish the 1 second timeout. The B and R inputs of this oneshot are not used, and are wired high.

J. Unit Head Selection

U34 contains four 2-input multiplexers, two of which are unused. The signal -SELECTED DISK (U32-3) drives the select input (U34-1).

-LOAD HEAD Ø (U32-13) drives U34-10. -LOAD HEAD 1 (U32-11) drives U34-11. The appropriate one of these two signals is selected by the Drive Status multiplexer and delivered on U34-9. This line will be low when the selected head is loaded. It drives U15-9, the $\overline{A}$ input of the second oneshot in package U15. This oneshot fires on the leading edge of the selected head loaded signal, and remains on for approximately 40 ms. The B and R inputs are unused and are wired high. During this 40 ms, U15-12 is low and drives U10-11 low.

K. Read/Write Timing

U10-11 is the $\overline{S}$ input of the SREADY FF of the Drive Status Timers. When it is low the FF is forced on, and its $\overline{Q}$ output (U10-9) is low. The J and K inputs (U10-14, U10-13) are wired low, and the $\overline{R}$ input is wired high so that the FF can be restored to its normal off state only by being clocked by a rising edge at U10-12. This pin is driven by the signal $\overline{\text{RSECT}}$, the selected sector reset signal from the formatter. $\overline{\text{RSECT}}$ marks the beginning of a new block passing the read/write head.

The $\overline{Q}$ output of this FF, when low, holds the status bit SREADY low, indicating that the controller is not ready. This will occur for 40 ms following the start of selected head loaded, and will remain until the first $\overline{\text{RSECT}}$ occurring after the 40 ms. This circuitry relieves the software of the responsibility for the 40 ms head load timeout. The software merely awaits SREADY.

L. Producing The Status Bits

1. SREADY

SREADY is produced by gates U12-11 and U12-8 of the Data Transfer Status Register. Input U12-12 is driven by U10-9 as just discussed. Input U12-13 is driven low by U22-12, if a transfer has been requested but not started. If either of these is low, U12-11 will be low, driving U12-10 low. Input U12-9 is driven low by DMAOFF (U20-10 of the Transfer Command Logic), if a transfer is in progress. If either U12-10 or U12-9 is low, then SREADY (U12-8) will be low.

2. SELECTED DRIVE READY

The signal -READY 1 arrives from the disk drive on P2-6. It indicates that the right-hand (odd-numbered) unit in the selected disk drive is ready (low = ready). It drives U34-14.

The signal -READY Ø arrives from the disk drive on P2-22. It indicates that the left-hand (even-numbered) unit in the selected disk drive is ready. It drives U34-13 of the Drive Status Multiplexer.

-SELECT DISK 1 causes U34 to select the appropriate one of these two signals. The selected signal appears at U34-12, which drives U50-6 of the Status Read Driver. This line is the status bit SELECTED DRIVE READY.

3. SEEK COMPLETE

The signal -SEEK COMPLETE arrives from the disk drive on P2-10. It is delivered directly to the Status Read Driver U50-2. This line is the status bit SEEK COMPLETE. If low, it indicates that any requested track-seek operation (seek or restore) has been done.

4. SEPARATED INDEX

The signal -SEPARATED INDEX arrives from the disk drive on P2-8. It is delivered directly to U50-4. This line is the status bit SEPARATED INDEX. If low, it indicates that the selected disk is in the "index" reference position. This signal is called "separated" index because it originates mixed with sector, and has been separated into index and sector signals. Each dual drive has two index and sector optical pickups, but only 1 separator circuit. Therefore, separated index and separated sector may be invalid for 1 revolution after a change of selected unit. If you are attempting to design a software handler for this controller, beware.

M. Pass-Through Signals on The Controller Board
(Refer to Fig. 8-16, Pin-to-Pin Signal Flow Diagram.)

The signals -SEPARATED INDEX (P2-8), -SEPARATED DATA (P2-48), -SEPARATED CLOCK (P2-50), and -SEPARATED SECTOR (P2-20) arrive from the disk drive on the P2 pins cited, and drive pins of the same numbers in P3 of the controller which sends them to the formatter.

The signal -WRITE DATA arrives from the formatter on P3-38 and drives P2-38 which sends it to the disk drive.

N. Poweron Clear (Write Timing Control)

The signal $\overline{\text{POC}}$ appears at S-100 bus pin 99. Its use varies somewhat depending on the host computer, but it normally represents a reset or a statement that power has just been turned on. The controller uses it to assure that no write or DMA operation is occurring and that none will be started until the software enables it. A low pulse on $\overline{\text{POC}}$ drives U39-15 low, resetting the $\overline{\text{PWR ON}}$ FF. U39-10 goes low and remains low until a transfer command strobe (port F1) occurs. This low pulse originates at U42-15 and drives U39-11 low setting $\overline{\text{PWR ON}}$. $\overline{\text{PWR ON}}$ low drives U39-1 low resetting the WRITE FF in the Transfer Command Logic (U39-6 goes low). It also drives U20-11 low, setting the DMAOFF FF (U20-10 goes high). $\overline{\text{PWR ON}}$ also drives several latches in the DMA circuitry (Hold Sequence Logic) which have not yet been described.

The principal risk to recorded data other than mechanical damage to the recording surface is the risk that the controller may write at the wrong place or time. The controller will not write unless the write FF is on.

> CAUTION
>
> The circuitry just described assures that WRITE remains off starting with the $\overline{\text{POC}}$ signal, but does not provide protection during the time that power goes off. Therefore, it is advisable to remove disks before turning power off.

7.10.2 DMA TRANSFERS (Refer to Fig. 7-5A, DMA Transfer, the Process as Seen by the PTDOS.)

A. General Description of The DMA Transfer

The previous paragraphs describe the circuitry which communicates control from and status to the central processor. The following describes the moving of data to and from memory.

Data transfers are done by direct memory access (DMA). This means that the data goes directly to and from memory under the direction of the controller without being handled or controlled by the central processor. The DMA controller takes

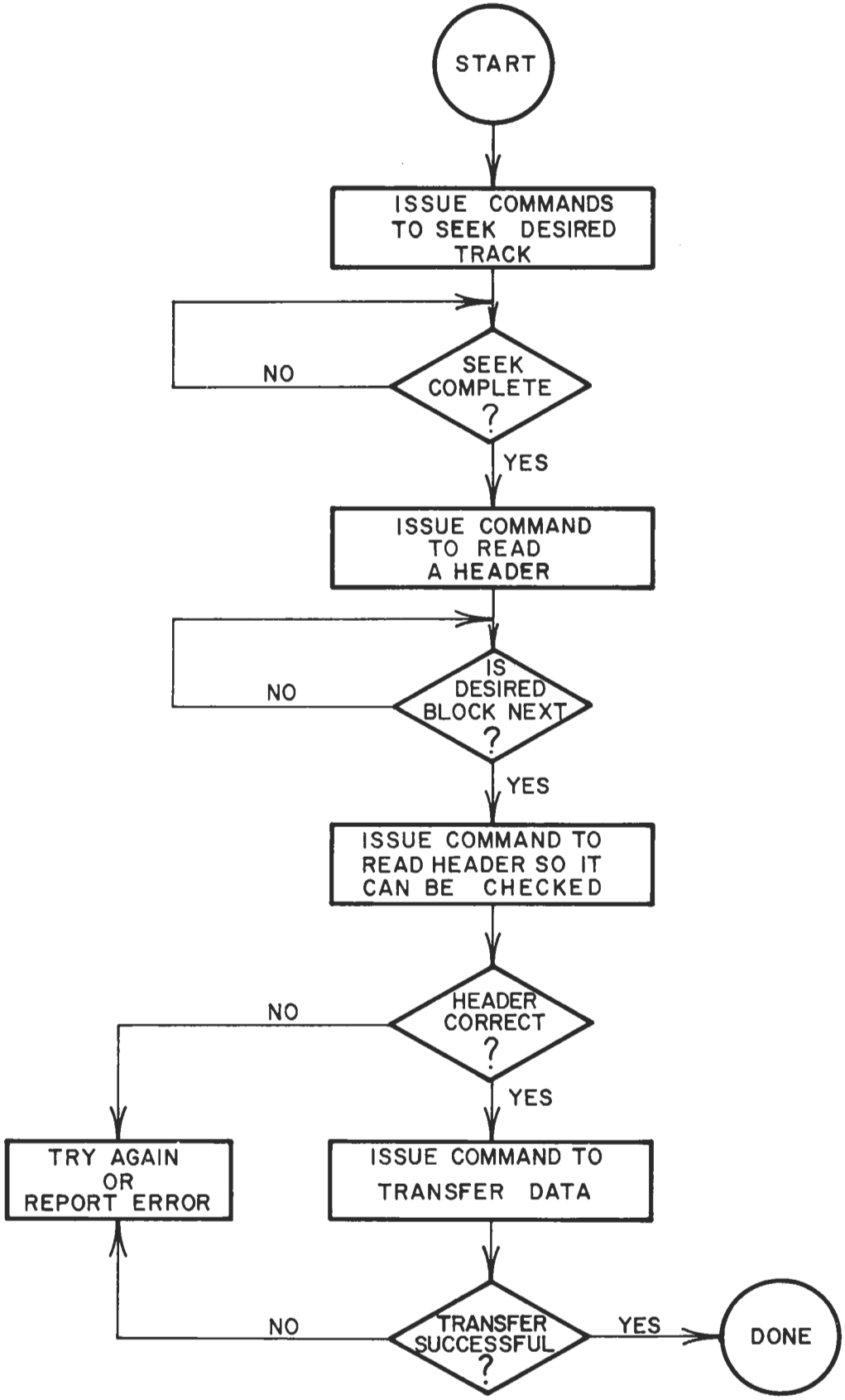


Fig. 7-5A DMA Transfer, The Process As Seen by The PTDOS

possession of the bus, putting itself in the place of the central processor. The DMA controller logic is on the controller board with some outlying functions being done on the formatter.

Within the scope of Helios II, a DMA TRANSFER means the sequence of events which occurs to move data bytes specified by the software via OUT instructions. This data will always be a data block, or the header describing a data block. A DMA transfer consists of one or more hold sequences interspersed with periods of normal CPU activity.
A HOLD SEQUENCE is the sequence of events which occurs when the DMA controller takes possession of the bus and moves a group of bytes to or from memory.

B. Timing of DMA Transfers And Transfer Request

A typical hold sequence lasts for 20 µs and moves 12 bytes. After the hold sequence, the controller is inactive for a period typically about 370 µs. During this period the CPU resumes its normal activity.

A DMA transfer lasts for as much as 130 ms, depending on block length.

A DMA transfer is represented by the time that the signal DMAOFF is low. A hold transfer is represented by the time that the HOLD FF (U2-6) is high.

DMA transfers are begun and ended under software control and timed by disk position as previously described in 7.10.1, paragraphs I and following.

Individual requests for hold sequences are initiated by the signal $\overline{\text{SET HOLD RQST}}$. This is generated on the formatter and arrives via P3-46. A low pulse here drives low U37-1 of the Hold Sequence Logic. This rests the FF $\overline{\text{HOLD RQST}}$, causing its $\overline{Q}$ output (U37-7) to go high, and remain high. This signal is applied to U35-4, and to U1-13, the D-input of a type D binary called HRR.

Φ2 (U6-8) drives the clock input of HRR (U1-9) sampling the hold request signal to HRR's output (U1-15). This signal represents a hold request, resynchronized to the Φ2 clock. Its complement appears on U1-14.

C. Bus Access Status Indicators (Hold Sequence Logic)

1. PHLDA is a S-100 bus signal appearing on S-100 pin 26. PHLDA high means that the processor has abandoned the bus signals to some other device (a DMA controller or alternate processor). PHLDA drives the D-input (U1-4) of the type D binary PHLDAR whose clock input (U1-9) is driven by Φ2 (U6-8). PHLDAR is a slightly delayed version of PHLDA. (Refer to Table 7-7, S-100 Pins.)
2. PHLDAR low (U1-3 high) means that no DMA device has control of the bus. U1-3 high enables gates U8-6 and U8-8 of the I/O Port Decoder, making possible the port strobes described earlier. U1-3 if high, enables and-gate UØ-3, by driving input UØ-1 high.

3. $\overline{\text{PHOLD}}$ is an S-100 bus signal by which DMA devices request control of the bus. It appears at S-100 pin 74. This signal drives UØ-2. If high it means that no DMA device is asking for the bus.

4. UØ-3 drives UØ-5 and UØ-10. The second inputs of these 2-input andgates are driven by $\overline{\text{HRR}}$ and HRR. Andgate UØ-6 if high means: No DMA device has the bus, no DMA device has asked for the bus, and the controller does not want the bus.

5. Controller's Priority of Bus Access

   Andgate UØ-6 drives a single wire connector (J4) at the top edge of the board. It is labeled PRIORITY OUT and is intended to be the beginning of a priority chain establishing an order of priority among DMA devices. Note that this board has no PRIORITY IN connector. As the executive device of the operating system it demands first priority. This will not usually be a problem to other DMA devices since this device takes control for 5% of the time or less and does so only for about 20 μs at a time. This controller will not demand that another DMA device give up control once that device has established control. If another device keeps control for long periods of time it may cause individual DMA transfers by this controller to abort. The operating system will normally be able to recover from such errors, but caution is advisable.

6. UØ-8 of the Hold Sequence Logic, if high, means that no DMA device has control of the bus, no DMA device has asked for control of the bus, and "this" controller wants control of the bus.

D. Controller Requests Bus

UØ-8 drives the J input (U2-2) of the HOLD FF of the Hold Sequence Logic. HRR (U1-15) drives the $\overline{\text{K}}$ input (U2-3) of the HOLD binary. Φ2 drives the clock input (U2-4) of the HOLD binary. Therefore, HOLD will come on at the first trailing edge of Φ2 after HRR rises, provided that no other device has control of the bus or has requested control by pulling down $\overline{\text{PHOLD}}$. Other DMA devices should lower $\overline{\text{PHOLD}}$ only at the trailing edge of Φ2.

The S and R inputs of the Hold binary are unused and are wired high. $\overline{\text{HOLD}}$ (U2-7) drives the disable input (U41-15) and the signal input (U41-14) of the $\overline{\text{PHOLD}}$ driver, whose output (U41-13) drives $\overline{\text{PHOLD}}$. When HOLD is high this board will drive $\overline{\text{PHOLD}}$ low. When HOLD is low, this board will release $\overline{\text{PHOLD}}$ to the third state (open circuit).

$\overline{\text{HOLD}}$ also drives U3-2, the input of a non-inverting driver whose output (U3-3) drives P3-18 providing the signal $\overline{\text{HOLD}}$ to the formatter.

HOLD (U2-6) drives U36-10. This resets a latch when low, and allows it to operate when high.

E. Generation And Function of BUSTR

HOLD drives UØ-12, the input of an andgate. The output of this gate (UØ-11) will be high when both HOLD and PHLDAR are high. This signal drives the D-input (U1-5) of the FF BUSTR. The clock input of BUSTR (U1-9) is driven by Φ2. The output (U1-7) of BUSTR is (HOLD and PHLDAR) delayed until Φ2 rises.

BUSTR is the signal which executes the bus transfer. It drives so many inputs that fanout drivers are used. U40-3 and U40-11 are inverting fanout drivers made from exclusive-OR gates. These devices generate two equivalent signals which drive many three-state driver disable inputs. Their effect is to cause the S-100 drivers of the CPU to release the bus lines, and the drivers on the controller to seize them.

BUSTR drives the reset input (U37-15) of the FF DNSYNC. When BUSTR is low, DNSYNC is held reset. When BUSTR is high, DNSYNC is released to function normally.

BUSTR also drives U35-3. This is an input of a three-input andgate with inverted output.

F. PSYNC Originated to Begin Hold Transfer

At the rise of BUSTR, $\overline{\text{DNSYNC}}$ is high and drives U35-5 high. U35-4 is held high by U37-7. All 3 inputs now being high, U35-6 goes low. This signal is $\overline{\text{DMASYNC}}$. It drives the inputs (U18-12, U18-13) of a gate wired as an inverter. Its output (U18-11) is DMASYNC. It is applied to U43-14, the input of a three-state driver, whose output (U43-13) drives the S-100 bus signal PSYNC (S-100 pin 76). U18-11 also drives the J-input of DNSYNC (U37-14).

The clock input of DNSYNC (U37-12) is driven by Φ2. When DMASYNC is high, DNSYNC will be low, and its $\overline{\text{K}}$-input will be high. The first Φ2 leading edge will clock DNSYNC (U37-10) high, and $\overline{\text{DNSYNC}}$ (U37-9) low. This will lower U35-5 and force DMASYNC low.

G. The Hold Transfer Cycle (Refer to Fig. 7-5B, Single Byte DMA Hold Transfer Cycle, Flow Chart.)

1. The SYNC Phase

Thus PSYNC has been applied to the bus and removed announcing the start of a normal cycle which is intended to transfer one byte.* DNSYNC will remain high holding PSYNC low until the cycle is complete.

*PSYNC is active high.

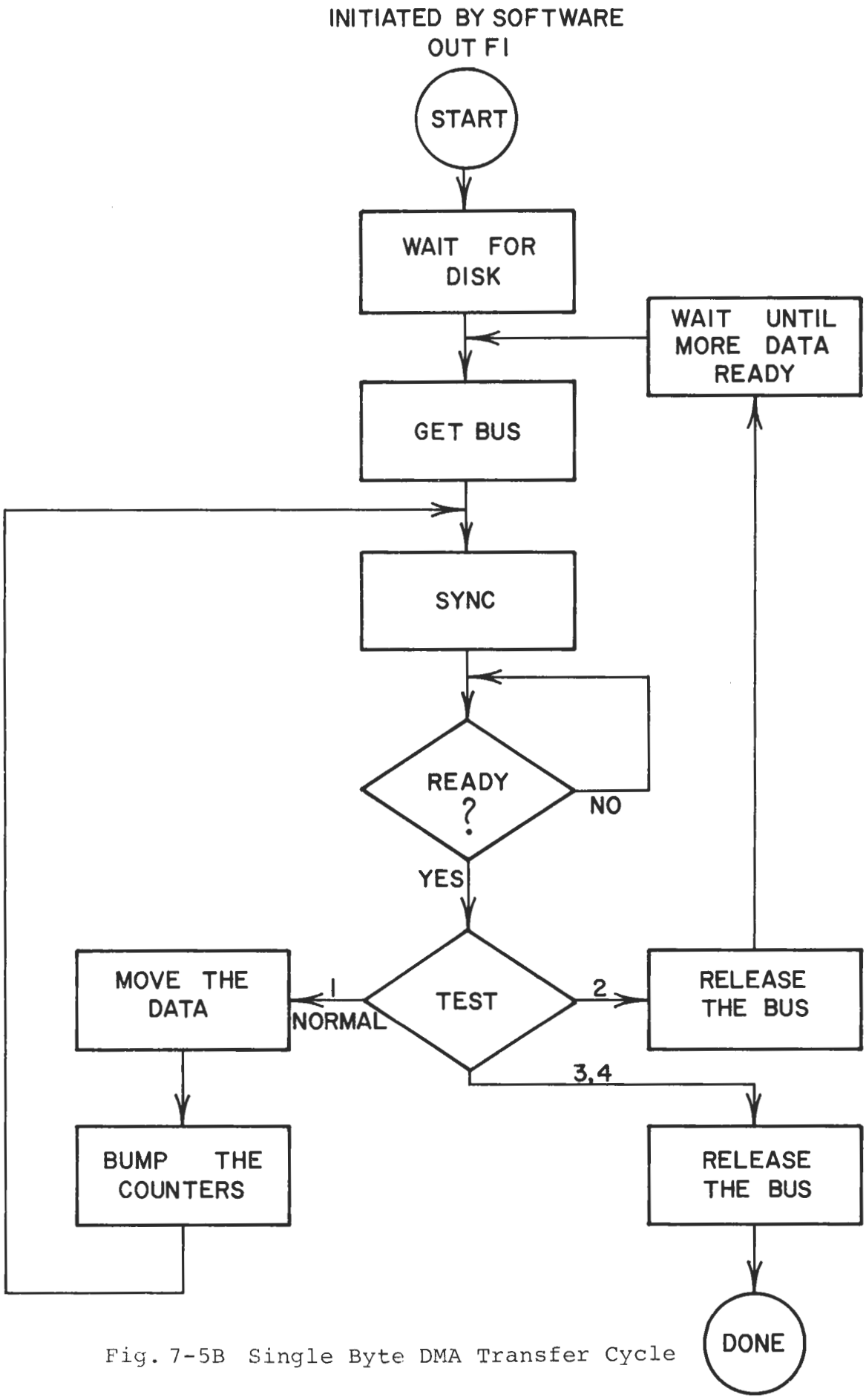


Fig. 7-5B Single Byte DMA Transfer Cycle

2. The Ready Phase

U23-8 of the Hold Sequence Logic is a four-input and-gate with inverted output. It has hysteresis inputs for noise immunity. Input U23-12 is driven by S-100 pin 3, XRDY. Input U23-13 is driven by S-100 pin 72, PRDY. Input U23-9 is driven by DNSYNC. If U23-10 is high, a high on DNSYNC samples the ready lines, producing a low at U23-8 if both ready lines are ready (high).

3. The Test Phase

a. U23-8 drives U38-12, the D-input of the type D binary $\overline{\text{TEST}}$, whose clock-input (U38-9) is driven by $\overline{\Phi 2}$. $\overline{\text{TEST}}$ (U38-10) is normally high, becoming low on the first Φ2 trailing edge after DNSYNC has risen and the ready lines are high.

b. $\overline{\text{TEST}}$ drives U36-1. If low, U36-3 will be low, driving U23-10 low which raises U23-8. $\overline{\text{TEST}}$ will be clocked high at the next Φ2 trailing edge. $\overline{\text{TEST}}$ can remain low for only one Φ2 period at a time.

c. $\overline{\text{TEST}}$ drives the $\overline{\text{enable}}$ input U16-1 of a decoder which tests the states of two signals. The first of these signals, appearing at U16-2, indicates the readiness of the FIFO buffer memory to provide data or space for the byte to be transferred. A low indicates ready.

d. The second signal indicates whether the requested number of bytes has already been transferred. A low indicates completion. The negative pulse at U16-1 will result in a similar negative pulse at one of the 4 outputs of this decoder, the selection being determined by the states of the two inputs. Whichever one of these outputs is active will result in a permutation of the basic cycle. (Refer to Fig.7-5B, the decision block "test.") We will now examine these 4 cases individually.

H. Types of Hold Transfer Cycles

(Refer to Fig. 7-6, Hold Transfer Cycle, Timing Diagram.)

1. The Normal Cycle (Refer to Fig. 7-5B, branching condition 1 at the TEST decision block.)

Only this first version of the cycle results in the transfer of a byte.

a. The normal case is described by FIFO ready (U16-2 low) and count not complete (U16-3 high). This will produce a low pulse at U16-6. This will result in the transfer of 1 byte, and the repeating of the cycle.

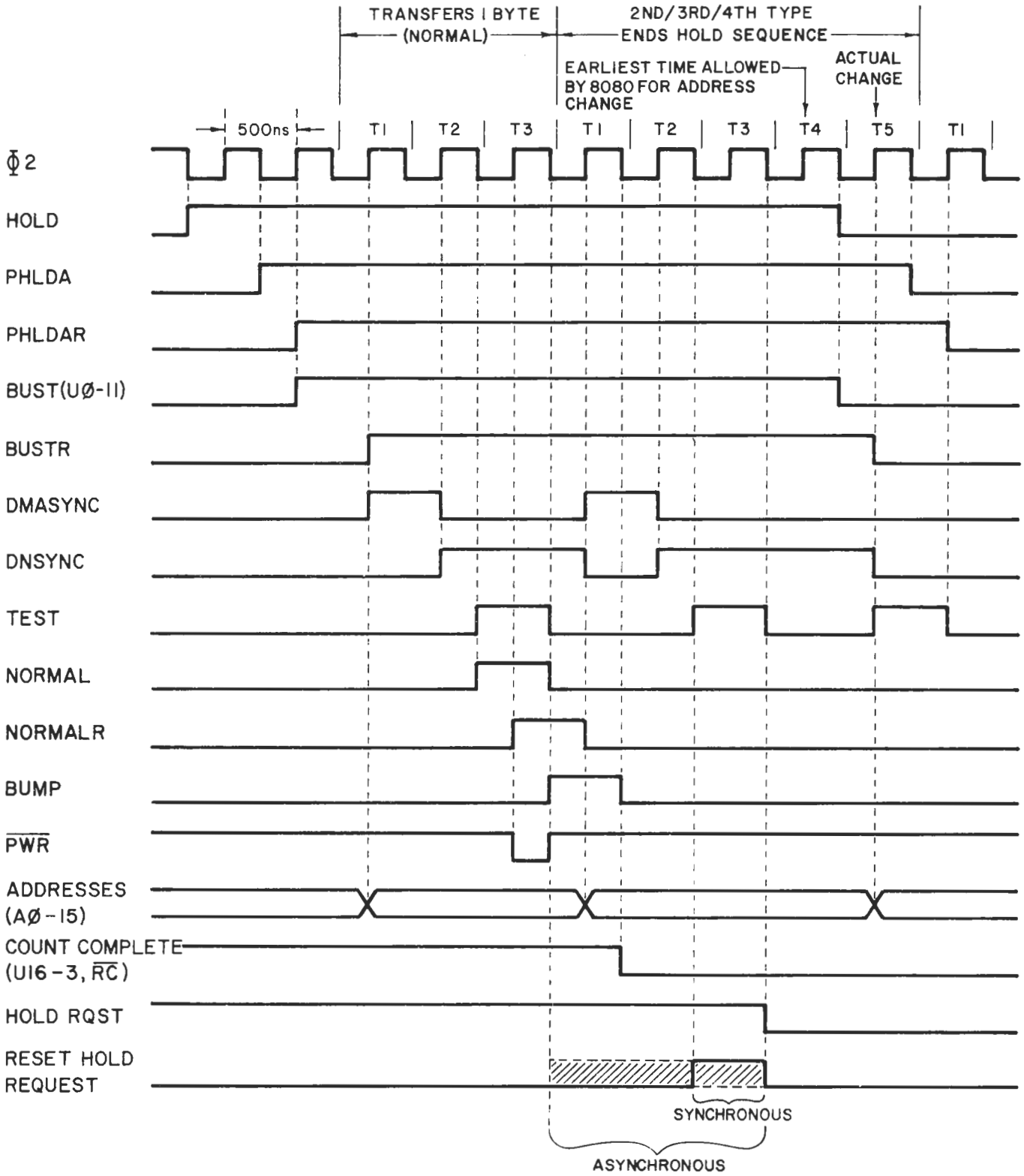


Fig. 7-6 Hold Transfer Cycle, Timing Diagram

b. U16-6 drives the D-inputs of 2 type-D binaries, $\overline{\text{NORMALR}}$ and $\overline{\text{BUMP}}$. The clock input of $\overline{\text{NORMALR}}$ is driven by Φ2. The clock input of $\overline{\text{BUMP}}$ is driven by Φ2.

c. U16-6 is a negative pulse of duration equal to one Φ2 period. It begins and ends on Φ2 trailing edges. $\overline{\text{NORMALR}}$ is identical but delayed, changing on Φ2 leading edges. $\overline{\text{BUMP}}$ is identical but delayed more. It changes on Φ2 trailing edges, being delayed by 1 full cycle.

d. NORMALR (U1-11) and $\overline{\text{BUMP}}$ (U38-15) are applied to the inputs of a gate (U18-9, U18-10). Its output (U18-11) will be low when both inputs are high. This is the first part of $\overline{\text{NORMALR}}$ before $\overline{\text{BUMP}}$ has started. It corresponds to a single high pulse of Φ2. This low pulse is the data strobe. When delivering data to memory, it provides $\overline{\text{PWR}}$. When getting data from memory, it provides the parallel load pulse which moves a byte into the top of the FIFO buffer memory.

e. U18-8 drives U13-13. This is an input to a two-input multiplexer. The alternate input (13-14) is wired inactive (high). Selection is determined by $\overline{\text{WRITE}}$ applied to U13-1. U13-15 is wired enabled (low). Output U13-12 is applied to U44-12, the input of a three-state driver whose output (U44-11) drives $\overline{\text{PWR}}$ (S-100 pin 77). $\overline{\text{PWR}}$ will be driven low during the data strobe when writing to memory (reading from disk).

f. U18-8 drives U11-5. This is an input to a two-input multiplexer. The alternate input (U11-6) is wired inactive (high). Selection is determined by $\overline{\text{WRITE}}$ applied to U11-1. U11-15 is wired enabled (low). The output of this multiplexer is an inverter. The output (U11-7) drives the PL-inputs of both FIFO buffer memories (U52-2, U53-2). PL will normally be low, and will be pulsed high by the data strobe.

g. $\overline{\text{NORMALR}}$ (U1-10) drives the clock-inputs of the address counter. These are U24-14, U25-14, U26-14 and U27-14. Counting occurs on the trailing edge. The address counter counts upward since Pin 5 of each stage is wired low.

h. BUMP (U38-14) drives the clock-input (U28-14) of the transfer length counter. Counting occurs on the leading edge. The counter counts downward since pin 5 of each stage is wired high. The terminal carry of this counter (U30-13) drives U16-3 providing the signal which indicates completion of the requested number of bytes. This signal will be low (completed) only if all bits of the counter are zero, and BUMP is low.

i. $\overline{\text{BUMP}}$ (U38-15), if low holds U36-2 low which holds U36-3 low which drives U23-10 low, preventing a new TEST pulse. $\overline{\text{BUMP}}$ drives the $\overline{\text{K}}$ input (U37-13) of DNSYNC. The Φ2 leading edge during BUMP clocks DNSYNC off, raising U37-9, and enabling the start of a new DMASYNC.

j. During read (from disk), $\overline{\text{BUMP}}$ which drives U13-6, is selected by the multiplexer U13-7 to drive the FIFO TOP (transfer out parallel) inputs (U52-13, U53-13). The trailing (rising) edge of this low pulse causes a new byte to be dropped from the bottom of the stack to the output-register within each FIFO.

This concludes the description of a normal cycle during which one byte is transferred to or from memory.

2. Second Type of Hold Transfer Cycle

a. Now we will discuss the second type of cycle. The signal $\overline{\text{TEST}}$, a negative pulse, enables U16-1. At this time the transfer length count is incomplete (U16-3 high), and the FIFO is unready to supply space or data for a transfer (U16-2 high). The present hold-sequence must be ended to allow time for the disk to move more data to or from the FIFO.

b. A negative pulse appears at U16-7, driving U16-13 low. U16-9 goes high, driving U36-9 high. Since HOLD is high, U36-10 is high; therefore U36-8 is high. This drives U16-15 high. U16-9 and U36-8 are connected as a latch. Once both are high, they will remain high until reset by lowering U36-10. This will eventually occur when HOLD goes low.

c. U36-8 drives the J-input (U37-2) of the $\overline{\text{HOLD RQST}}$ latch. $\overline{\text{HOLD RQST}}$ will be clocked to a 1 (U37-7 low) by the trailing (rising) edge of $\overline{\text{TEST}}$. The next Φ2 rise will clock HRR (U2-15) low, which drives the $\overline{\text{K}}$ input (U2-3) of the HOLD binary low. The next Φ2 trailing edge clocks HOLD low, resetting the latch (U36-8, U16-9).

d. $\overline{\text{HOLD}}$ (U2-7) rises, causing $\overline{\text{HOLD}}$ (P3-18) to rise, and $\overline{\text{PHOLD}}$ (S-100 bus pin 74) to be released to the third state.

e. HOLD (U2-6) drives UØ-12. When low, U2-11 goes low, driving the D-input of BUSTR low. At the next Φ2 leading edge, BUSTR goes low, disabling the bus drivers on this board, and enabling those of the S-100 CPU. Note that the S-100 status lines are now invalid until new status is latched during the next processor sync.

f. The processor will note the removal of $\overline{\text{PHOLD}}$ and will lower PHLDA at the start of a new T1 cycle. SYNC will rise on Φ2 leading edge. The processor is now back to its usual routine. PHLDA drives the D-input of PHLDAR. PHLDAR goes low on the first Φ2 leading edge. This is the same edge which causes the new SYNC from the processor. $\overline{\text{PHLDAR}}$ (U1-3) goes high, enabling input and output to the controller, and enabling UØ-1. This raises UØ-3, since UØ-2, $\overline{\text{PHOLD}}$,is high. UØ-3 drives UØ-5. $\overline{\text{HRR}}$ (UØ-4) is high, so UØ-5 high causes UØ-6 to go high. This is priority out. It is permission for other devices to use $\overline{\text{PHOLD}}$. (See 7.10.2,C,5, "Controller's Priority of Bus Access.")

This completes the discussion of the second type cycle which ends a hold sequence. No data byte was transferred. Control of the bus was returned to the CPU.

3. 3rd and 4th Type of Hold Transfer Cycle

a. We will now discuss the remaining type of cycle. (The 3rd and 4th types are identical.) The signal $\overline{\text{TEST}}$, a negative pulse, enables U16-1. At this time the transfer length count is complete (U16-3 is low). Depending on the signal at U16-2, a negative pulse will appear at U16-4 or at U16-5. In either case, a negative pulse will appear at U17-6. This pulse will cause the end of the present hold sequence, and indicate that the DMA transfer is complete.

b. U17-6 drives U16-14. When these go low, U16-9 and U36-8 are latched high. This causes a sequence identical to that previously described, which ends the hold sequence and returns control of the bus to CPU.

c. U17-6 drives the $\overline{\text{S}}$ input (U33-3) of the latch TC. When low, TC (U33-4) will become high and remain high until reset by an F5 port strobe. TC is bit Ø of the status byte. TC is delivered to a status driver input (U51-4) and to an inverter input (U7-11).

d. $\overline{\text{TC}}$ (U11-10) drives gate input (U19-12). U19-11 is driven by $\overline{\text{ORE}}$, a signal which is low when the FIFO output register is empty (and some other times, too; see paragraph L, FIFO discussion for details). If both U19-11 and U19-12 are low, U19-13 will be high. It drives U3-10, a driver whose output (U3-9) drives P3-4, sending ORE AND TC to the formatter. The formatter uses this signal to break out of a loop, which escape eventually causes the end of the DMA transfer by producing CROSSOVER.

I. Abort Signals

There are 5 abort signals, all of which set the ABORT latch. The first 3, PWR ON, SYNC ERROR, and FIFO DEPLETED all terminate a DMA transfer as just described. The remaining two OVER INDEX and MISSED do not terminate the DMA transfer.

1. PWR ON (U39-10) has already been discussed. It drives U17-1. If low, U17-12 will be low. This drives U17-11, and U17-3. If U17-3 is low, U17-6 will be low. This will result in TC being set and the present hold sequence and DMA transfer being ended as previously described.

   If U17-11 is low, U17-8 will be low, driving the $\overline{S}$ input (U33-6) of ABORT low. ABORT (U33-7) then goes high and stays high until reset by an OUT F5 strobe.

2. SYNC ERROR arrives at P3-6 from the formatter board. It drives U17-2. If low, U17-12 goes low, producing the same results as PWR ON.

   SYNC ERROR low means that the state counter on the formatter is out of step with the data passing the head.

3. FIFO DEPLETED is produced at U35-8 and drives U17-13. If low, U17-12 goes low, producing the same results as PWR ON.

   FIFO DEPLETED means that bad data has been transferred because the FIFO buffer memory ran out of space or data needed by the disk. This can happen if the system fails to respond to the controller in a timely manner. Possible causes are hardware failure, slow memory, failure of another DMA device to release the bus at reasonable intervals, or a ready line held low.

   This abort is indicative of system inadequacy of some sort and is never seen in normal operation.

   FIFO DEPLETED is produced by gates U35-8, U18-8 and U35-12. They are equivalent to one 5-input andgate with inverted output. FIFO DEPLETED will be low if the following five signals are all high:

NAME	SOURCE	INPUT
$\overline{\text{DMAOFF}}$	U20-9	U35-10
"*"	U11-12	U35-9
$\overline{\text{TC}}$	U7-10	U35-1
MAIN CLOCK	U11-4	U35-2
TEXT	P3-14	U35-13

   The signal marked "*" is produced by the 2-input inverting multiplexer U11-12. Selection is controlled

by WRITE (U39-7) which drives the select input (U11-1). The enable input is wired low (enabled). U11-12 will be high if WRITE is low and OREB (U53-22) is low, or if WRITE is high and IRFB (U53-1) is low. These two cases correspond to writing on the disk, and reading from the disk respectively.

4. OVER INDEX (P3-10) originates on the formatter. It drives U17-9. If low, U17-8 goes low, setting the ABORT latch (U33-7) high.

   OVER INDEX low means that the formatter board has found the sector mark after index to be within a data block. This is a violation of the rule that the sector mark after index must be a data block boundary.

5. MISSED (U40-6) drives U17-10. If low, U17-8 goes low, setting the ABORT latch (U33-7) high.

   RSECT (P3-32) originates on the formatter. It is the sector reset which starts a new data block. RSECT drives U19-3. U22-13 is the output of the transfer command register which indicates whether a pending transfer command is to move header or data. Low indicates data. If both these signals are low, U19-1 and U40-5 will be high; U40-6 and U17-10 will be low.

   MISSED low means that a new block has started without doing a data transfer command which is still pending.

   Transfer data commands are given only after finding the correct header. Such a command must be given before the next crossover (about 350 µs, in order to be executed in the correct block. If this timing requirement is not met, a MISSED abort will occur at the beginning of the next block. The software must send a null transfer command (OUT F1, data = FF) to cancel the missed transfer; otherwise the wrong block will be transferred. Software handler designers beware. (PTDOS takes care of this automatically.)

J. CRC Reporting

The following is a description of the circuitry which reports the results of the CYCLICAL REDUNDANCY CHECK (CRC).

1. DMAOFF (U20-9) drives U21-9. If high it indicates that a DMA transfer is in progress and a report is appropriate. TEXT (P3-14) drives U21-10. If high it indicates that the formatter is in the text of a message (not preamble or postamble). If both these signals are high, U21-8 will be low. It drives U14-3, the high order select-input of a 2-to-4 line decoder.

2. CRCERR (P3-24) is the output of the CRC checker on the formatter. It carries continually changing data which at one unique time represents the results of the CRC

check. High at that time represents an error. CRCERR is applied to the low order select-input (U14-2) of the decoder.

3. $\overline{RMC}$ (P3-42) originates on the formatter. It is a latched copy of the "missing clock" signal. It represents the unique time at which CRCERR is valid. $\overline{RMC}$ drives the $\overline{enable}$ input of the decoder.

4. Only 2 of the 4 outputs are used. All outputs remain high unless $\overline{RMC}$ is pulsed low. If $\overline{RMC}$ goes low, one of the outputs will go low.

5. If U14-3 is high, one of the unused outputs goes low, and nothing happens. If U14-3 is low, one of the two used outputs will be pulsed low by $\overline{RMC}$. If U14-2 is low, U14-4 will be pulsed low by $\overline{RMC}$, driving U33-11 low and setting the status latch CRC CHECKED (U33-9) high. This indicates completion of the check with no error. If U14-2 is high, U15-5 will be pulsed low driving U33-12 and U33-15 low. This sets both the CRC CHECKED latch (U33-9) and the CRC ERROR latch (U33-13) high, indicating completion of the check and an error.

6. Note that the latches CRC CHECKED, CRC ERROR, ABORT, and TC remain high, once set high. Any OUT F5 instruction will produce a negative pulse at U42-10, driving the $\overline{R}$ inputs U33-1, U33-5, U33-14 and U33-10 low, thus resetting the four latches.

K. The Erase Function

ERASE on the controller is used to describe an operation which writes an entire track to an empty, primative format. It is an erase from the point of view of data, but is not really erasure in the usual magnetic recording sense.

ERASE will occur in response to an OUT F1 instruction executed with the low order bit of the accumulator containing a zero. It will continue until removed by executing an OUT F1 with the low order bit of the accumulator containing a one. To assure that a full track is formatted, the software should count two index marks while ERASE is on.

While erase is on, U22-15 will be low. This drives U39-5 and U33-3. The $\overline{S}$ input (U39-5) of the WRITE FF when low forces WRITE (U39-6) high. The $\overline{S}$ input of the TC latch when low, forces TC (U33-4) high. This causes the controller and formatter to write continuously until U22-15 returns high. Writing will continue after that, until the next crossover. This results in a clean departure, leaving a complete track written in format legible to the controller. The headers on such a track contain 13 bytes of FF_{16} (all ones), and the data blocks contain 1 byte (also FF_{16}). There are 16 blocks per track.

L. FIFO Buffer Functions

1. The controller board uses two 9403 ICs to provide a first in, first out (FIFO) buffer memory, and to do the serial-to-parallel, and parallel-to-serial conversion required by the serial-by-bit disk format, and the 8-bit parallel format of the S-100 bus.

2. The buffer memory allows the controller to communicate with the disk at the relatively slow data rate required by the disk, without requiring continual participation by the processor. At intervals, the controller suspends the operation of the processor for a short time, while communicating with memory at the maximum speed the system can accommodate.

3. The result is that data can be moved to and from disk with only a minimum requirement of processor time. Typically, the system is tied up by disk communications only 5% of the time while transfers are occurring.

4. For a discussion of the operation of the 9403 refer to the Fairchild publications, Low Power Schottky and Macrologic or Macrologic Bipolar Microprocessor Databook.

5. Because of a successful effort to minimize the number of pins, the pinout nomenclature of the FIFO is somewhat enigmatic. In particular do not put too much reliance on the words "serial" and "parallel" in the names of control pins. Nearly every pin has functional requirements in both serial and parallel operation.

6. This controller uses two 9403s arranged in parallel using the method suggested by Fairchild.

7. U52, FIFO A is the master, so distinguished by having pins 9 and 15 tied low. U53, FIFO B is the slave.

8. FIFO pin assignments, signals and interconnections are summarized in Table 7-6, FIFO Interconnections. Most of this is self-explanatory. Signals needing elaboration are marked "*" and discussed below.

Table 7-6 FIFO Interconnections

FIFO A

PIN	MNEMONIC	COMMENT
1	$\overline{IRF}$	Low indicates input register full (first half). Drives $\overline{IES}$ (U53-9) of FIFO B, enabling if low.
2	PL	Parallel Load; rise moves 1 byte to input register; lowers $\overline{IRF}$.
3	DØ	Parallel input driven directly by S-100 D17.
4	D1	Parallel input driven directly by S-100 D16.
5	D2	Parallel input driven directly by S-100 D15.
6	D3	Parallel input driven directly by S-100 D14.
7	DS	Serial input driven by RDATA (P3-44).
8	$\overline{CPSI}$	* Clock Pulse, Serial Input.
9	$\overline{IES}$	Input Enable, Serial. Wired low to establish FIFO A as the master.
10	$\overline{TTS}$	Transfer To Stack. Driven by $\overline{IRF}$ of FIFO B.
11	$\overline{MR}$	Master Reset. Driven by U18-6. Clears the control circuitry at the start of each DMA transfer.
12	GND	Ø V from power supply.
13	TOP	Transfer Out, Parallel. Moves a byte from bottom of stack to output register.
14	$\overline{TOS}$	Transfer Out, Serial. Driven by $\overline{ORE}$ of FIFO B.
15	$\overline{OES}$	Output Enable, Serial. Wired low, A is the master.
16	$\overline{CPSO}$	* Clock Pulse, Serial Output.
17	$\overline{EO}$	Enable Output. Driven by WRITE (U39-6).
18	Q3	Parallel data output. Drives DO4 driver.
19	Q2	Parallel data output. Drives DO5 driver.
20	Q1	Parallel data output. Drives DO6 driver.
21	QØ	Parallel data output. Drives DO7 driver.
22	QS	Serial data output. Sent to formatter via the driver U3-7 and P3-12.
23	$\overline{ORE}$	Output Register Empty (if low). Drives $\overline{OES}$ of FIFO B.
24	VCC	+5 V from power supply.

Table 7-6 FIFO Interconnections (Continued)

FIFO B

PIN	MNEMONIC	COMMENT
1	$\overline{\text{IRF}}$	* Input Register Full (if low). Drives $\overline{\text{TTS}}$ of both FIFOs.
2	PL	Parallel Load. Rise moves 1 byte to input register, lowers $\overline{\text{IRF}}$.
3	DØ	Parallel input driven directly by S-100 DI3.
4	D1	Parallel input driven directly by S-100 DI2.
5	D2	Parallel input driven directly by S-100 DI1.
6	D3	Parallel input driven directly by S-100 DIØ.
7	DS	Serial input driven by RDATA (P3-44).
8	$\overline{\text{CPSI}}$	* Clock Pulse, Serial Input.
9	$\overline{\text{IES}}$	Input Enable, Serial. Driven by $\overline{\text{IRF}}$ of FIFO A. Low indicates the slaves's turn to load bits.
10	$\overline{\text{TTS}}$	Transfer To Stack. Driven by $\overline{\text{IRF}}$ of FIFO B.
11	$\overline{\text{MR}}$	Master Reset. Driven by U18-6. Clears the control circuitry at the start of each DMA transfer.
12	GND	Ø V from power supply.
13	TOP	Transfer Out, Parallel. Moves a byte from bottom of stack to output register.
14	$\overline{\text{TOS}}$	Transfer Out, Serial. Driven by $\overline{\text{ORE}}$ of FIFO B.
15	$\overline{\text{OES}}$	Output Enable, Serial. Driven by $\overline{\text{ORE}}$ of FIFO A. Low indicates the slave's turn to deliver bits.
16	$\overline{\text{CPSO}}$	* Clock Pulse, Serial Output.
17	$\overline{\text{EO}}$	Enable Output. Driven by WRITE (U39-6).
18	Q3	Parallel data output. Drives DOØ driver.
19	Q2	Parallel data output. Drives DO1 driver.
20	Q1	Parallel data output. Drives DO2 driver.
21	QØ	Parallel data output. Drives DO3 driver.
22	QS	Serial data output. Sent to formatter via the driver U3-7 and P3-12.
23	$\overline{\text{ORE}}$	* Output Register Empty (if low). Drives $\overline{\text{TOS}}$ of both FIFOs.
24	VCC	+5 V from power supply.

M. FIFO Input And Output Signals

1. Origin of $\overline{\text{CPSI}}$ Input Signal

U12-2 of the DMA logic is driven by TEXT (P3-14). U12-1 is driven by MAIN CLOCK (U11-4). If both of these signals are high, U12-3 will be high, and will drive U13-3 high. U13-4 is a 2-input multiplexer. Its $\overline{\text{enable}}$ input (U13-15 is wired low (enabled). Its select input (U13-1) is driven by $\overline{\text{WRITE}}$ (U39-7). Its alternate input U13-2 is wired high. When writing (to disk) U13-4 will be high. At other times it will follow the signal at U13-3. U13-4 drives the $\overline{\text{CPSI}}$ inputs of both FIFOs.

2. Origin of the $\overline{\text{CPSO}}$ Input Signal

U12-4 is driven by WRITE (U39-6). U12-5 is driven by $\overline{\text{CLOCK 2}}$ (U14-11). If both are high, U12-6 will be high. U12-6 drives the $\overline{\text{CPSO}}$ inputs of both FIFOs.

3. FIFO-Full Reporting

The $\overline{\text{IRF}}$ output of FIFO B is the signal used to report to the controller whether the FIFOs are full. It drives multiplexers at U11-11 and U11-13.

The $\overline{\text{ORE}}$ output of FIFO B is the signal used to report to the controller whether the FIFOs are full. It drives multiplexers at U11-14 and U11-10. It also drives U19-11 to produce the signal ORE AND TC which is sent to the formatter.

The signals $\overline{\text{IRF}}$ and $\overline{\text{ORE}}$ are not as simple as their names would indicate. Each is driven to unnatural states by other control signals, therefore, they are valid full- or -empty reports only at certain times. See the Fairchild data for details if needed (paragraph 7.10.2, L, 4 above.)

U11-12 is a 2-input multiplexer which supplies the appropriate one of $\overline{\text{IRF}}$ or $\overline{\text{ORE}}$ to the FIFO DEPLETED ABORT circuit at U35-9.

U11-9 is a 2-input multiplexer which supplies the appropriate one of $\overline{\text{IRF}}$ or $\overline{\text{ORE}}$ to a binary U2-10. Both this and the previous multiplexer are wired enabled (low) at U11-15, and selection is governed by $\overline{\text{WRITE}}$ (U39-7) which drives the select input (U11-1).

The FF U2-10 is needed to latch the full or empty signal for use by the DMA circuitry in selecting the type of cycle to be performed. It is the FIFO ready indicator discussed. U11-9 drives the J and $\overline{\text{K}}$ inputs making it effectively a type-D FF. This data is clocked to the output at the rising (trailing) edge of the $\overline{\text{DMASYNC}}$ pulses. $\overline{\text{DMASYNC}}$ originates at U35-6

which drives the clock input (U2-12). The R and S inputs are wired high (unused).

4. FIFO Parallel Output to S-100 DO Bus

U48 and U47 each contains 4 tristate drivers as well as the receivers previously discussed. These 8 drivers are enabled by $\overline{\text{BUSTR}}$ (U40-3) at pins U47-9 and U48-9. They deliver the FIFO parallel output to the S-100 DO bus.

Table 7-7 Numerical Pin-to-Pin Assignments Between Controller and S-100 Backplane (with Descriptions)

PIN #	SIGNAL SYMBOL	SIGNAL NAME	FUNCTION
1	+8V	+8 VDC	Unregulated supply to controller from S-100.
2	Not used by the controller		
3	XRDY	EXTERNAL READY	External ready input to CPU and controller.
4-17	Not used by the controller		
18	$\overline{\text{STATUS DSBL}}$	STATUS DISABLE	Disables the CPU buffers for the 8 status lines.
19	$\overline{\text{CC DSBL}}$	COMMAND/CONTROL DISABLE	Disables the CPU buffers for the 6 command/control lines.
20-21	Not used by the controller		
22	$\overline{\text{ADDR DSBL}}$	ADDRESS DISABLE	Disables the CPU buffers for the 16 address lines.
23	$\overline{\text{DO DSBL}}$	DATA OUT DISABLE	Disables the CPU buffers for the 8 data output lines.
24	$\phi 2$	PHASE 2 CLOCK	S-100 clock.
25	Not used by the controller		
26	PHLDA	HOLD ACKNOWLEDGE	Processor command/control output signal that responds to HOLD, indicating that the data and address buses will go to the high impedance state and the processor will enter the HOLD state after the current machine cycle.
27	PWAIT	WAIT	Processor command/control signal which acknowledges that the processor is in a wait state. The controller holds this line at a low state during DMA transfers.
28	PINTE	INTERRUPT ENABLE	Processor command/control output signal; indicates interrupts are enabled, as determined by the contents of the CPU internal interrupt flip-flop. When the flip-flop is set (Enable Interrupt instruction), interrupts are accepted by the CPU; when it is reset (Disable Interrupt instruction), interrupts are ignored.
29	A5	ADDRESS LINE #5	
30	A4	ADDRESS LINE #4	
31	A3	ADDRESS LINE #3	

Table 7-7 Numerical Pin-to-Pin Assignments Between Controller and S-100 Backplane (with Descriptions), Continued

PIN #	SIGNAL SYMBOL	SIGNAL NAME	FUNCTION
32	A15	ADDRESS LINE #15 (MSB)	
33	A12	ADDRESS LINE #12	
34	A9	ADDRESS LINE #9	
35	DO1	DATA OUT LINE #1	
36	DOØ	DATA OUT LINE #Ø	
37	A10	ADDRESS LINE #10	
38	DO4	DATA OUT LINE #4	
39	DO5	DATA OUT LINE #5	
40	DO6	DATA OUT LINE #6	
41	DI2	DATA IN LINE #2	
42	DI3	DATA IN LINE #3	
43	D17	DATA IN LINE #7	
44	SM1	MACHINE CYCLE 1	Status output signal that indicates that the processor is in the fetch cycle for the first byte of an instruction.
45	SOUT	STATUS OUTPUT	Status output signal that indicates the address bus contains the address of an output device and the data-out bus will contain the ouput data when $\overline{PWR}$ is active.
46	SINP	STATUS INPUT	Status output signal indicating that the address bus contains the address of an input device and the input data should be placed on the data bus when PDBIN is active.
47	SMEMR	MEMORY READ	Status output signal that indicates the data bus will be used to read memory data.
48	SHLTA	HALT ACKNOWLEDGE	Status output signal that acknowledges a HALT instruction.
49	Not used by the controller		
50	GND	GROUND	
51	+8V	+8 VDC	Unregulated supply to the controller.
52-71	Not used by the controller		

Table 7-7 Numerical Pin-to-Pin Assignments Between Controller and S-100 Backplane (with Descriptions), Continued

PIN #	SIGNAL SYMBOL	SIGNAL NAME	FUNCTION
72	PRDY	PROCESSOR READY	Memory and I/O input to the CPU Board wait circuitry and to the controller.
73	Not used by the controller		
74	$\overline{\text{PHOLD}}$	$\overline{\text{HOLD}}$	Processor command/control input signal that requests the processor enter the HOLD state; allows an external device to gain control of address and data buses as soon as the processor has completed its use of these buses for the current machine cycle.
75	Not used by the controller		
76	PSYNC	SYNC	Processor command/control output; provides a signal to indicate the beginning of each machine cycle.
77	$\overline{\text{PWR}}$	$\overline{\text{WRITE}}$	Processor command/control output; used for memory write or I/O control. Data on the data-out bus is stable while the $\overline{\text{PWR}}$ is active.
78	PDBIN	DATA BUS IN	Processor command/control output; indicates to external circuits that the data-in bus is in the input mode.
79	AØ	ADDRESS LINE #Ø (LSB)	
80	A1	ADDRESS LINE #1	
81	A2	ADDRESS LINE #2	
82	A6	ADDRESS LINE #6	
83	A7	ADDRESS LINE #7	
84	A8	ADDRESS LINE #8	
85	A13	ADDRESS LINE #13	
86	A14	ADDRESS LINE #14	
87	A11	ADDRESS LINE #11	
88	DO?	DATA OUT LINE #2	
89	DO3	DATA OUT LINE #3	
90	DO7	DATA OUT LINE #7	
91	DI4	DATA IN LINE #4	

Table 7-7 Numerical Pin-to-Pin Assignments Between Controller and S-100 Backplane (with Descriptions), Continued

PIN #	SIGNAL SYMBOL	SIGNAL NAME	FUNCTION
92	DI5	DATA IN LINE #5	
93	DI6	DATA IN LINE #6	
94	DI1	DATA IN LINE #1	
95	DIØ	DATA IN LINE #Ø	
96	SINTA	INTERRUPT ACKNOWLEDGE	Status output signal; active when the CPU processes an accepted interrupt. Controller ignores INTERRUPT REQUEST and keeps SINTA low when in control.
97	$\overline{\text{SWO}}$	$\overline{\text{STATUS WRITE OUT}}$	Status output signal; indicates that the operation in the current machine cycle will be a WRITE memory or output function.
98	SSTACK	STATUS STACK	Status output signal indicates that the address bus holds the pushdown stack address from the Stack Pointer.
99	$\overline{\text{POC}}$	$\overline{\text{POWER-ON CLEAR}}$	Resets DMA transfer logic.
100	GND	GROUND	

7.11 FUNCTIONAL CIRCUIT ANALYSIS OF THE FORMATTER

(Refer to Fig. 8-12, Formatter PCB Schematic and Fig. 8-17, System Block Diagram.)

7.11.1 DESCRIPTION OF FORMATTING

(Refer to Fig. 7-1, Format within A Block.)

The controller uses a combination of hard and soft sectoring techniques to provide a recording format with variable sector length and good utilization of disk capacity.

There are 77 tracks per diskette. Each recorded sector lies entirely within a single track. Recording on the disk is serial-by-bit; all recording is done in 8-bit bytes. There are 32 "hard sector marks" per revolution of the disk. These marks are in the form of small holes at the same radius as index hole. There is one "index mark" which falls halfway between two of the hard sector marks. The hard sector mark immediately after the index mark is sector mark zero.

Only 16 of the hard sector marks are used by the controller. These are the alternate ones starting with zero. The 16 are numbered Ø-15. The others are completely ignored.

The preamble of Header begins at the leading edge of a sector mark. It is recorded with all clocks present, and all data zero. It may contain crossovers which may cause missing clocks. A crossover is the point on the disk where writing started or stopped.

Within a single write-on-disk, clock and data marks are recorded coherently. Since disk speed is somewhat variable, there is an incoherency at each crossover. When reading, the clock separator will momentarily lose and regain sync at crossovers, sending some missing clock pulses as it does so.

The preamble of Header is space to allow the clock separator to lose and regain sync at crossover, and space to allow the controller to gain sync with the new sector.

Header is a block of 13 bytes which identify the sector, 2 bytes of redundancy data for checking, and one byte of synchronization of data.

The preamble of Data provides space to re-sync the clock separator and the controller and provides program time for the processor to examine the content of the Header just read, and make a decision whether to read, write or ignore the Data.

Note that the Header and Data of a sector are read by separate operations, and written by separate operations.

The data block is of variable length and contains the actual data. It also contains 2 bytes of redundancy check data and one byte of synchronization data.

The length of the data block (not counting CRC and Sync) is selected by the processor. Generally this can be any length from Ø to 4095 bytes; however, certain byte counts are forbidden. Checking for this is done by the DOS. If a forbidden byte count is requested, the DOS will add dummy data, and increase the request to the next allowed size. This is done so that data blocks will not end too close to sector marks.

The postamble is the empty space after the end of Data, and before the next sector mark. It provides tolerance for disk speed variations.

7.11.2 CONTROLLER FUNCTIONS IN FORMATTING

The controller accepts requests for transfers of data between memory and the disk. These are accepted and stored as "transfer commands." These commands consist of 3 bits.

Bit 1 TRANSFER COMMAND

- Low: Do a transfer starting at the next appropriate crossover.
- High: Do not do a transfer.

Bit 2 $\overline{\text{TR DATA}}$

- Low: The transfer is to be a Data transfer; use the crossover after Header.
- High: The transfer is to be a Header transfer; use the crossover before Header.

Bit 3 R/$\overline{\text{W}}$

- Low: The transfer is to be a Write.
- High: The transfer is to be a Read.

When the controller is writing on disk, writing begins at a crossover mark, and proceeds through a given sequence of steps, timed by a crystal clock in the CPU. The timing accuracy is excellent, but recording position on the disk varies with variations in the sector detector, and with disk speed. When the same data is read later, the start is again subject to sector detector variation and disk speed variation. When the controller reads, it searches for a known byte (the sync mark) in order to prevent errors due to sector detector variation.

From this point, sequencing is caused by the clock received from the disk, thus avoiding errors due to disk speed.

Write sequencing consists of stepping through a known sequence; read sequencing consists of searches for sync followed by recognition of success and stepping through a known sequence, or recognition of failure to sync.

7.11.3 DETAILS OF SEQUENCING

A. Sector Reset Logic

The sector Reset logic does the following:

1. Separates the 16 "sector marks" from the 32 "hard sector marks."

2. Generates a signal $\overline{\text{RSECT}}$ (Sector Reset) which is synchronous with $\overline{\text{MAIN CLOCK}}$, and occurs just after the leading edge of each sector mark, if that sector mark has not been included in a block.

3. Detects the error and generates the error signal $\overline{\text{OVER INDEX}}$. This signal asserts that sector mark zero has been included within a block.

B. Sync Detector

1. Constantly watches for the sync byte, producing the signal $\overline{\text{SYNC}}$ whenever it is found.

2. Recognizes the end of a sync search and generates the error signal $\overline{\text{SYNC ERROR}}$ if sync was not found.

C. State Counter

(Refer to Fig. 7-4, State Counter Logic, and Fig. 5-3, Formatter Timing During Erase.)

The state counter generates the remainder of the signals needed to control the format when writing and interpret what is read.

The State Counter consists of three 4-bit binary counters and decoding logic. The three counters are called BC (Bit Counter), PC (Punctuation Counter) and CC (Construction Counter).

1. Bit Counter

(Refer to Fig. 7-7, Bit Counter Sequence and Fig. 5-2, Bit Counter Timing.)

The BC counts 8 bits per byte. Its terminal carry BCTC is used in many places. Its highest order binary output BCQD is used by the disk write multiplexer to indicate which clock is to be surpressed to become missing clock.

2. Construction Counter

(Refer to Fig. 7-8, Construction Counter Sequence.)

The CC counts the 5 parts of a sector. The first 3 outputs are named Text, Data and Done. The fourth is unused.

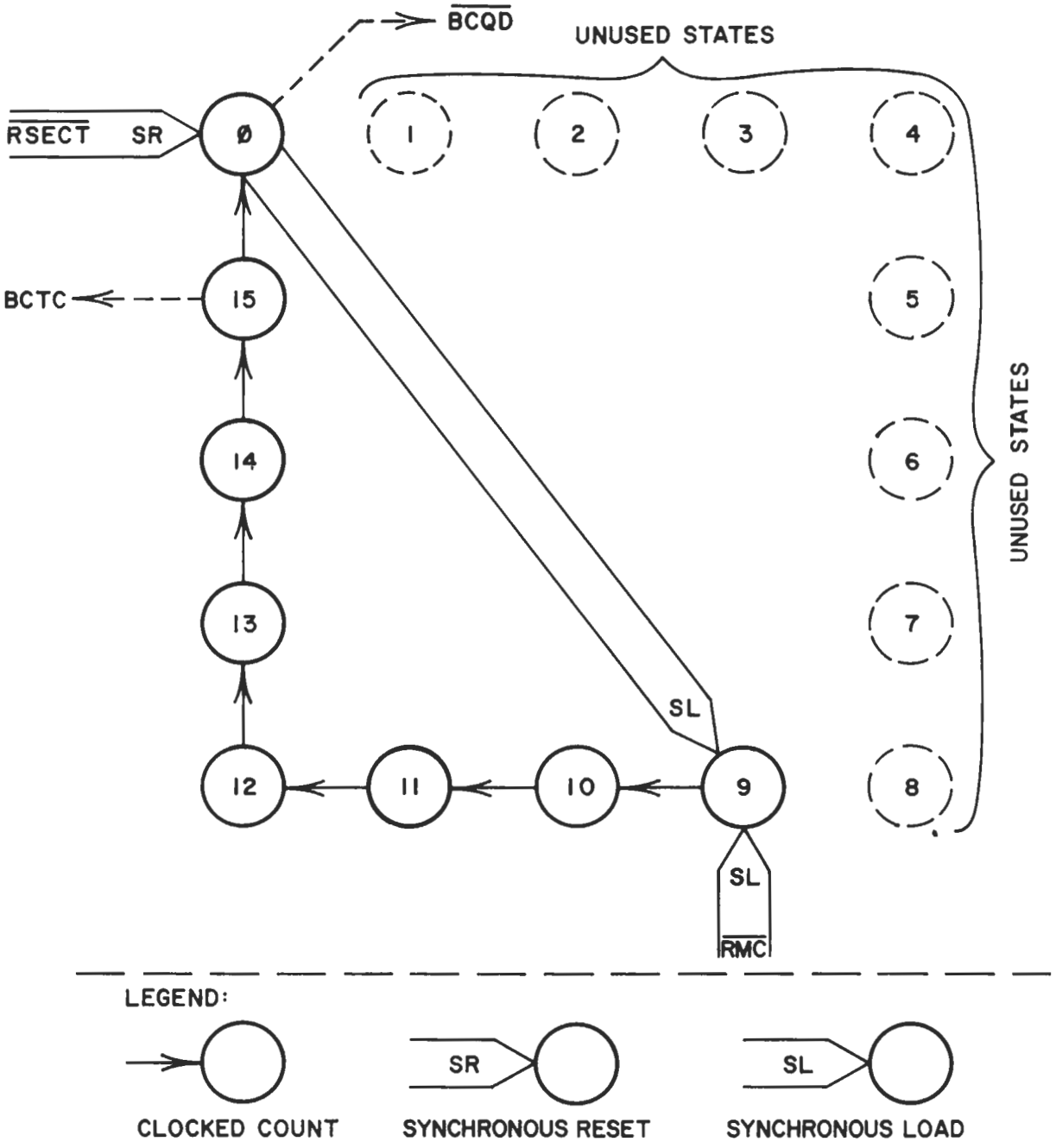


Fig. 7-7 Bit Counter Sequence

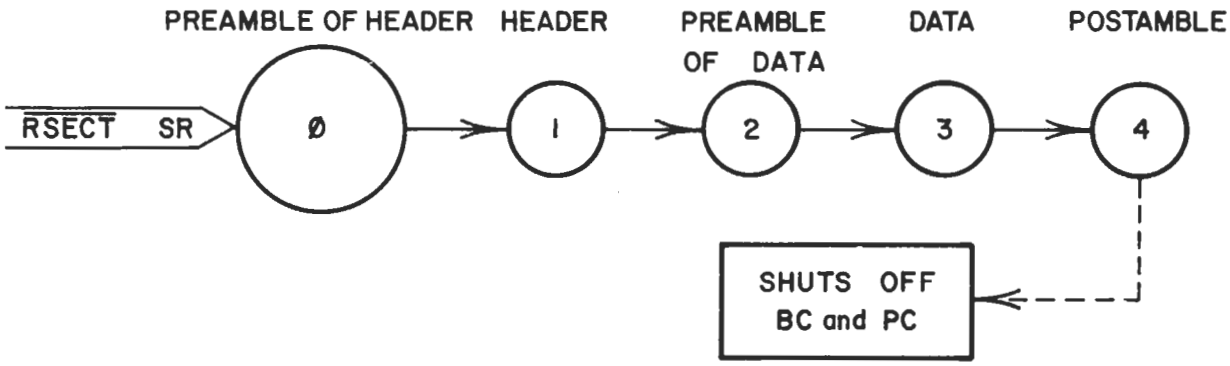


Fig. 7-8 Construction Counter Sequence

3. Punctuation Counter

(Refer to Fig. 7-9, PC And Key Sequence and Figures 7-10 through 7-13, State Counter Diagrams.)

The PC counts bytes. For Header, it counts 13 bytes of data, 2 of CRC, 1 sync (if writing), or (together with KEY) 20 bytes if reading. For Header preamble it (together with KEY) counts 16 bytes if writing, counts 24 bytes of search for sync if reading. For Data preamble it (together with KEY) counts 16 bytes if writing, counts 20 bytes of search for sync if reading.

For Data, byte counting is done elsewhere, except for the last 3 bytes (CRC and SYNC) which are counted by the PC.

Counts of 13 or 14 in the PC always indicate the 2 CRC bytes. A count of 15 always indicates the sync byte. The counts of 12, 13, 14, 15 are individually decoded and are collectively described by the signal $\overline{\text{PCHI}}$.

The $J\overline{K}$ FF Key in the Jump Logic, functions as part of the PC. It is set to 1 after the PC passes 12, and to Ø by $\overline{\text{RESECT}}$ or after $\overline{\text{SYNC}}$ or PC Terminal Carry. It is used to permit sync searches of more than 16 bytes.

SETHOLD RQST (SET HOLD REQUEST) initiates DMA transfers. $\overline{\text{DMAX}}$ parallel loads the PC to 13 (29) to write the CRC checked + Sync after the requested number of bytes have been written on disk by DMA. (DMA exit.)

7.11.4 TRANSFER COMMAND SEQUENCES

Because of hardware limitations of the disk drive, controller and formatter, not all the possible sequences of transfer commands are allowed.

1. For less than one minimum sector after writing, the read amplifiers in the disk drive are saturated, and it is not possible to get into sync. Attempts to read immediately after writing may result in aborts.

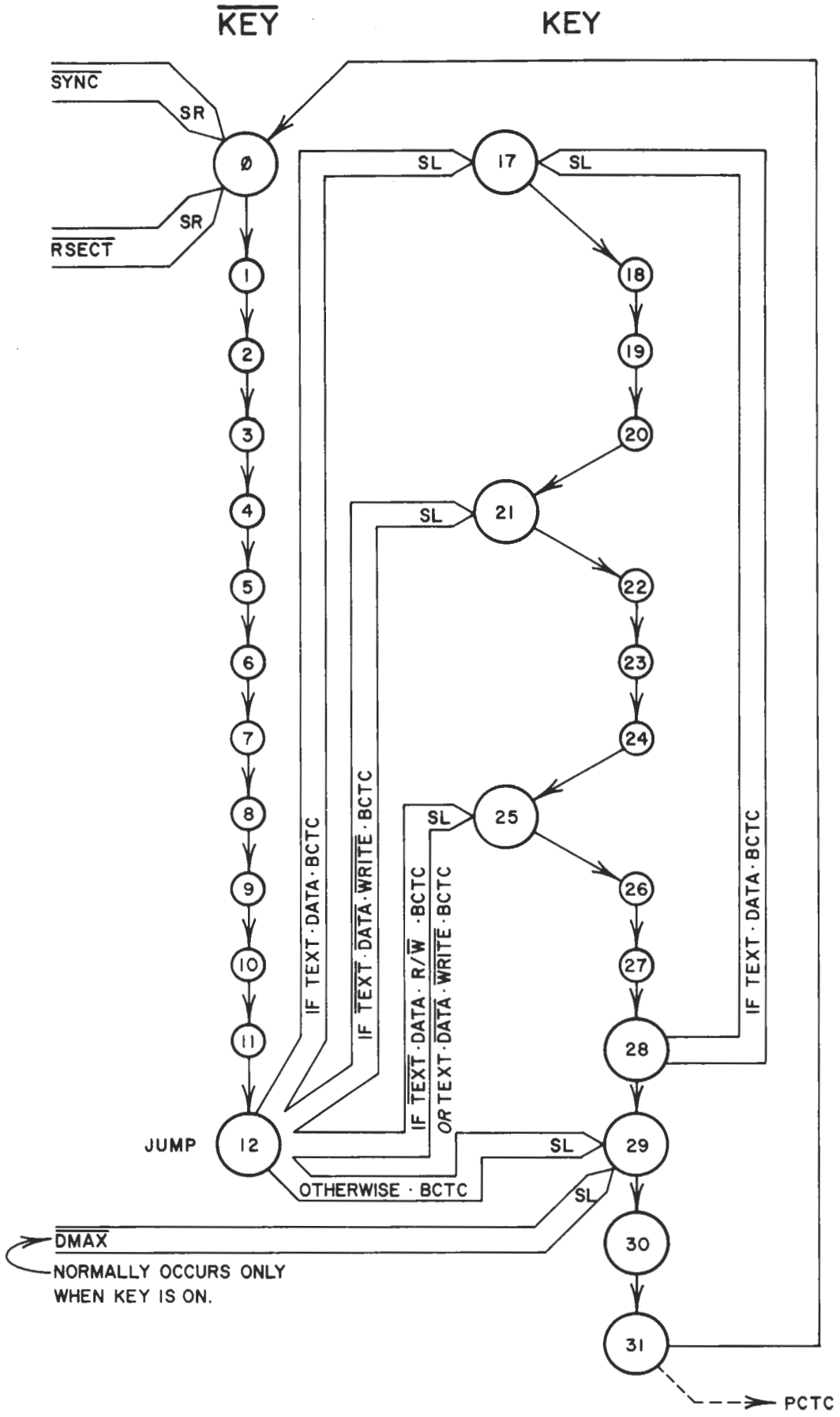


Fig. 7-9 PC And KEY Sequence

2. Only one transfer command may be pending at a time. There is storage only for one. Upon receipt of a transfer command, the SREADY status bits will go low (not ready). It will stay low until the transfer is complete. Do not send a transfer command if SREADY is low. (For an exception to this see 3c and d, below.)

   Note that SREADY may be low for other reasons.

3. The recommended transfer command sequences are as follows:

   a. To Read a Header

      Send Read Header and examine the result. Repeat until the desired one is found.

   b. To write Header, find the previous one as in a, then (within 10 ms) send Write Header.

   c. To read Data, find the correct Header as in a. Then send Read Data (within 300 ns).

   d. To write Data, find the correct Header as in a, then send Write Data (within 300 µs).

   Note that in c and d it is not practical, or necessary, to wait for SREADY AFTER reading Header. The data is in memory when TC status bit becomes a 1, you have about 300 µs to send a new transfer command. If you miss the timing, an abort will appear at the beginning of the next Header. If the transfer command was a write, it has not happened yet, but will happen in the wrong place. It can be prevented by sending a transfer command describing no transfer (1 in all 4 bits).

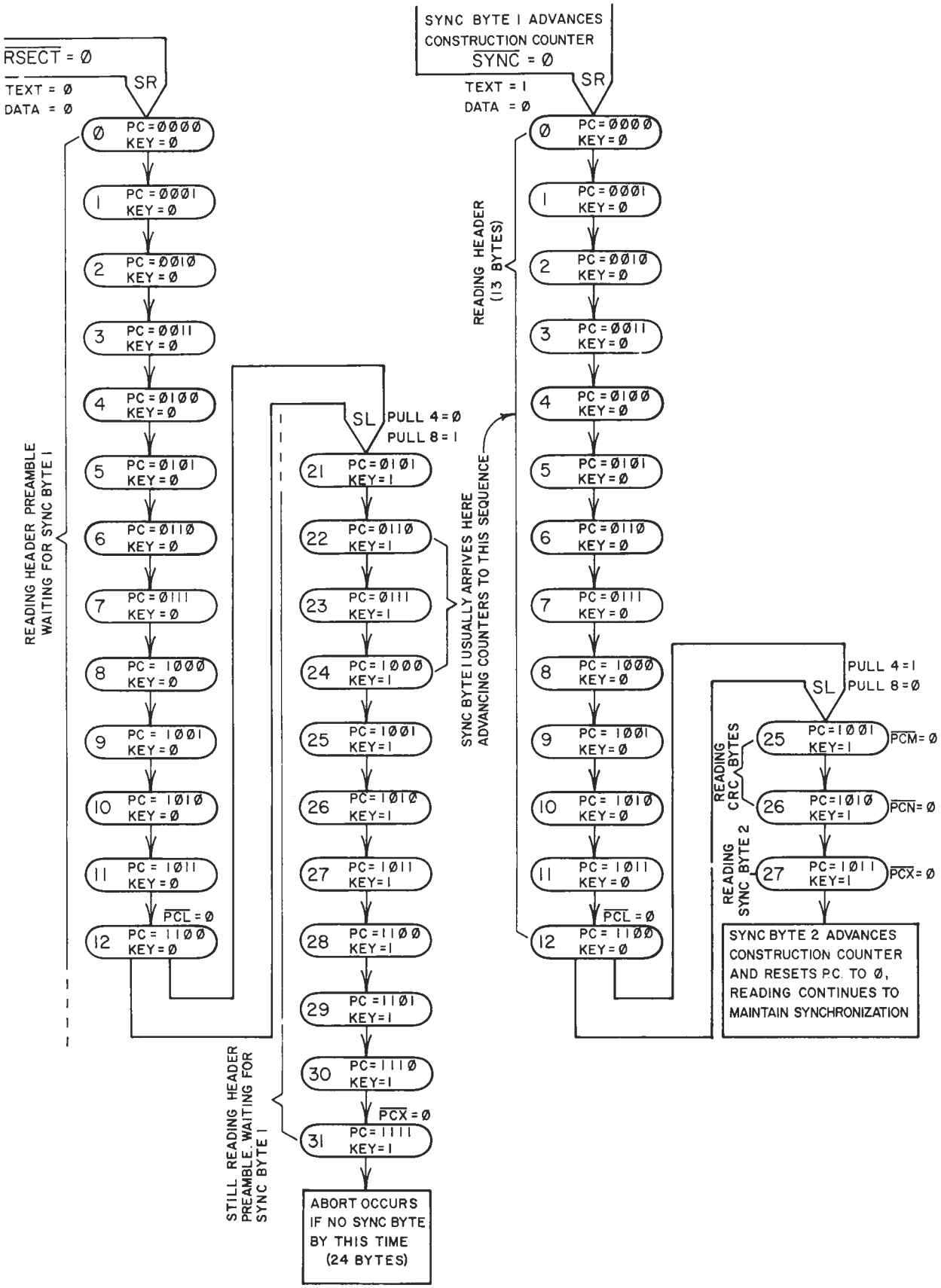


Fig. 7-10 State Counters During Read Header Command

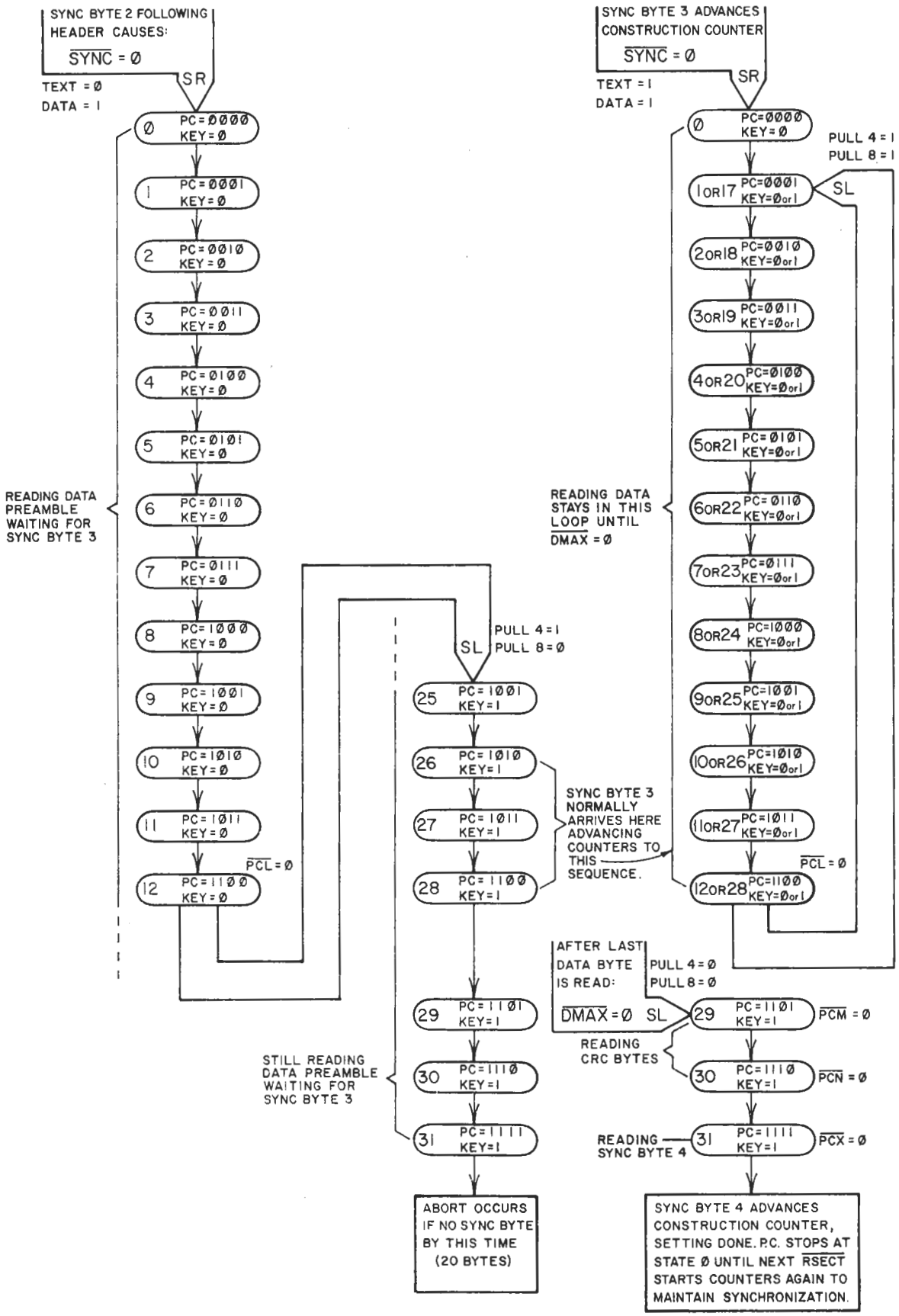


Fig. 7-11 State Counters During Read Data Command

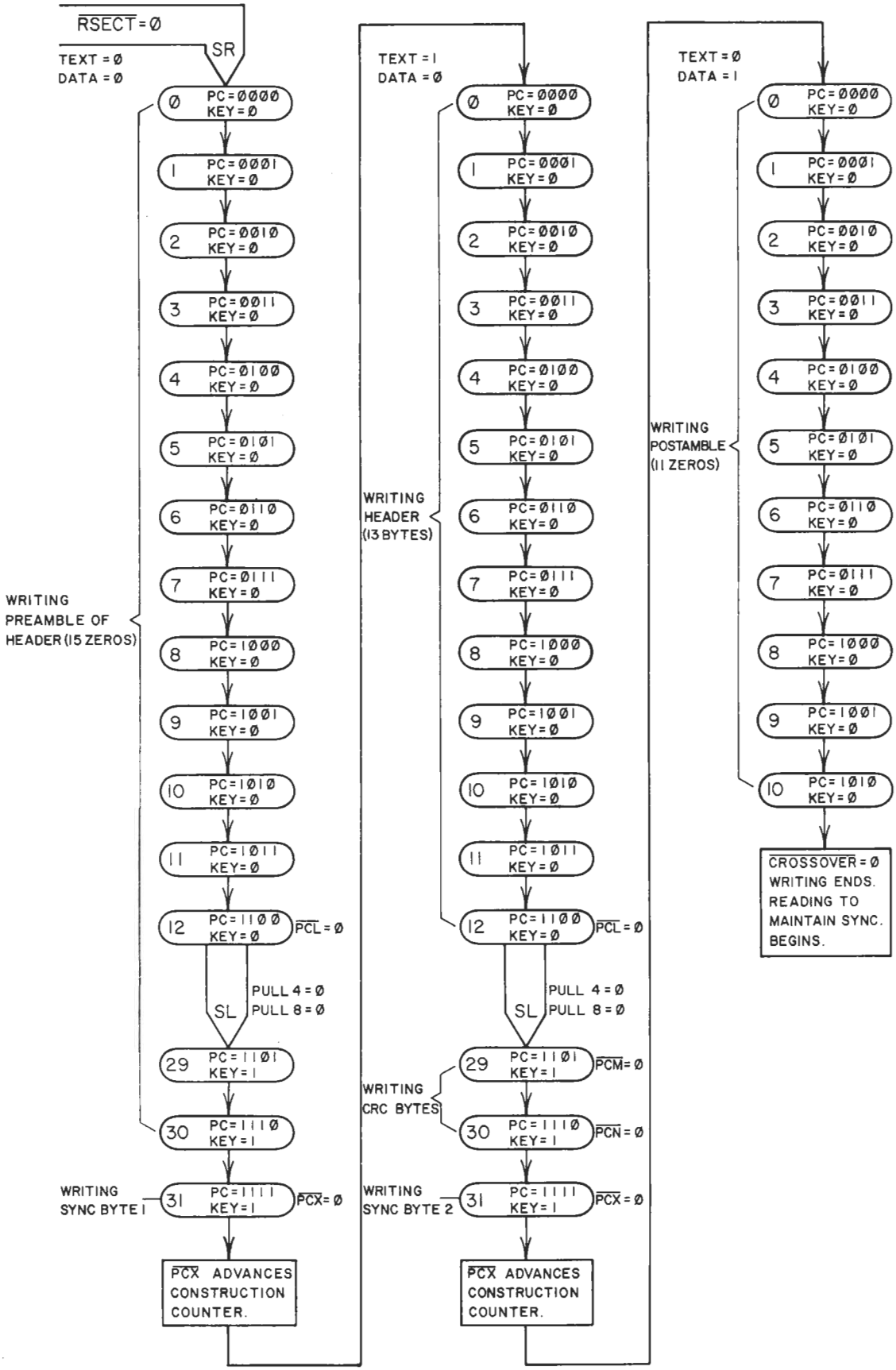


Fig. 7-12 State Counters During Write Header Command

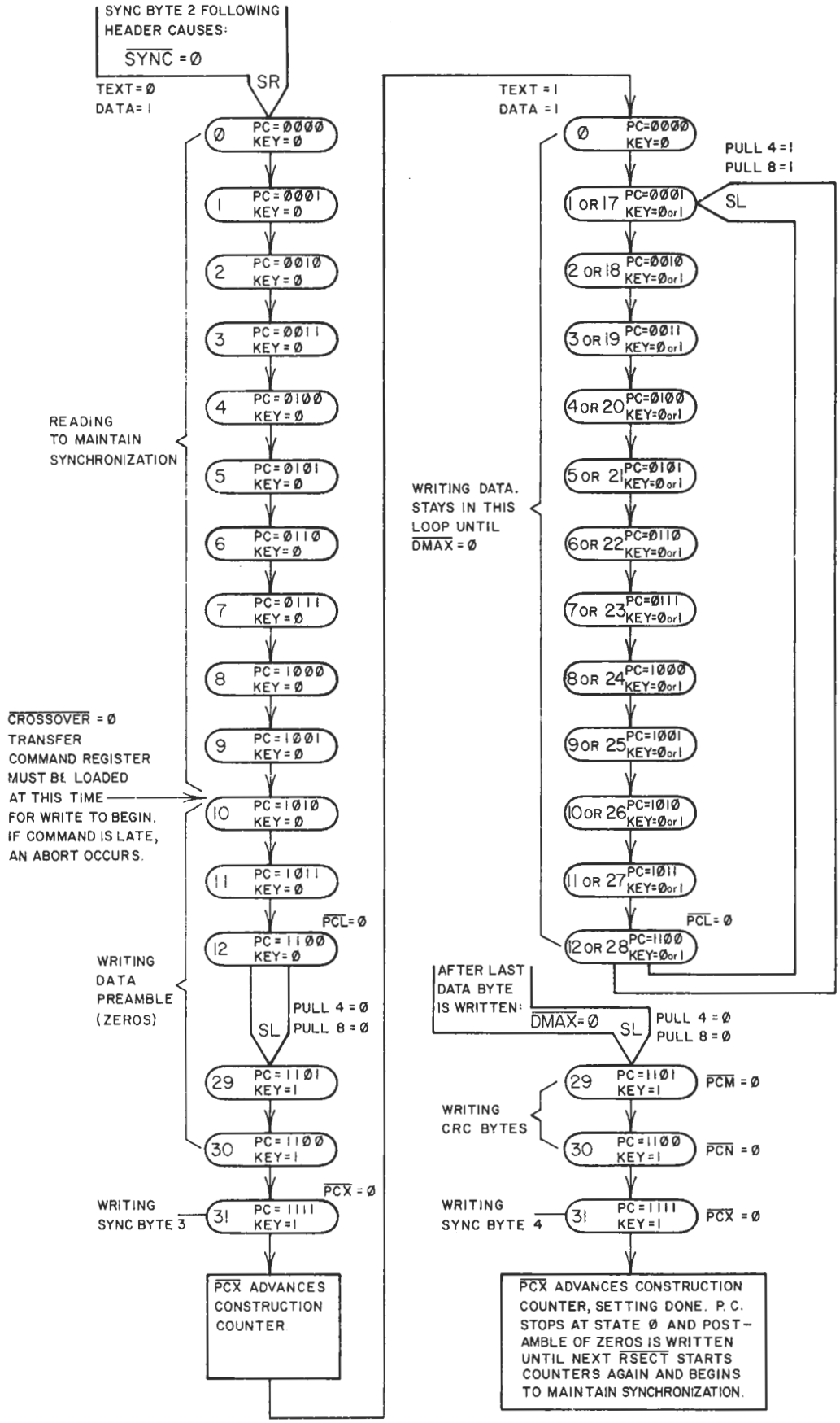


Fig. 7-13 State Counters During Write Data Command

NOTES

Fig. 7-14 Helios II Dual Diskette Drive Cabinet (Model 2)

7.12 DISKETTE DRIVE

7.12.1 ELECTROMECHANICAL DESCRIPTION

A. Head Loading Actuator

Each diskette is moved into contact with its read/write/erase head by a solenoid-controlled head actuator. An interface signal separately activates each head-load actuator and allows a pressure pad to bring the selected diskette into contact with the read/write/erase head with the proper contact pressure.

B. Head Positioning

The two read/write/erase heads are mounted on a movable head-carriage.

The head carriage is actuated by an electro-magnetic actuator utilizing a servo-driven coil moving within a permanent stator (voice coil motor). Positioning of the head with respect to the diskette is determined by the magnitude and direction of the current introduced into the coil windings.

The electromagnetic positioner moves the carriage to position the head at any of 77 positions. It is possible for the positioner to move the head directly from one position to another without returning to a reference point.

C. Diskette Surface Accessibility

Only one surface of the diskette is accessible by each single movable read/write/erase head. At the present time, diskettes are initialized and used only on the back side (side opposite to the label side). The design has provisions to accommodate future possible recording on both sides of the diskette. This feature requires that the drive be able to sense the offset index hole when the diskette is inserted into the drive 180° from its presently-used orientation.

D. Remote Eject Option

A remote diskette eject option is available, allowing the controller to eject a diskette at the end of a job. When this option is installed, a low logic level on Pin 14 will eject a diskette from Unit Ø; a low logic level on Pin 32 will eject a diskette from Unit 1. These lines must be held low for 1 second to ensure proper activation of this function. The option can be installed on either or both sides of the dual drive.

7.12.2 ELECTRONIC DESCRIPTION

A. Data Recording Scheme

A double frequency encoding scheme is used whereby each data bit is preceded by a clock bit. Each byte is written starting with the high-order clock bit, then the high-order data bit, and so on until the low-order data bit is finally written. The presence of a magnetic flux transition represents a binary one. Clock bits are binary ones unless otherwise noted. A byte with a value of binary zero comprises eight clock transitions and no data transitions.

B. Controller Seek Monitoring

The controller monitors the seek time and, if the desired track has not been located within the allocated time, the controller initiates a recalibration of the positioning system, causing the head to be repositioned to track ØØ.

C. Data Separator PCB

A phase-locked data separator for double frequency code (FM) is incorporated in the Helios II diskette drives. SEPARATED CLOCK is presented to the controller interface at P1 Pin 50, and SEPARATED DATA at P1 Pin 48. The phase-locked loop removes jitter due to peak shift from these signals.

SEPARATED CLOCK IS A 200 ns transition to logic low state for every "clock bit" written on the diskette. SEPARATED DATA is a similar transition for every "data bit" written on the diskette. A is connected to C on the data separator module for this output.

An alternative jumper connection on the data separator also provides data pulses on the clock line and clock pulses on the data line during a soft-sectored address mark, to simulate the action of a "1-shot" type of data separator. B is jumpered to C on the data separator module for this option. Both connections work as described with soft-sectored formats and with hard-sectored formats. Three bytes of data is required to synchronize the data separator.

D. High-Speed Seek

(Refer to Fig. 7-15, Simplified Controller Design Configuration with Fast Multi-Track Seek and Restore.)

A high-speed seek feature shortens maximum seek time to 100 ms. This makes use of the restore line and seek-complete line as well as step and direction. Step pulses for high-speed seek may be transferred at rates from 30Khz to 500Khz. A seek-complete indication is given by a logic low on P1 Pin 10 when the drive has settled within 0.001" of track center. On power turn on, or in the event of a missed seek, a logic low for 500 ns or greater will cause the drive to find track ØØ.

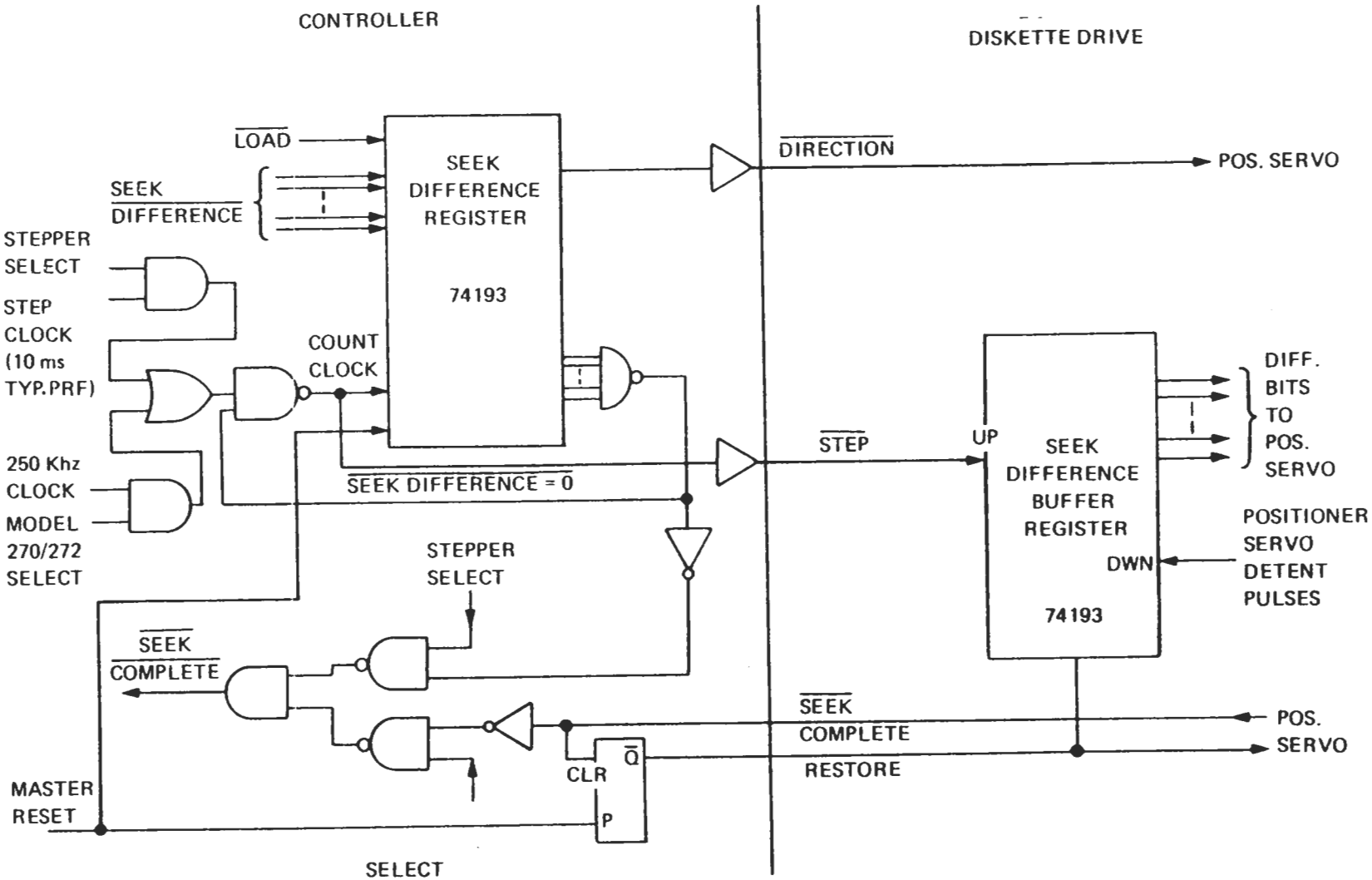


Fig. 7-15 Simplified Controller Design Configuration with Fast Multi-Track Seek and Restore

The simplified controller design configuration (Fig. 7-15) illustrates utilization of the fast multi-track seek and restore-to-track ØØ option capability while simultaneously employing their conventional stepper motor interfaces.

E. Parallel Operation and Unit Selection

(Refer to Fig. 7-16 for two drive parallel wiring diagram.)

For systems containing two or more dual drives, a terminator resistor pack (U5) must be located in the drive farthest electrically from the controller.

A selector module must be installed in U11 to identify the drive by number in a multidrive system. (See Section 4.2.2, Multi-drive System Configuration.)

In any multidrive system, selector units must be installed in each drive so that no more than one drive is enabled at a time. Within each drive all interface signals are controlled by this drive-enable logic.

A drive is identified to serve a pair of units by the presence of a unit selector in socket U11 on the Data and Interface PCB of the disk drive. This unit selector decodes one of the four possible binary combinations of -DRIVE SELECT 1 and -DRIVE SELECT 2 and enables the drive only when that combination appears.

If a drive has no selector installed, it will be enabled for any of the 4 combinations.

A drive being de-selected causes all outputs to go to the high logic state and inhibits all inputs except spindle-motor-enable.

7.12.3 SIGNAL NAMES AND FUNCTIONS

(Refer to Table 7-8, Diskette Drive Power and Interface Pin Connections.)

> NOTE
>
> The names of the signals used in this section are those used on the schematics for the diskette drive. (See Helios II Service Manual.) They are somewhat different from those of the corresponding pin numbers on connector P2 of the controller PCB. (cf. Fig. 8-16, Pin-to-Pin Signal Flow Diagram and Table 8-2, Numerical Pin-to-Pin Assignments, Controller/Drive/Indicator Panel.)

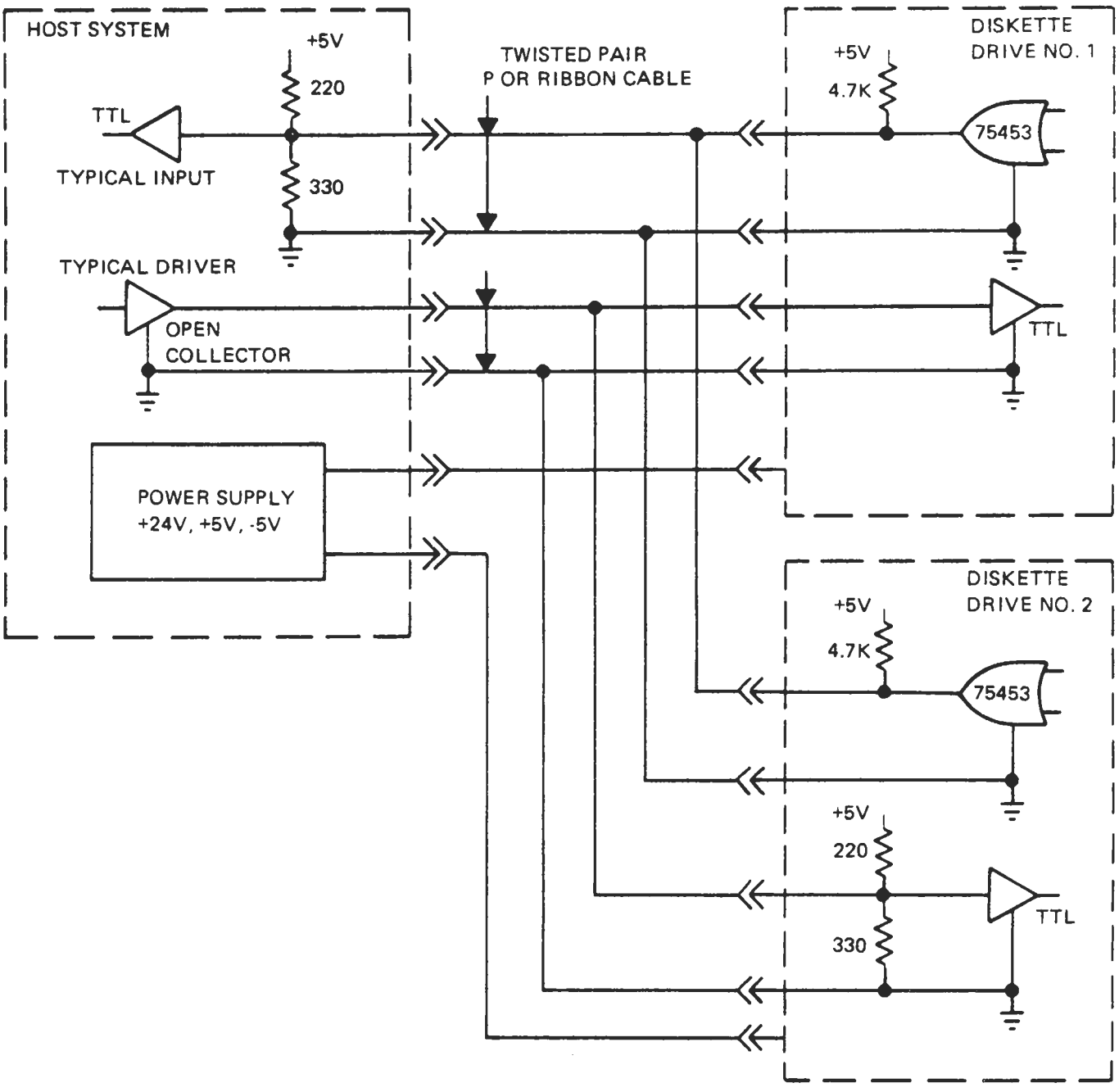


Fig. 7-16 Two-Drive Parallel (Daisy-Chain) Connection Wiring Diagram

Table 7-8. Diskette Drive Power and Interface Pin Connections

P1 - SIGNAL CONNECTOR

(50 Pin PCB Edge Connector-0.1" Centers)

Pin Numbers		
Gnd	Signal	
1	2	DISK SELECT
3	4	HEAD LOAD 1
5	6	READY 1
7	8	INDEX 1
9	10	SEEK COMPLETE
11	12	RESTORE
13	14	REMOTE EJECT Ø
15	16	SPINDLE POSITION PULSES
17	18	HEAD LOAD Ø
19	20	INDEX Ø
21	22	READY Ø
23	24	SPINDLE MOTOR ENABLE
25	26	DRIVE SELECT 2
27	28	DRIVE SELECT 1
29	30	WRITE PROTECT 1
*	32	REMOTE EJECT 1
33	34	DIRECTION SELECT
35	36	STEP
37	38	WRITE DATA
39	40	WRITE GATE
41	42	TRACK ØØ
43	44	WRITE PROTECT Ø
45	46	READ DATA
47	48	SEPARATED DATA
49	50	SEPARATED CLOCK

Mating Connectors

Flat Cable
Scotchflex 3415-0000
or
T&B Ansley 609-5005

Solder Connector
Viking Connector 3VH25/1JN-5
or
TI Connector H312125

*Pin 31 space is occupied by a polarizing key.

P3 - POWER CONNECTOR

(10-Pin Molex-0.156" Centers)

Pin No.	Signal
1	Chassis Gnd
2	+5V DC
3	+8V Unreg.
4	Key
5	+24V DC
6	Gnd
7	Gnd
8	Gnd
9	Gnd
10	-5V DC

Mating Connector

Connector-Molex 09-50-7101

Terminal - 08-50-0106

Polarizing Key - 15-04-0219

2 DISK SELECT

A positive level on this line selects the left unit for connection to the controller read/write interface signals; a negative level similarly selects the right unit. Selection of one of the two heads for the Write operation automatically selects the other head for the Read operation.

4 HEAD LOAD 1

Head 1 remains loaded for the length of time that a negative level is held on this line. This signal is gated by the Drive Select line. Head 1 is the head of the right unit.

6 READY 1

A negative level on this line indicates that a diskette is loaded in unit 1 and is within 90% of operating speed. This signal is gated by the Drive Select line.

8 INDEX 1

This line is normally at the positive level. A one ms pulse to the negative level is transmitted on this line once for each revolution of the diskette in unit 1 as the diskette index hole passes the index hole sensor. This signal is gated by the Drive Select line.

10 SEEK COMPLETE

A negative level on this line indicates that a seek or restore operation has been completed. A positive level on this line indicates that a seek operation is in process. This signal is gated by the Drive Select line.

12 RESTORE

A negative level on this line causes a low-speed repositioning of the heads to Track ØØ. This line takes priority over the Track Address Difference Register lines within the drive. This signal is gated by the Drive Select line.

14 REMOTE EJECT Ø

A negative level on this line energizes a relay that ejects the diskette in unit Ø. This line is held at the negative level for 1 second to allow operation of the eject mechanism. This signal is gated by the Drive Select line.

16 SPINDLE POSITION PULSES

A 4800 Hz ±2% square wave, symmetrical to within ±5%, is presented on this line, synchronized to change in spindle position. The signal is derived from the 800 equally-spaced pulses on the spindle code wheel, each cycle representing 0.45 degree of spindle rotation. This signal is gated by the Drive Select line.

18 HEAD LOAD Ø

Head Ø remains loaded for the length of time that a negative level is held on this line. This signal is gated by the Drive Select line. Head Ø is the head of the left unit.

20 INDEX Ø

This line is normally at the positive level. A one ms pulse to the negative level is transmitted on this line once for each revolution of the diskette in unit Ø (left side when viewed from front panel looking toward rear of drive) as the diskette index hole passes the index hole sensor. This signal is gated by the Drive Select line.

22 READY Ø

A negative level on this line indicates that a diskette is loaded in unit Ø and is within 90% of operating speed. This signal is gated by the Drive Select line.

24 SPINDLE MOTOR ENABLE

Pin 24 of the diskette drive provides controller control of the spindle motor. A logic low on this line enables the spindle servo, such that the spindle turns when a diskette is installed. A logic high inhibits the spindle motor, thus allowing the system to "stand by" at very low power consumption with a diskette loaded.

The spindle motor attains operating speed within 1 second after application of the negative level to this line. This signal is gated by the Drive Select line. Drive interface signal lines Ready Ø and Ready 1 remain at the negative (True) level if the Spindle Motor Enable line is positive (False) and the diskette is present.

26 DRIVE SELECT 2

A negative level on this line selects the drive containing units 4 and 5, and the drive containing units 6 and 7 (the drives in cabinet 2). A positive level on this line selects the drive containing units Ø and 1 and the drive containing units 2 and 3 (the drives in cabinet 1).

28 DRIVE SELECT 1

A negative level on this line selects the drive containing units 2 and 3, and the drive containing units 6 and 7 (the drives in the right-hand side of a cabinet.) A positive level on this line selects the drive containing units Ø and 1 and the drive containing units 4 and 5 (the drives on the left side of a cabinet.)

30 WRITE PROTECT 1

A negative level on this line indicates that the diskette in unit 1 is Write Protected and that the drive write circuitry is prevented from writing on this diskette. (The Helios II does not use the write-protect lines.)

32 REMOTE EJECT 1

A negative level on this line energizes a relay that ejects the diskette in unit 1. This line is held at the negative level for 1 second to allow operation of the eject mechanism. This signal is gated by the Drive Select line.

34 DIRECTION SELECT

The level on this line defines the direction of motion of the head positioner when the Step line is pulsed. A negative level defines the direction as inward (higher track number) and a positive level as outward (lower track number and away from the center).

36 STEP

A 200 ns to 1 µs pulse to the negative level is presented on this line for each track to be crossed by the head during a seek to a new address. The Direction Select level shall be stable for 100 ns prior to the leading edge of this Step pulse. Pulse trains representative of up to 76 tracks of address change may be transmitted at pulse recurrent frequencies up to 500 kHz. The entire pulse train representative of an address change must be transmitted in less than 2.0 ms.

38 WRITE DATA

Write current changes polarity for each positive level to negative level transition on this line. This line shall stay at a negative level for at least 180 ns after such a transition, but should be at a positive level for at least 180 ns before the next positive level to negative level transition. This signal is gated by the Drive Select line.

40 WRITE GATE

Write current is turned on for the duration of time that this line is held at a negative level. The selection of one head for writing automatically selects the other head for reading. This signal is gated by the Drive Select line. Erase current is also controlled by this line.

42 TRACK ØØ

This line is normally at the positive level. A negative level is presented on this line when the heads are positioned over Track ØØ. This signal is gated by the Drive Select line.

44 WRITE PROTECT Ø

A negative level on this line indicates that the diskette in unit Ø is Write Protected and that the drive write circuitry is prevented from writing on this diskette. (Not used in Helios II.)

46 READ DATA

This line transmits the output of the selected head at all times except when the Write Gate is enabled, at which time it transmits the output of the other drive head. Each flux transition on the diskette is represented by a 200 ns ±20% pulse to the negative level on this line. This signal is gated by the Drive Select line.

48 SEPARATED DATA

Separated data pulses from the selected head are presented on this line except when the Write Gate is enabled, whereupon the output is from the other drive head. Data separation is performed by a phase-locked oscillator. Each data pulse is represented by a 200 ns ±20% pulse to the negative level on this line. This signal is gated by the Drive Select line.

50 SEPARATED CLOCK

Separated clock pulses from the selected head are presented on this line except when the Write Gate is enabled, whereupon the output is from the other drive head. Clock separation is performed by a phase-locked oscillator which omits missing clock pulses. Each clock pulse is represented by a 200 ns ±20% pulse to the negative level on this line. This signal is gated by the Drive Select line.

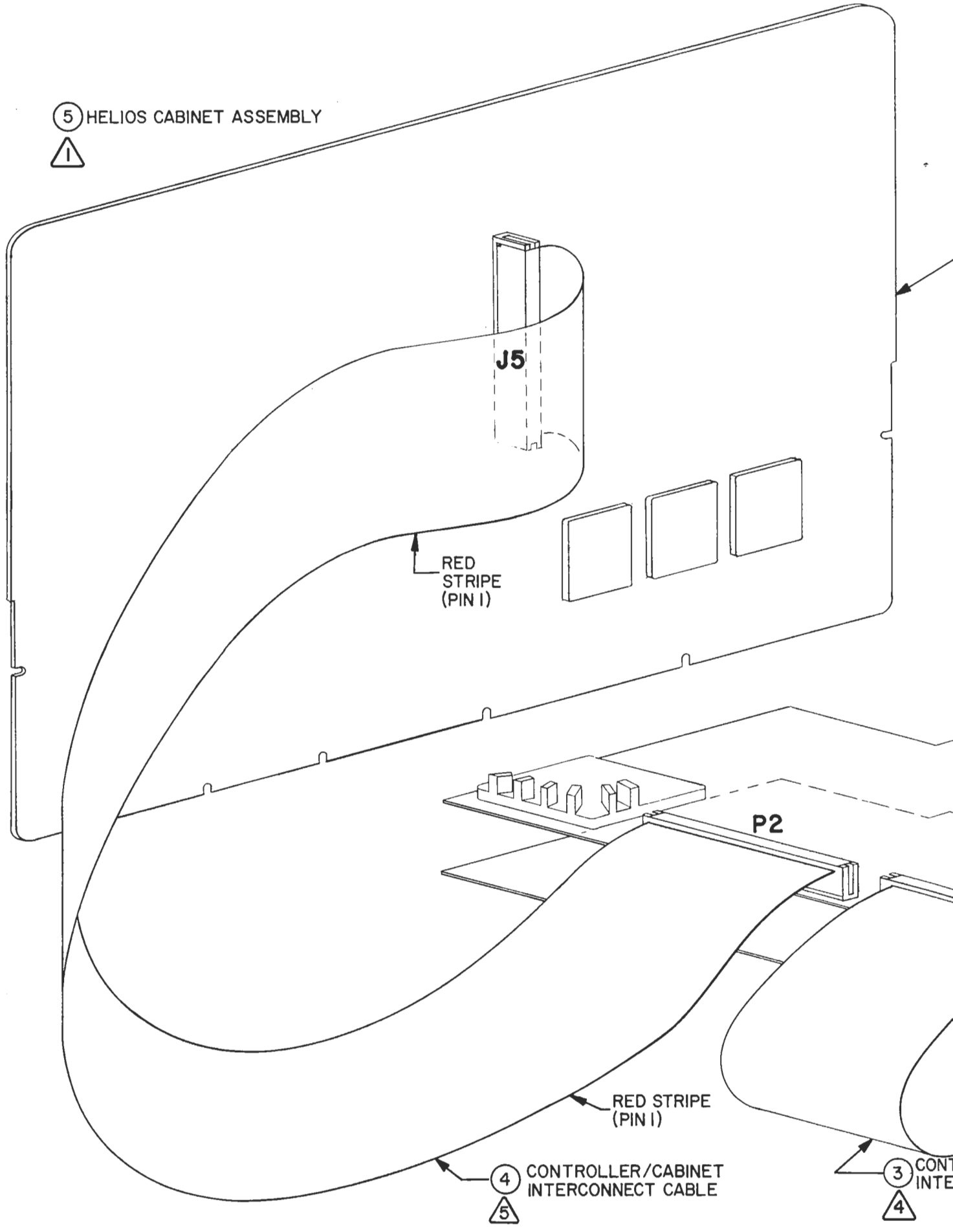
NOTE: When they are designated on the controller/formatter, the signals between controller P2 and drive P1 are prefixed by a minus sign to denote that they are drive signals as opposed to controller/formatter signals and that they are active low with regard to the drive. They do not have this minus sign on the drive vendor documentation. Once processed on either the controller or formatter, they are inscribed with a "not-bar." If inverted the "not-bar" is dropped.

CONTENTS

SECTION 8 DRAWINGS

MODEL 2

MODEL 4


5 HELIOS CABINET ASSEMBLY
1
J5
RED
STRIPE
(PIN 1)
P2
RED STRIPE
(PIN 1)
4 CONTROLLER/CABINET
INTERCONNECT CABLE
5
3 CONT
INTE
4

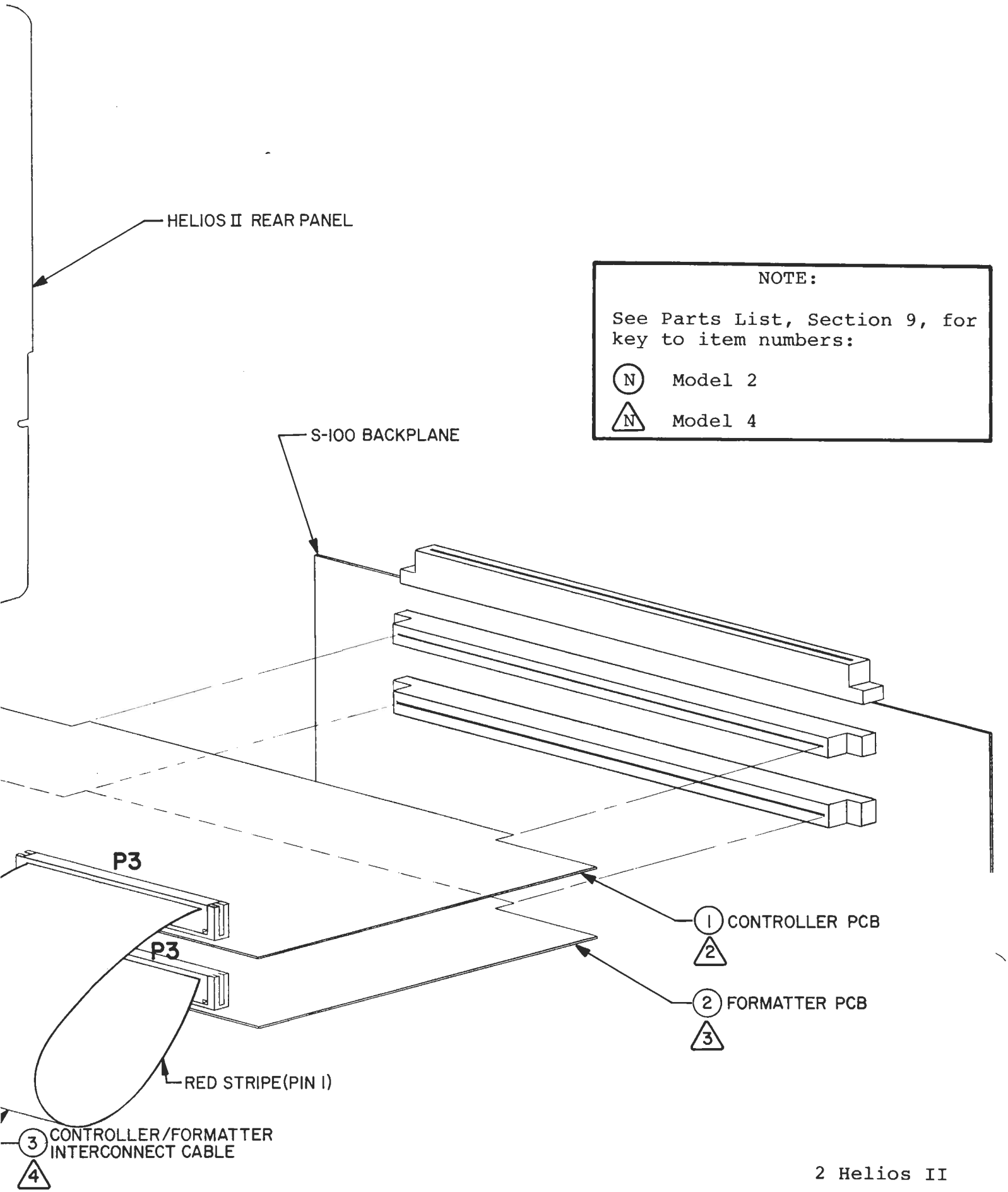
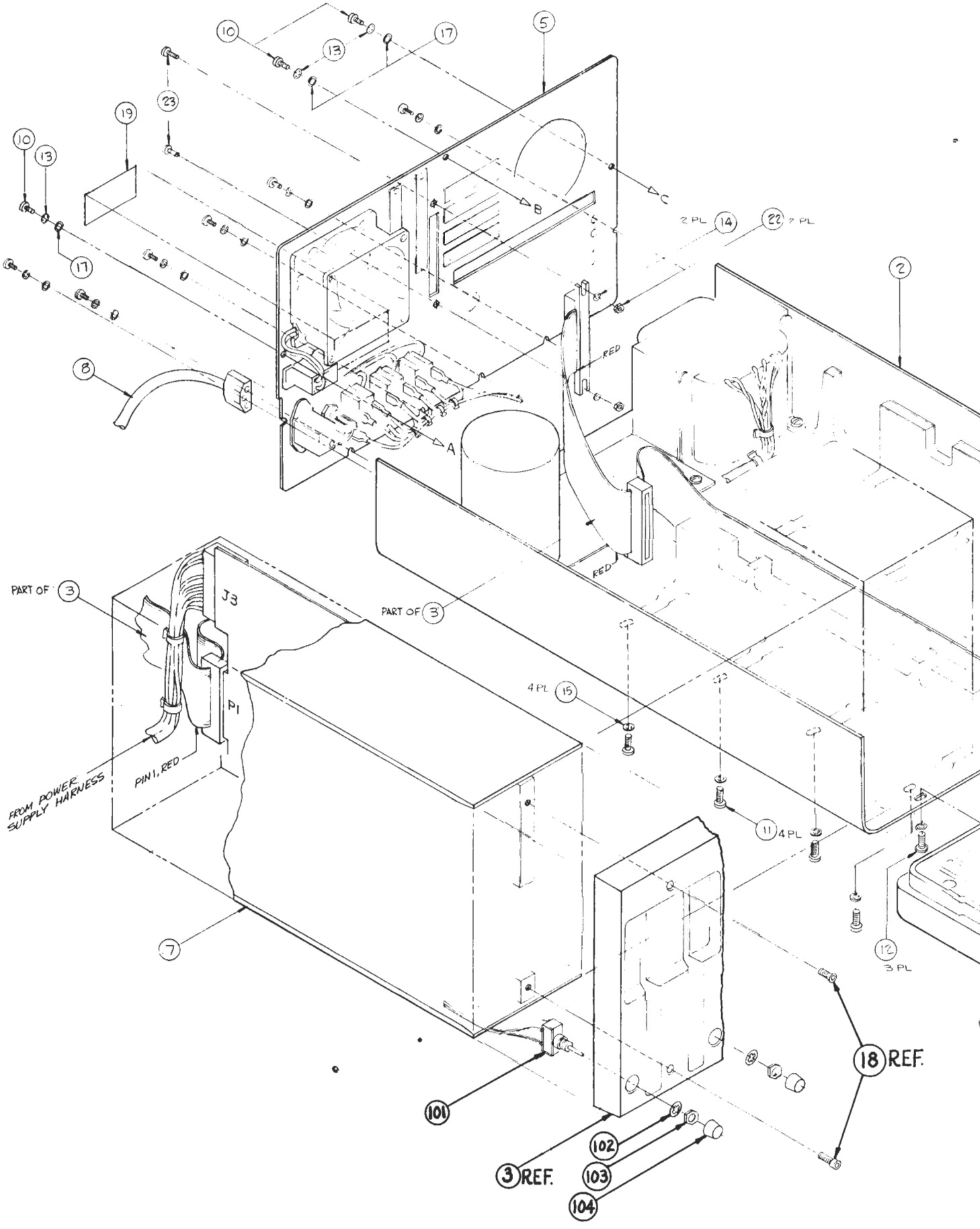
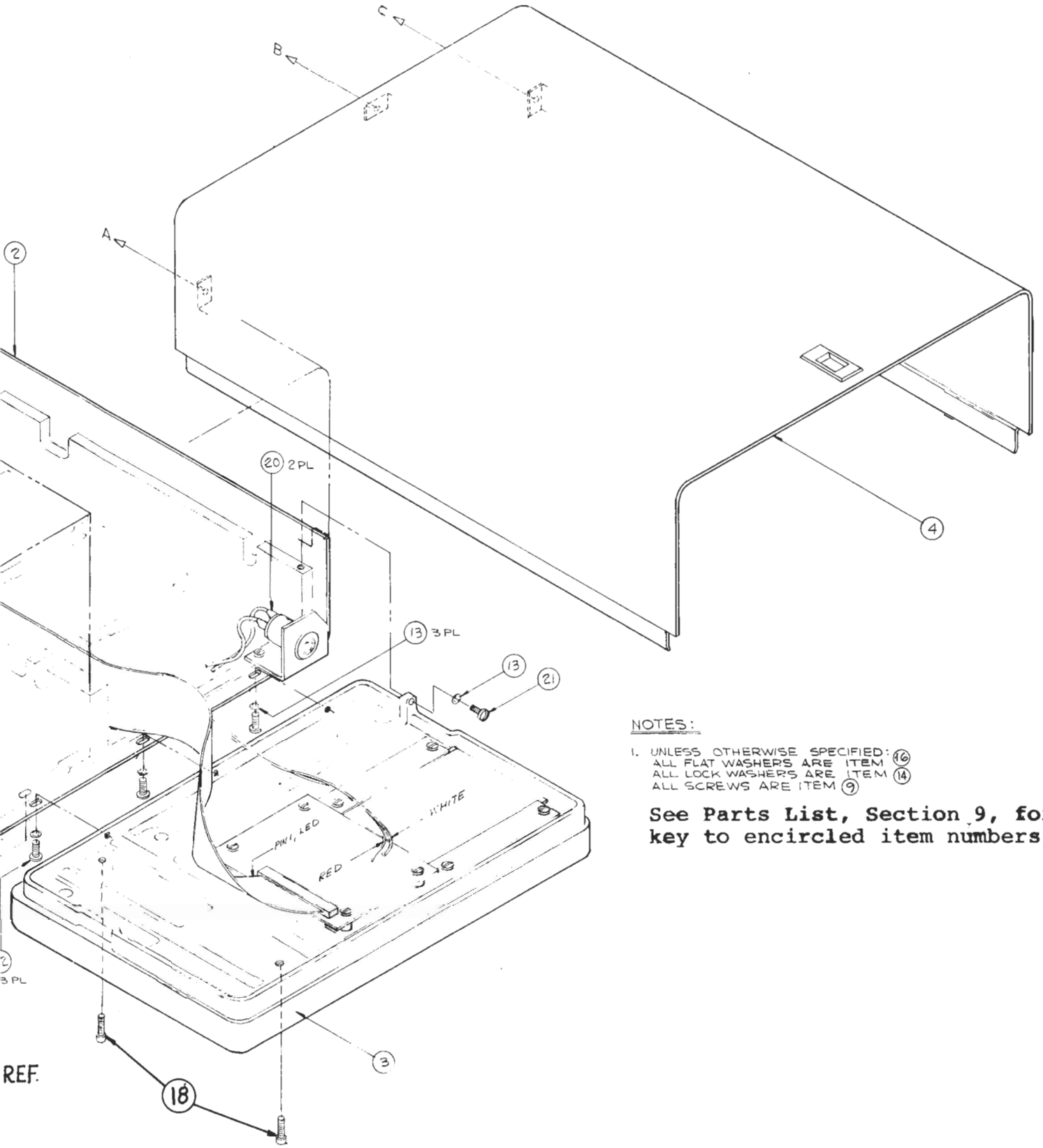


Fig. 8-1 System Assembly, Interconnect Diagram (I-2-7


10
13
17
5
23
19
10
13
17
8
A
B
C
2 PL
14
22
2 PL
2
RED
RED
PART OF 3
PART OF 3
J3
P1
PIN 1, RED
FROM POWER SUPPLY HARNESS
4 PL
15
11
4 PL
12
3 PL
7
18 REF.
101
102
103
104
3 REF.

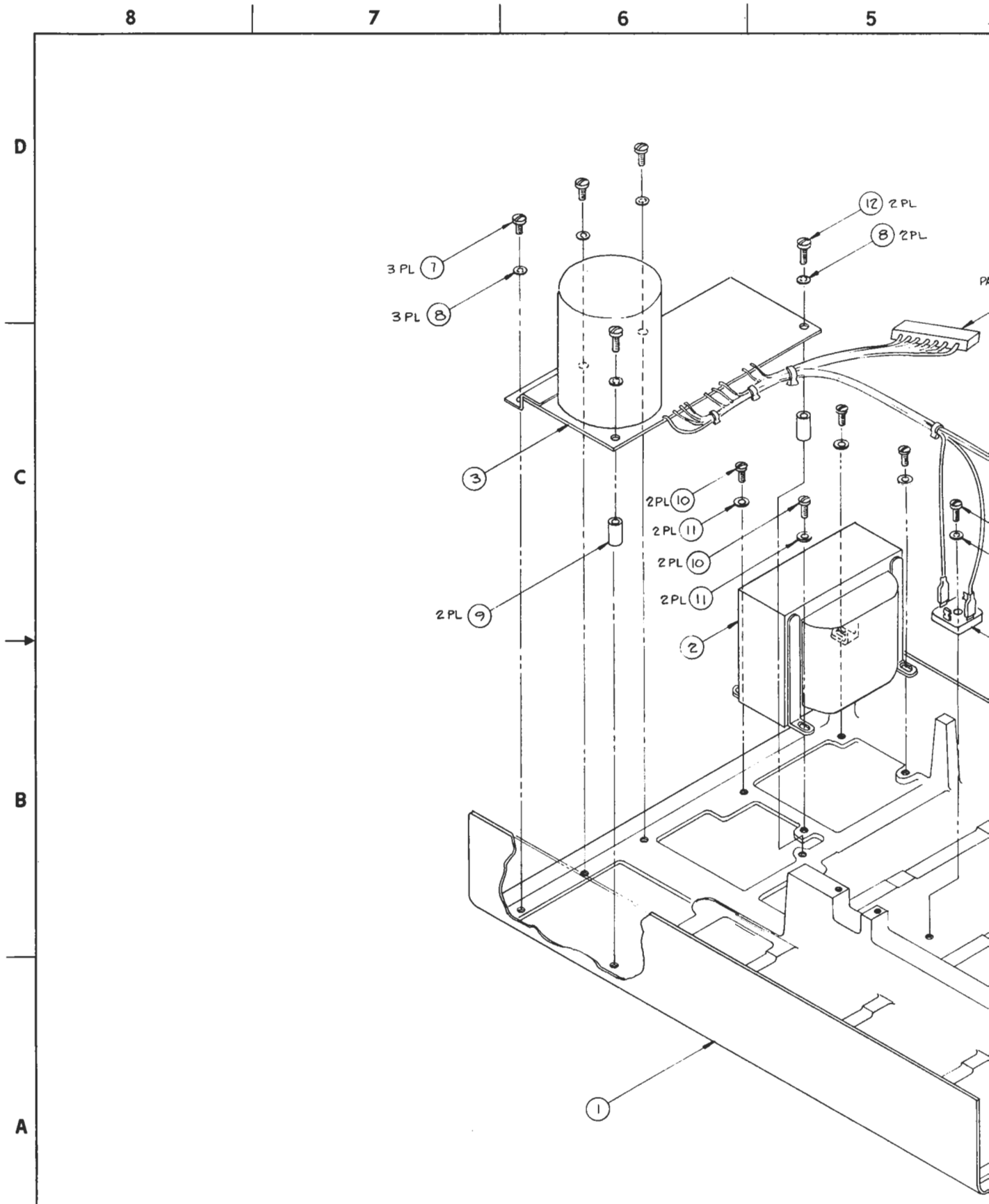


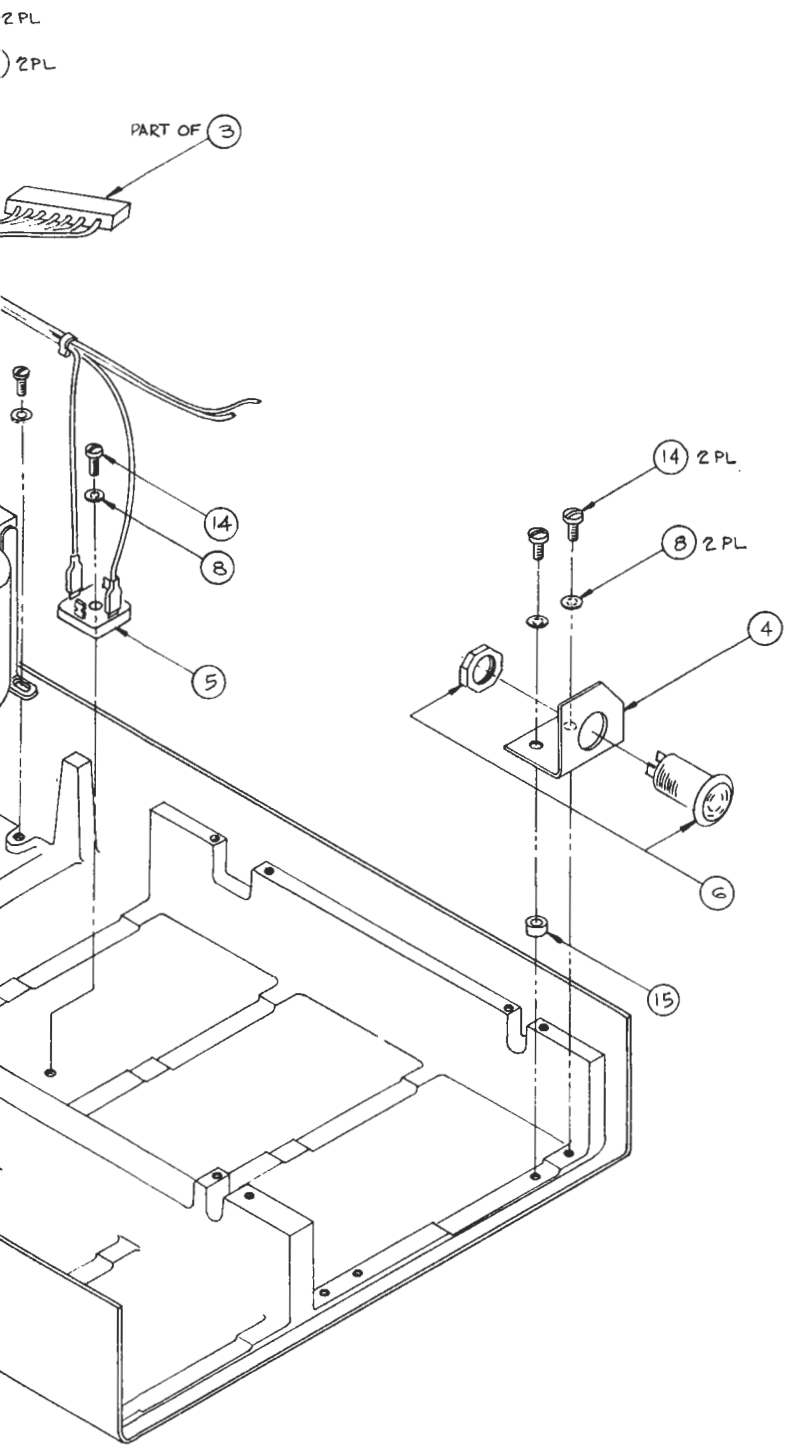
NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL FLAT WASHERS ARE ITEM (16)
   ALL LOCK WASHERS ARE ITEM (14)
   ALL SCREWS ARE ITEM (9)

See Parts List, Section 9, for key to encircled item numbers

Fig. 8-2 Cabinet Assembly, Model 2, Exploded (300000+I-2-78)


8
7
6
5
D
C
B
A
3 PL (7)
3 PL (8)
(12) 2 PL
(8) 2PL
(3)
2PL (10)
2 PL (11)
2 PL (10)
2PL (11)
2 PL (9)
(2)
(1)

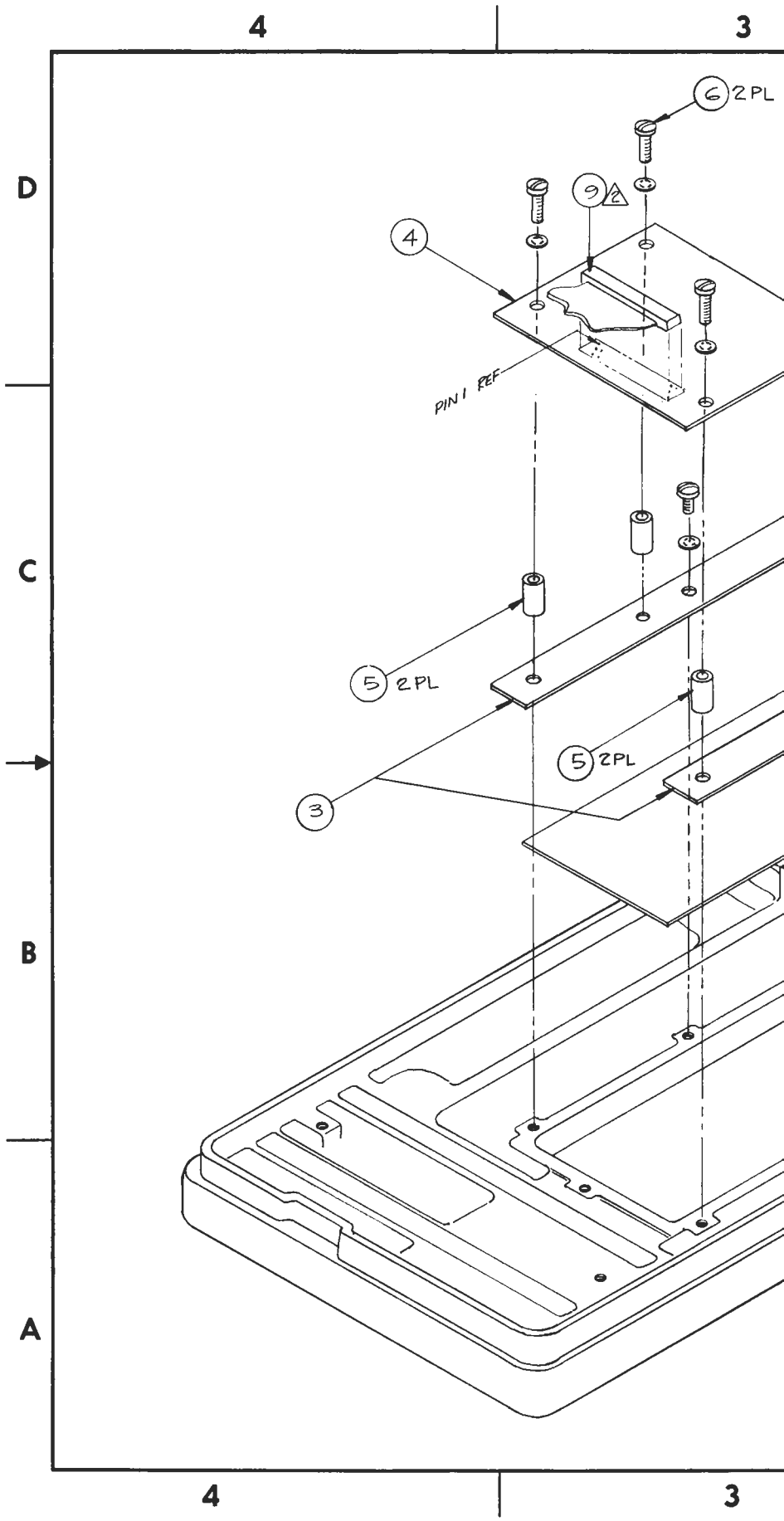


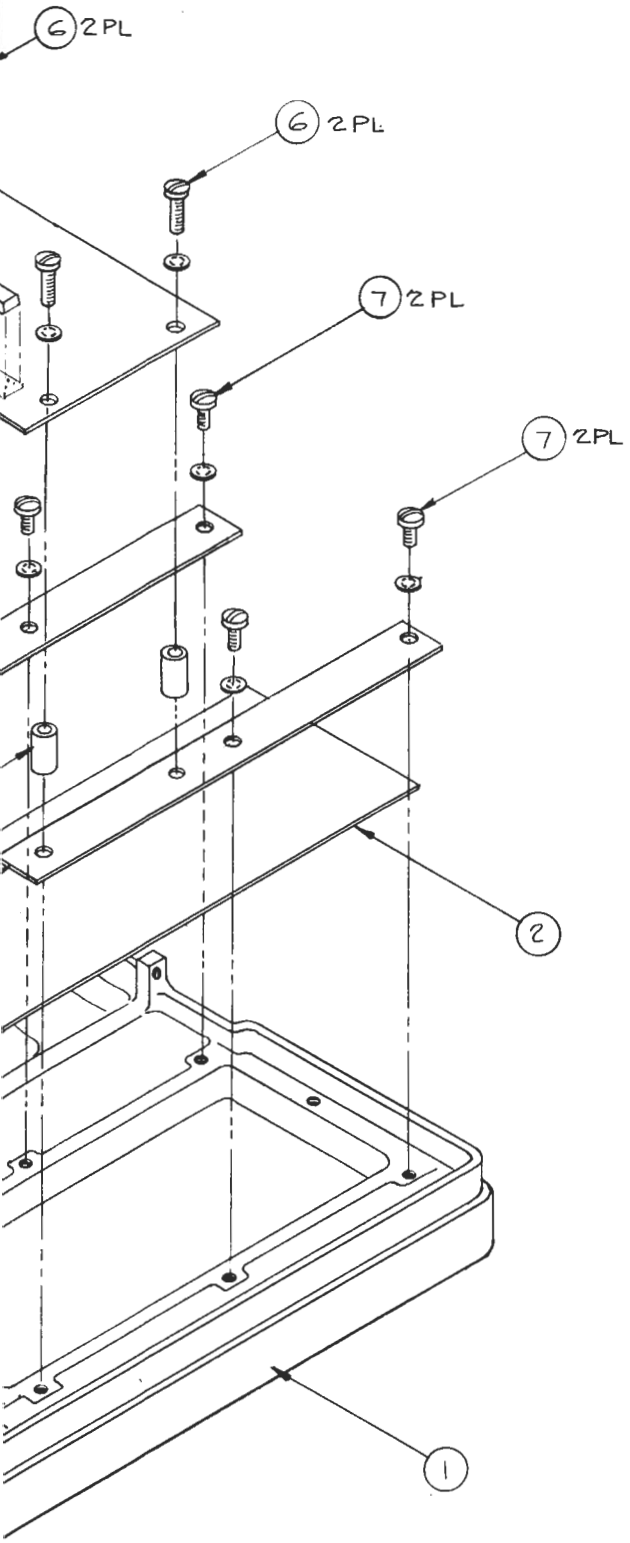
See Parts List, Section 9, for key to encircled item numbers

2 Helios II

302004 D

Fig. 8-3 Base Assembly, Model 2, Exploded


4
3
D
C
B
A
6 2PL
9
4
PIN 1 REF
5 2PL
5 2PL
3



NOTES:

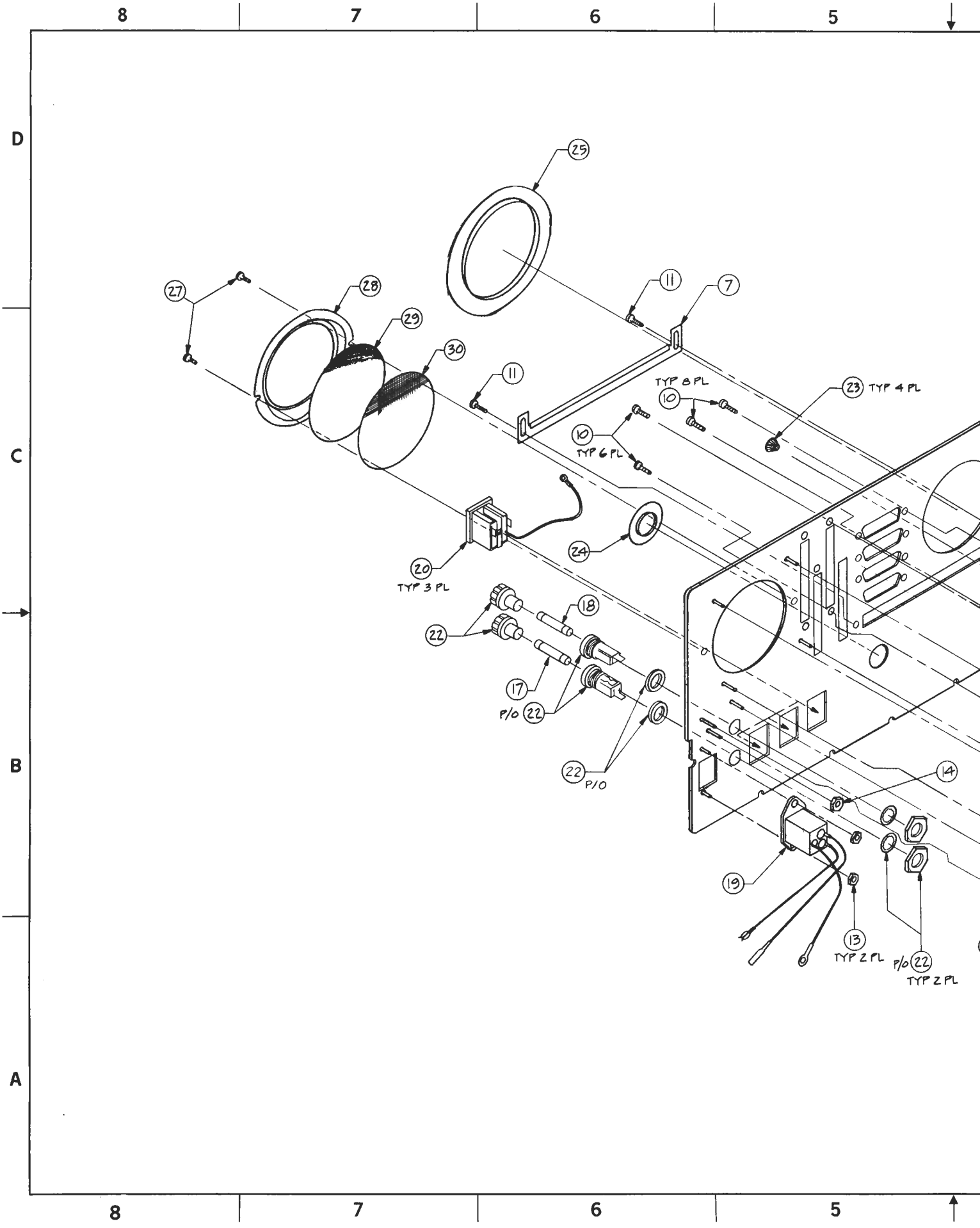
1. UNLESS OTHERWISE SPECIFIED: ALL LOCKWASHERS ARE ITEM 8.
2. SOLDER ITEM 9 TO ITEM 4 AS SHOWN BEFORE ITEM 4 IS MOUNTED TO ITEM 1.

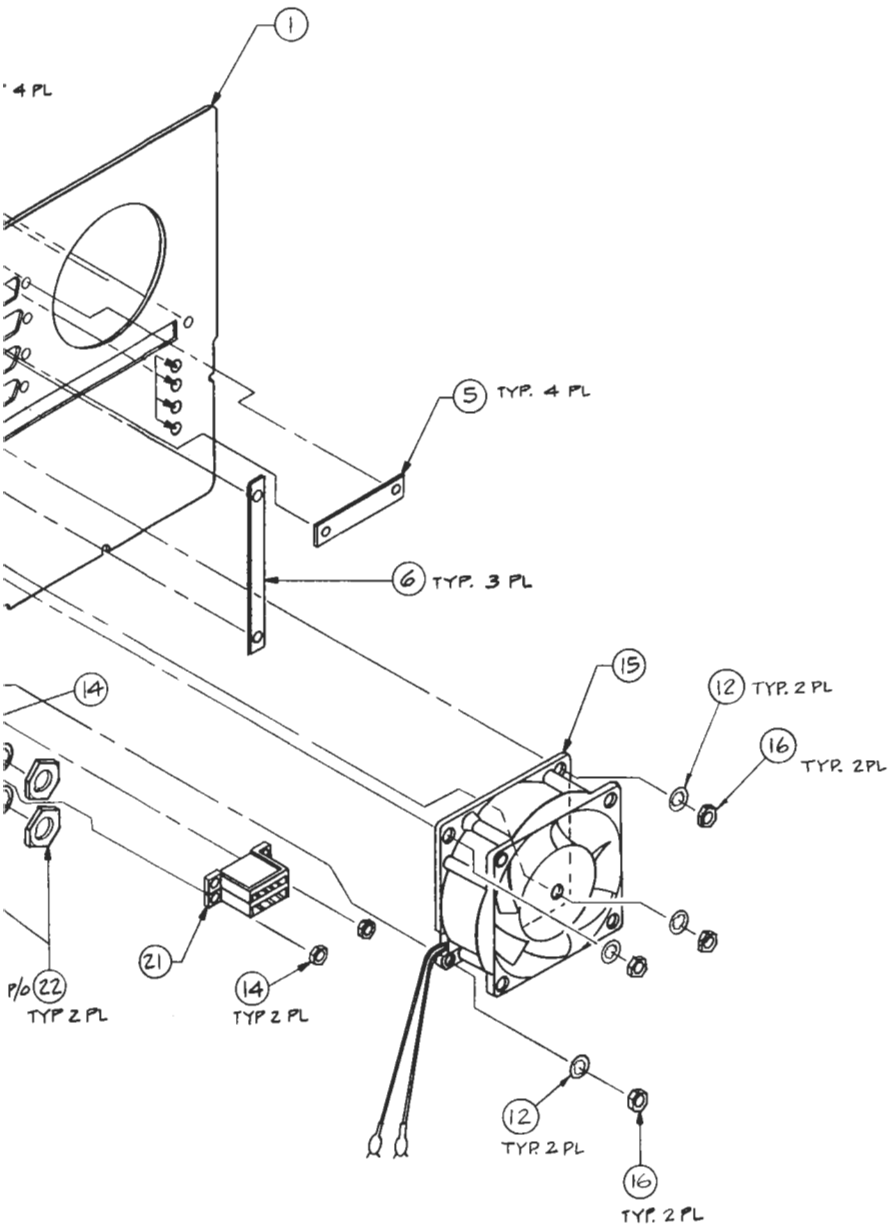
See Parts List, Section 9, for key to encircled item numbers

306000

2 Helios II

Fig. 8-4 Bezel Assembly, Model 2, Exploded (306000E)


8
7
6
5
D
C
B
A
25
27
28
29
30
11
7
11
TYP 8 PL
10
23 TYP 4 PL
10
TYP 6 PL
20
TYP 3 PL
24
18
22
17
P/O 22
22
P/O
14
19
13
TYP 2 PL
P/O 22
TYP 2 PL



NOTES:

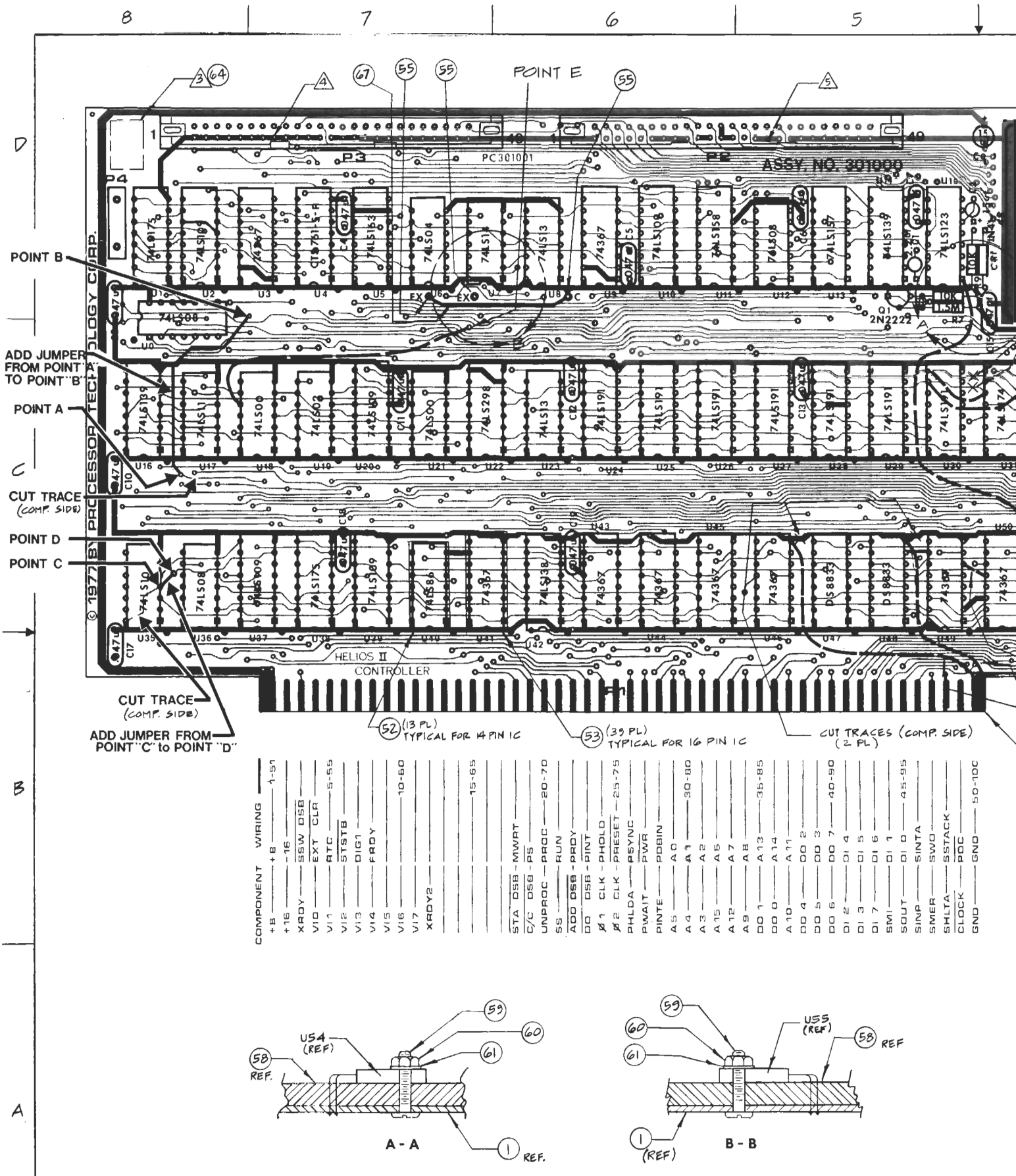
1. FOR AC POWER INTERCONNECT CABLE ④ CONNECTION SEE DWG 30000G (WIRING DIAGRAM, HELIOS II, MODEL 2).

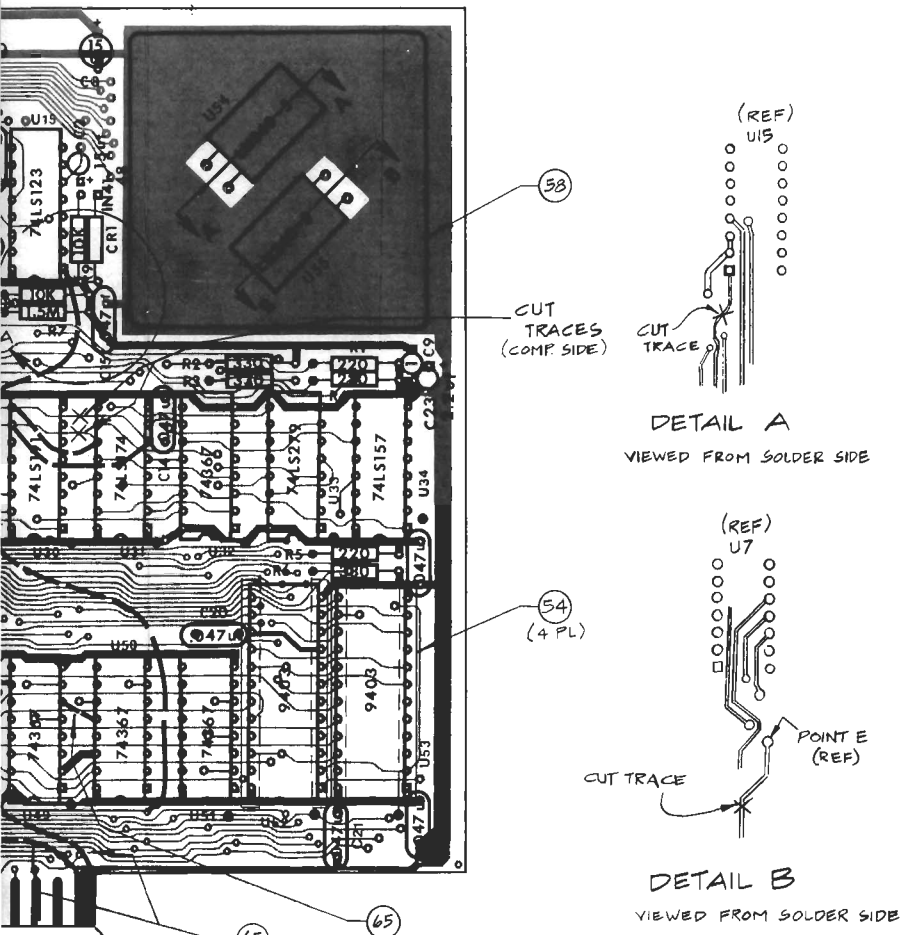
See Parts List, Section 9, for key to encircled item numbers

305000 D

2 Helios II

Fig. 8-5 Rear Panel Assembly, Model 2, Exploded


POINT E
ASSY. NO. 301000
PC301001
P3
P2
P4
POINT B
ADD JUMPER FROM POINT "A" TO POINT "B"
POINT A
CUT TRACE (COMP. SIDE)
POINT D
POINT C
CUT TRACE (COMP. SIDE)
ADD JUMPER FROM POINT "C" to POINT "D"
PROCESSOR TECHNOLOGY CORP.
© 1977 BY
HELIOS II CONTROLLER
(52) (13 PL) TYPICAL FOR 14 PIN IC
(53) (39 PL) TYPICAL FOR 16 PIN IC
CUT TRACES (COMP. SIDE) (2 PL)
Q1 2N2222
COMPONENT WIRING
+8 1-5
+16 5-10
XRDY SSW DSB 10-15
VIO EXT CLR 15-20
VI1 RTC 20-25
VI2 STSTB 25-30
VI3 DIG1 30-35
VI4 FRDY 35-40
VI5 40-45
VI6 45-50
VI7 50-55
XRDY2 55-60
60-65
65-70
STA DSB MWRT 70-75
C/C DSB PS 75-80
UNPROC PROC 80-85
SS RUN 85-90
ADD DSB PRDY 90-95
DO DSB PINT 95-100
Ø1 CLK PHOLD
Ø2 CLK PRESET
PHLDA PSYNC
PWAIT PWR
PINTE PDBIN
A5 A0 30-80
A4 A1
A3 A2
A15 A6
A12 A7
A9 A8
DO 1 A13 35-85
DO 0 A14
A10 A11
DO 4 DO 2
DO 5 DO 3
DO 6 DO 7 40-90
DI 2 DI 4
DI 3 DI 5
DI 7 DI 6
SMI DI 1 45-95
SOUT DI 0
SINP SINTA
SMER SWO
SHLTA SSTACK
CLOCK PDC
GND GND 50-100
U54 (REF)
U55 (REF)
REF.
A-A
B-B
(REF)



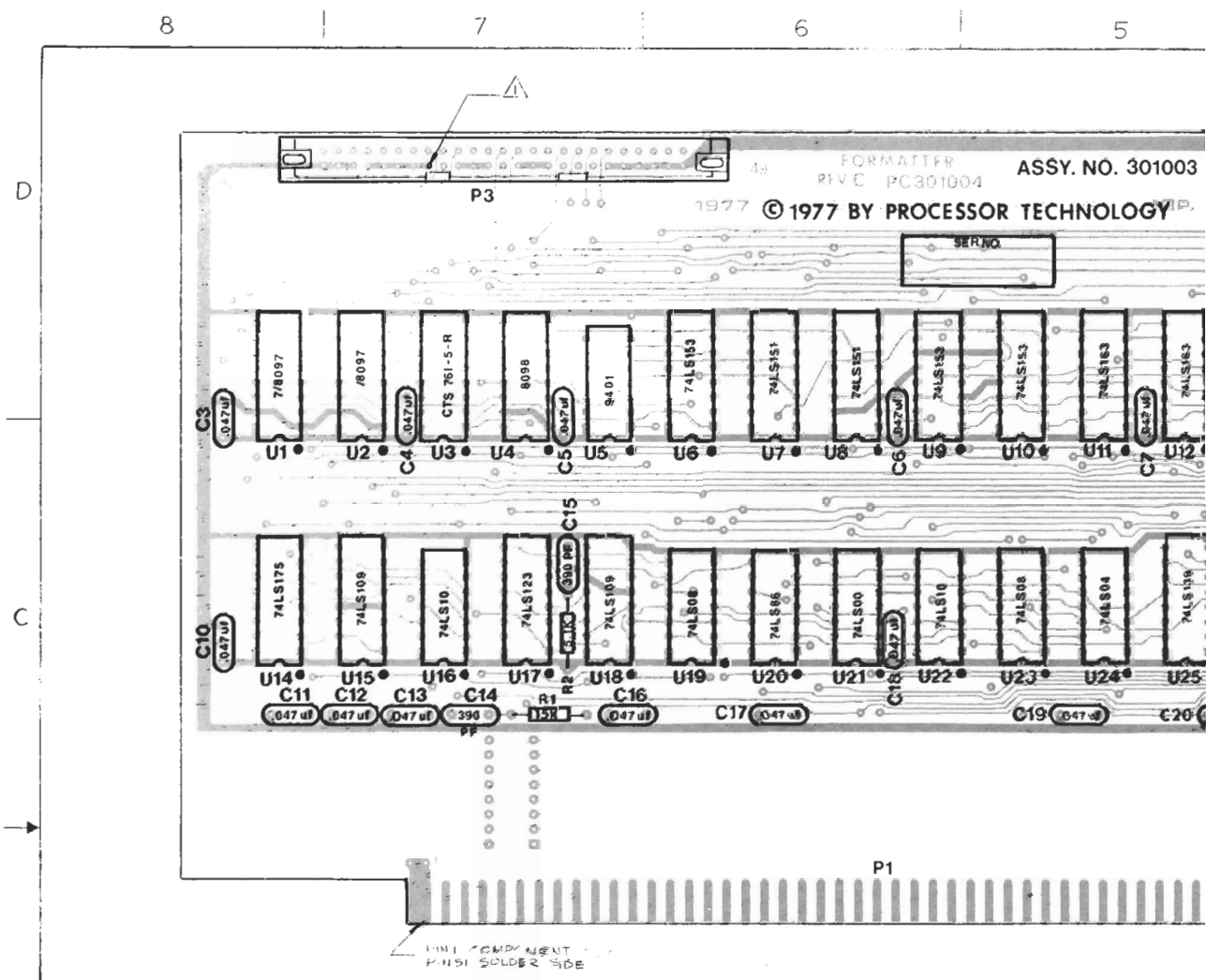
NOTES:

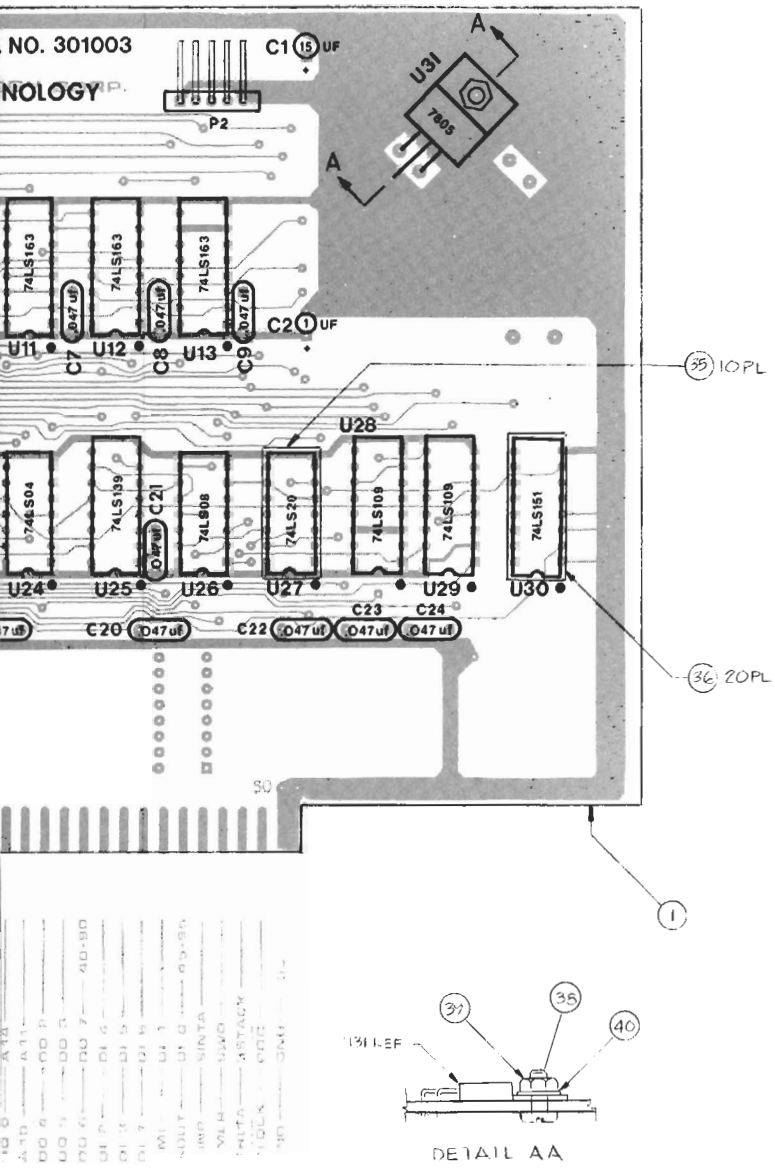
1. ALL HEAVY-THICK DASHED LINES ARE JUMPERS ON THE SOLDER SIDE (FARSIDE) OF THE PCB. ALL HEAVY-THICK SOLID LINES ARE JUMPERS ON THE COMPONENT SIDE (NEARSIDE) OF THE PCB.
2. (NOT USED)
3. MARK LABEL, ITEM (64), WITH REV LETTER AND PLACE IN APPROXIMATE AREA SHOWN.
4. REMOVE PIN 15 FROM HEADER PRIOR TO INSTALLING HEADER ON BOARD.
5. REMOVE PIN 31 FROM HEADER PRIOR TO INSTALLING HEADER ON BOARD.
6. UNLESS OTHERWISE SPECIFIED ALL JUMPER WIRES ARE 24 AWG, ITEM (67)

See Parts List, Section 9, for key to encircled item numbers

2 Helios II

Fig. 8-6 Controller PCB Assembly (C/G)


FORMATTER
REV C PC301004
ASSY. NO. 301003
1977 © 1977 BY PROCESSOR TECHNOLOGY
SER NO.
P3
P1
U1 U2 U3 U4 U5 U6 U7 U8 U9 U10 U11 U12
U14 U15 U16 U17 U18 U19 U20 U21 U22 U23 U24 U25
C3 C4 C5 C6 C7 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20
R1 R2
8 7 6 5
D C B A



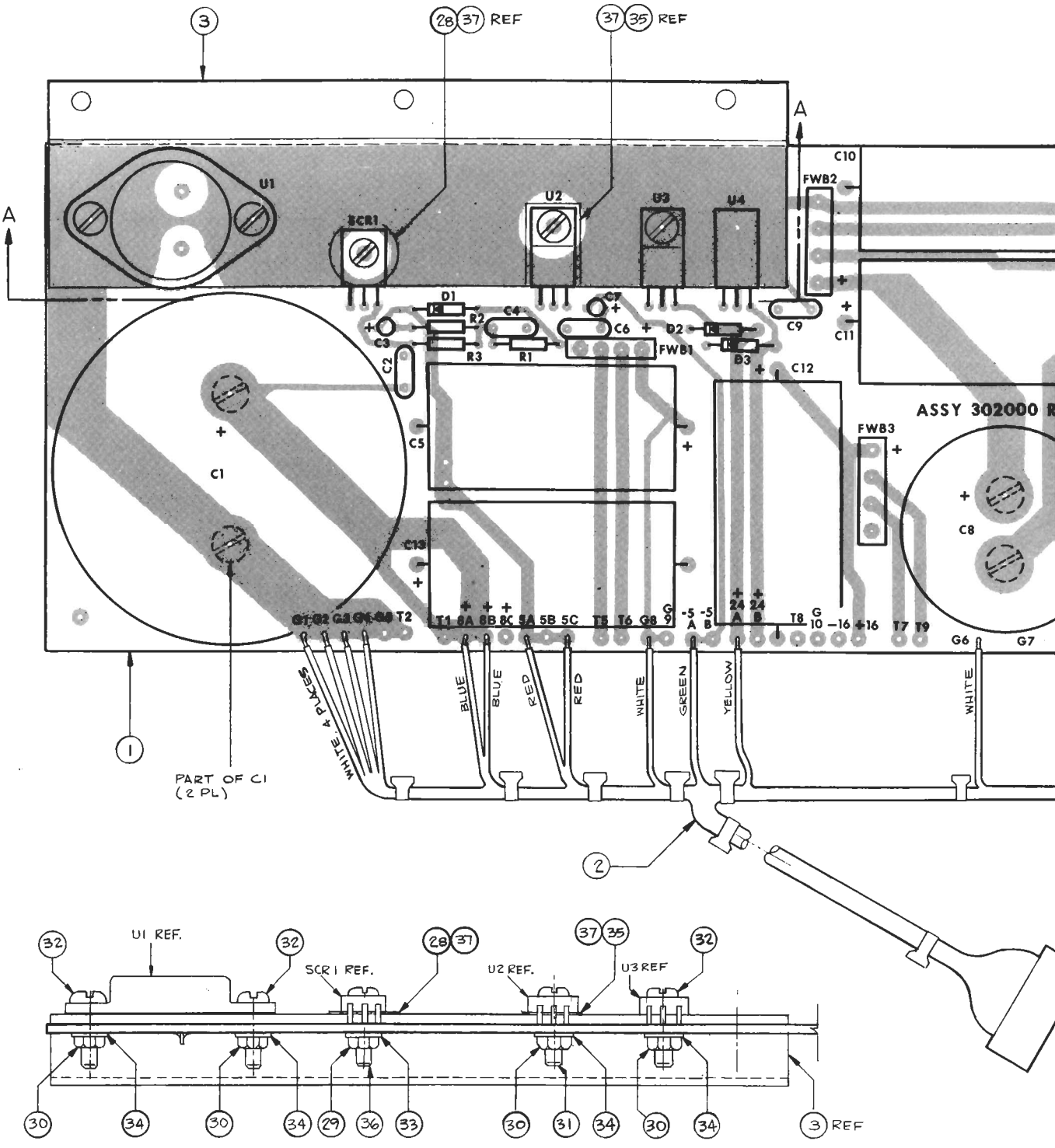
NOTES:

1. REMOVE PIN 1 FROM HEADER PRIOR TO INSTALLING HEADER ON BOARD.

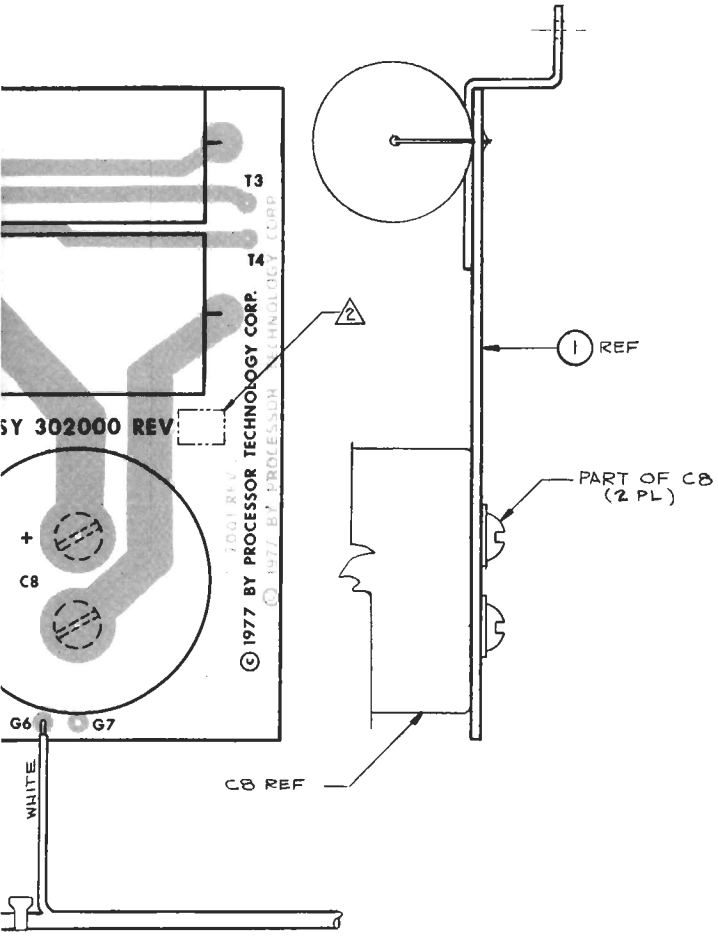
See Parts List, Section 9, for key to encircled item numbers

2 Helios II

Fig. 8-7 Formatter PCB Assembly (C/E)


3
28 37 REF
37 35 REF
A
U1
SCR1
U2
U3
U4
C10
FWB2
C11
C9
D1
R2
C4
C7
C6
D2
C3
R3
R1
FWB1
D3
C2
C12
C5
ASSY 302000
FWB3
C1
C8
C13
T1 6A 6B 6C 5A 5B 5C T5 T6 G8 9 -5 -5 24 24 T8 G 10 -16 +16 T7 T9 G6 G7
WHITE 4 PLACES
BLUE
BLUE
RED
RED
WHITE
GREEN
YELLOW
WHITE
1
PART OF C1 (2 PL)
2
32 U1 REF. 32 SCR1 REF. 28 31 U2 REF. 37 35 U3 REF 32
30 34 30 34 29 36 33 30 31 34 30 34 3 REF

DETAIL A-A



NOTES:

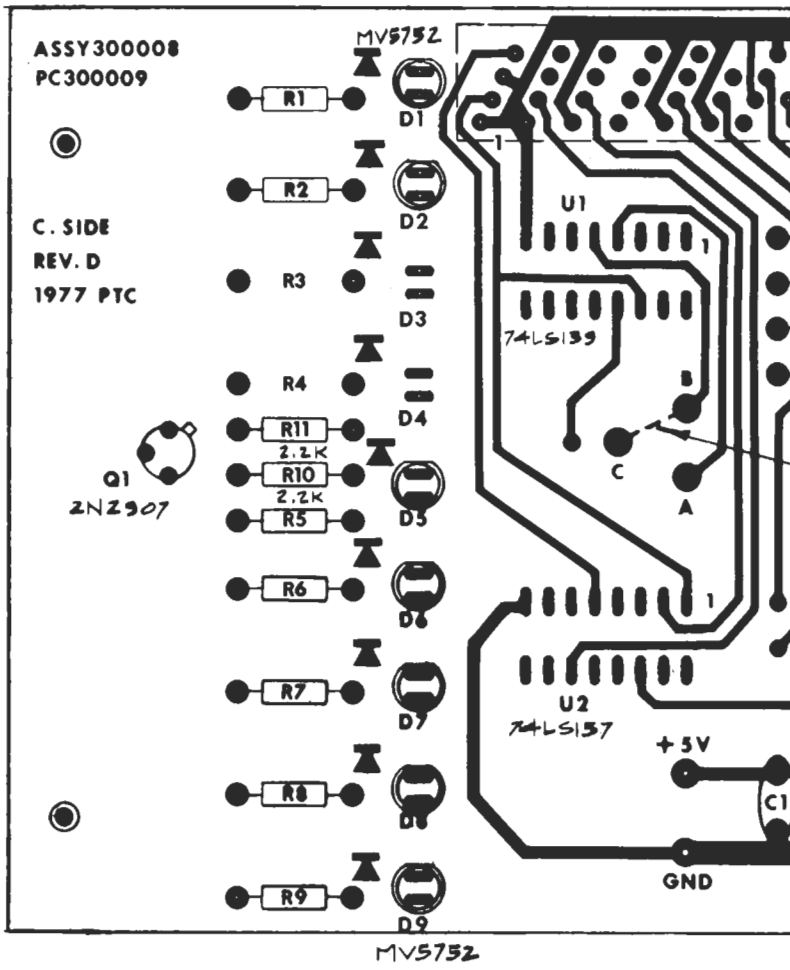
1. THERMAL COMPOUND, ITEM 37, IS TO BE PLACED BETWEEN HEATSINK AND ALL COMPONENTS WHICH ARE MOUNTED TO THE HEATSINK.
2. MARK REV LETTER "D" WITH INDELIBLE INK IN APPROXIMATE AREA SHOWN.

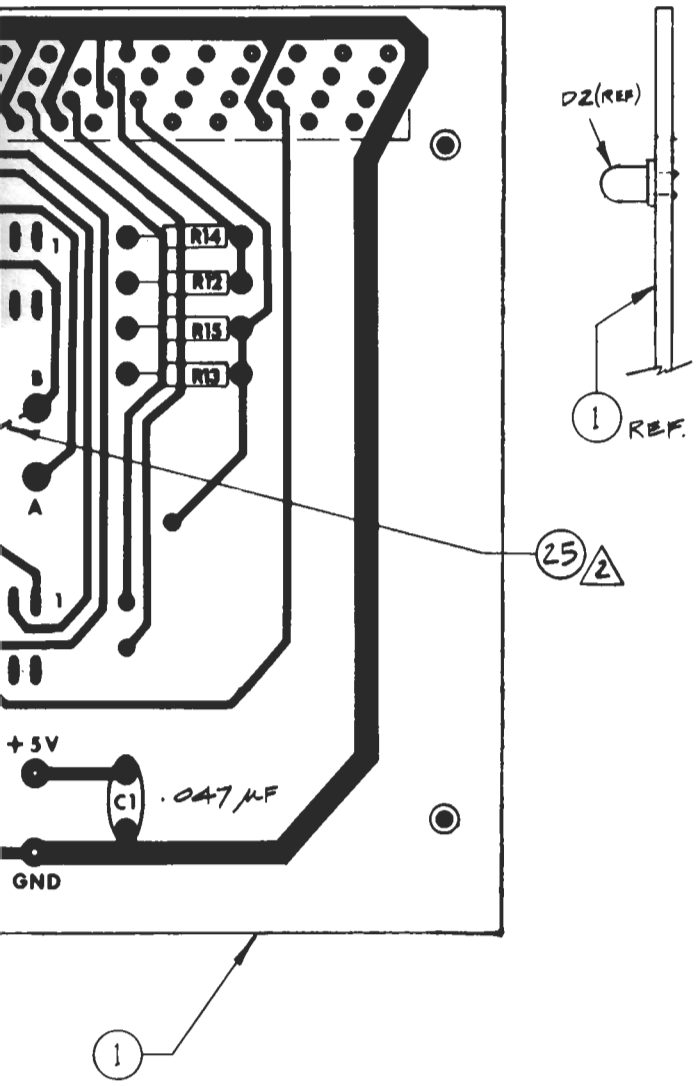
See Parts List, Section 9, for key to encircled item numbers

302000

2 Helios II

Fig. 8-8 Regulator PCB Assembly, Model 2 (C/D)

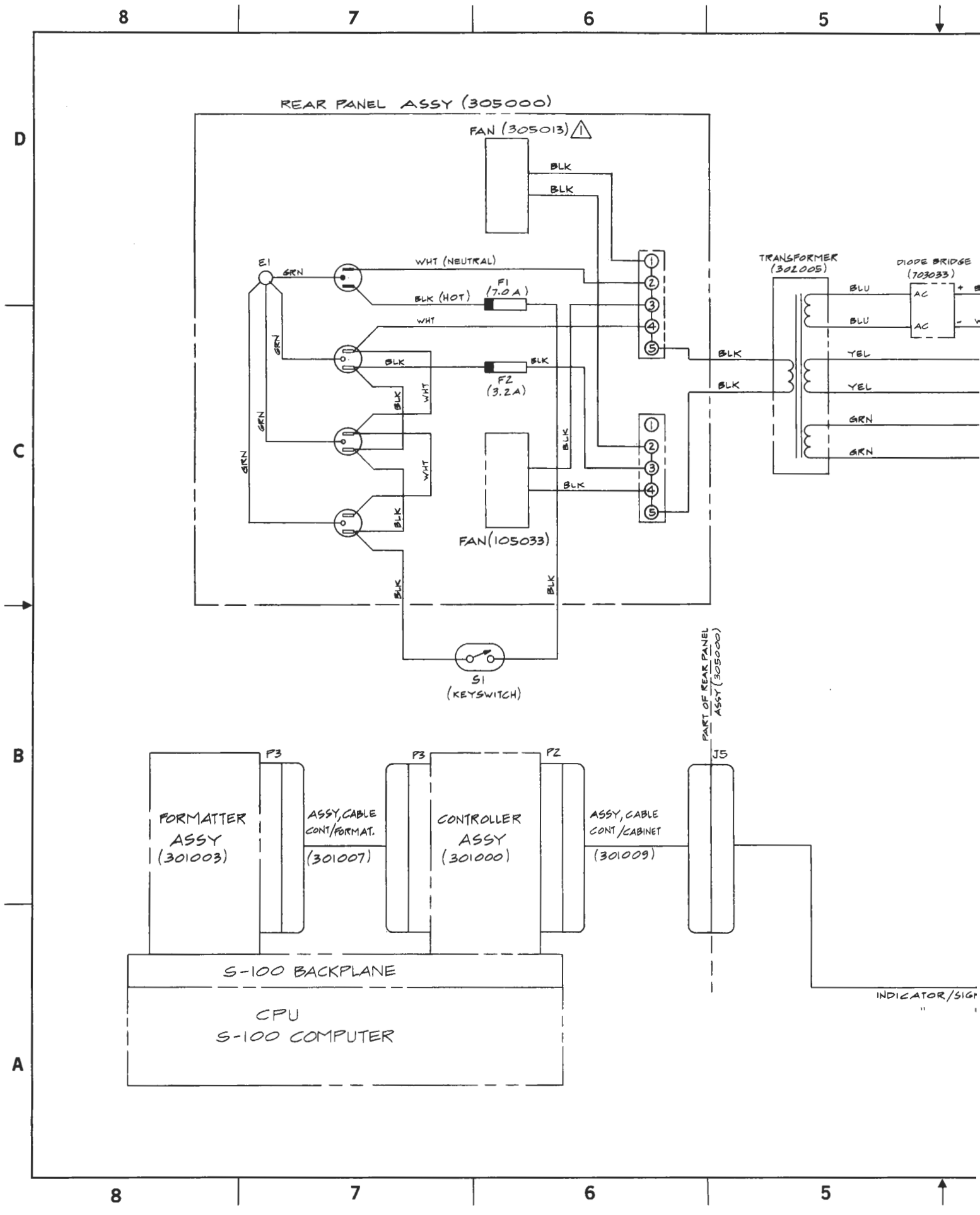

ASSY300008
PC300009
C. SIDE
REV. D
1977 PTC
MV5752
R1
R2
R3
R4
R11
2.2K
R10
2.2K
R5
R6
R7
R8
R9
D1
D2
D3
D4
D5
D6
D7
D8
D9
Q1
2N2907
U1
74LS139
U2
74LS157
C
A
+5V
GND
C1
MV5752



NOTES:
UNLESS OTHERWISE SPECIFIED:
1. RESISTOR VALUES ARE 220 OHMS.
2. SOLDER A #24 SOLID BUS WIRE JUMPER BETWEEN B & C ON THE FARSIDE (SOLDER SIDE) OF PCB.

See Parts List, Section 9, for key to encircled item numbers

Fig. 8-9 Indicator Panel PCB Assembly (300008 D/F)


REAR PANEL ASSY (305000)
FAN (305013)
BLK
BLK
E1
GRN
WHT (NEUTRAL)
F1
(7.0 A)
BLK (HOT)
WHT
GRN
BLK
BLK
FZ
(3.2A)
BLK
WHT
GRN
GRN
WHT
BLK
BLK
FAN(105033)
BLK
BLK
S1
(KEYSWITCH)
TRANSFORMER
(302005)
DIODE BRIDGE
(703033)
BLU
BLU
AC
AC
YEL
YEL
GRN
GRN
BLK
BLK
PART OF REAR PANEL ASSY (305000)
J5
P3
P3
P2
FORMATTER
ASSY
(301003)
ASSY, CABLE
CONT/FORMAT.
(301007)
CONTROLLER
ASSY
(301000)
ASSY, CABLE
CONT/CABINET
(301009)
S-100 BACKPLANE
CPU
S-100 COMPUTER
INDICATOR/SIGN

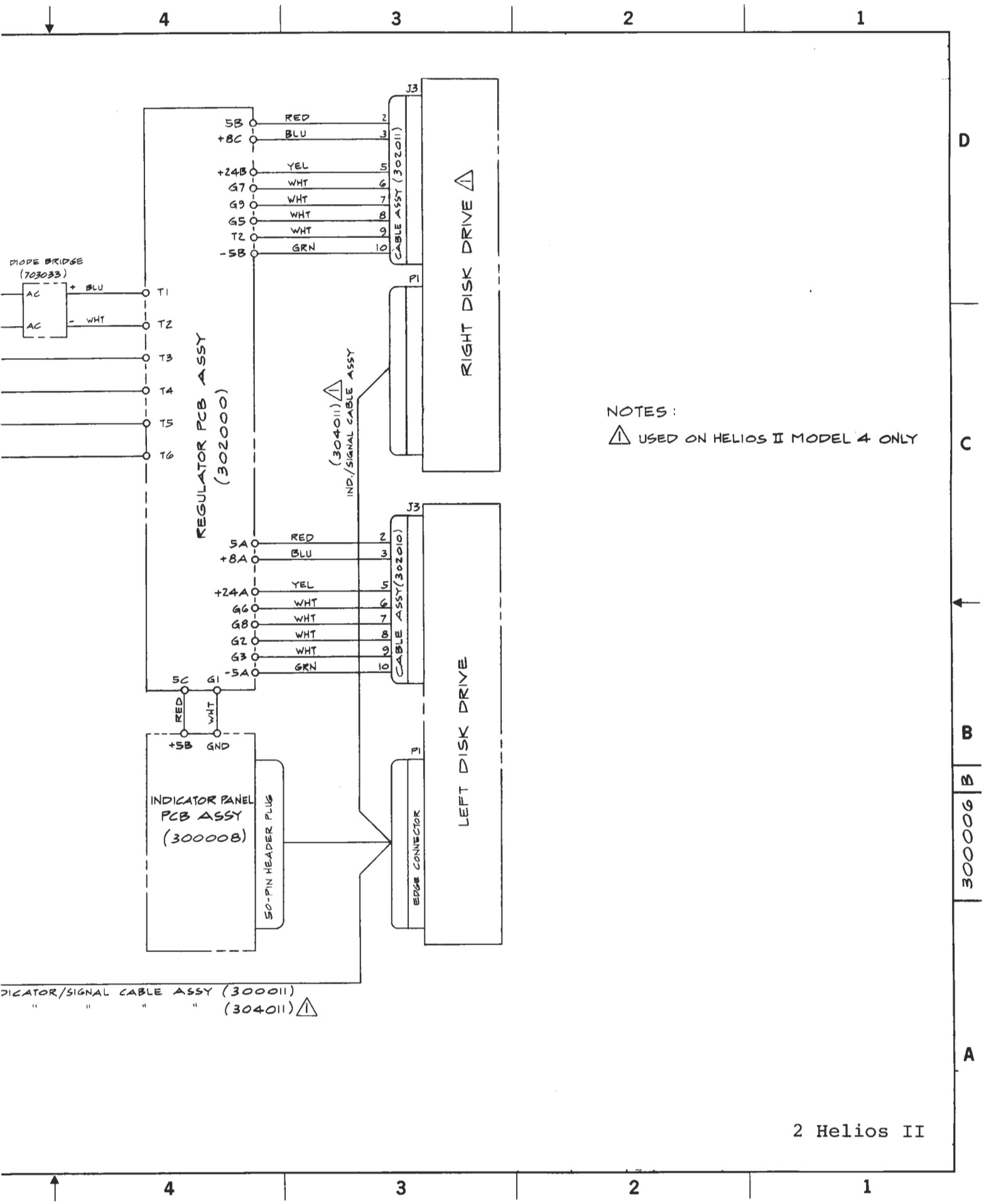
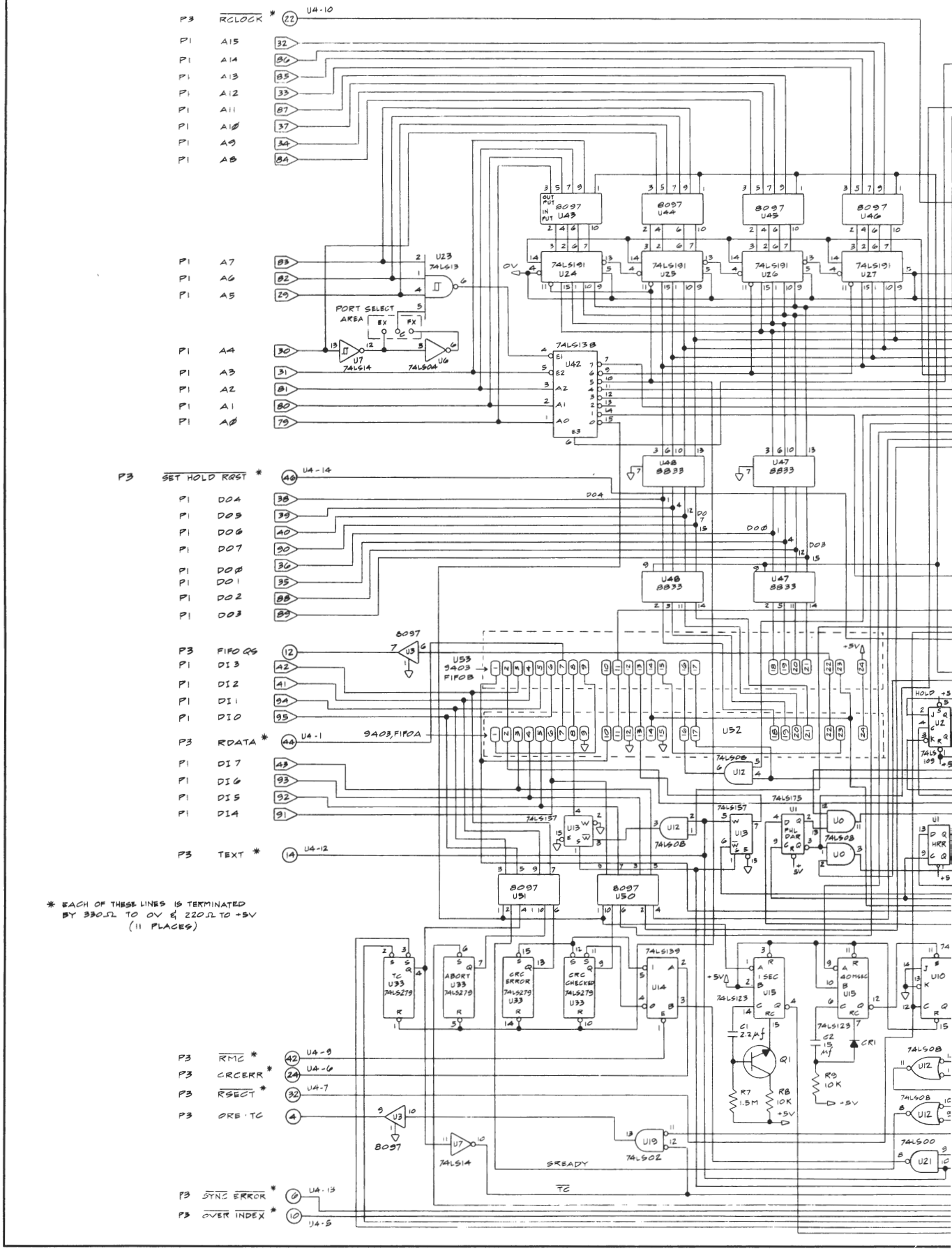


Fig. 8-10 System Wiring Diagram


P3 RCLOCK * 22 U4-10
P1 A15 32
P1 A14 31
P1 A13 35
P1 A12 33
P1 A11 37
P1 A10 37
P1 A9 34
P1 A8 34
P1 A7 83
P1 A6 82
P1 A5 29
P1 A4 30
P1 A3 31
P1 A2 81
P1 A1 80
P1 A0 79
PORT SELECT AREA
EX
FX
U23 74LS13
U7 74LS14
74LS04 U6
74LS138 U42
8097 U43
8097 U44
8097 U45
8097 U46
74LS191 U24
74LS191 U25
74LS191 U26
74LS191 U27
0V
P3 SET HOLD RQST * 46 U4-14
P1 D04 38
P1 D05 39
P1 D06 40
P1 D07 30
P1 D00 36
P1 D01 35
P1 D02 88
P1 D03 89
8BB33 U48
8BB33 U47
P3 FIFO QS 12
P1 DI3 42
P1 DI2 41
P1 DI1 94
P1 DI0 95
P3 RDATA * 44 U4-1
P1 DI7 43
P1 DI6 93
P1 DI5 92
P1 DI4 91
P3 TEXT * 14 U4-12
8097 U3
U53 9403 FIFOB
9403,FIFOA
U52
74LS08 U12
74LS157 U13
74LS175 U1
74LS08 U0
8097 U51
8097 U50
* EACH OF THESE LINES IS TERMINATED BY 330Ω TO 0V & 220Ω TO +5V (11 PLACES)
TC U33 74LS279
ABORT U33 74LS279
CRC ERROR U33 74LS279
CRC CHECKED U33 74LS279
74LS139 U14
1 SEC U15
40MSEC U15
74LS123
C1 .22μf
C2 15 μf
CR1
Q1
R7 1.5M
R8 10K
R9 10K
+5V
P3 RMC * 42 U4-9
P3 CRCERR * 24 U4-6
P3 RSECT * 32 U4-7
P3 ORB·TC 4
8097 U3
74LS14 U7
74LS02 U19
SREADY
TC
74LS08 U10
74LS08 U12
74LS00 U21
P3 SYNC ERROR * 9 U4-13
P3 OVER INDEX * 10 U4-5

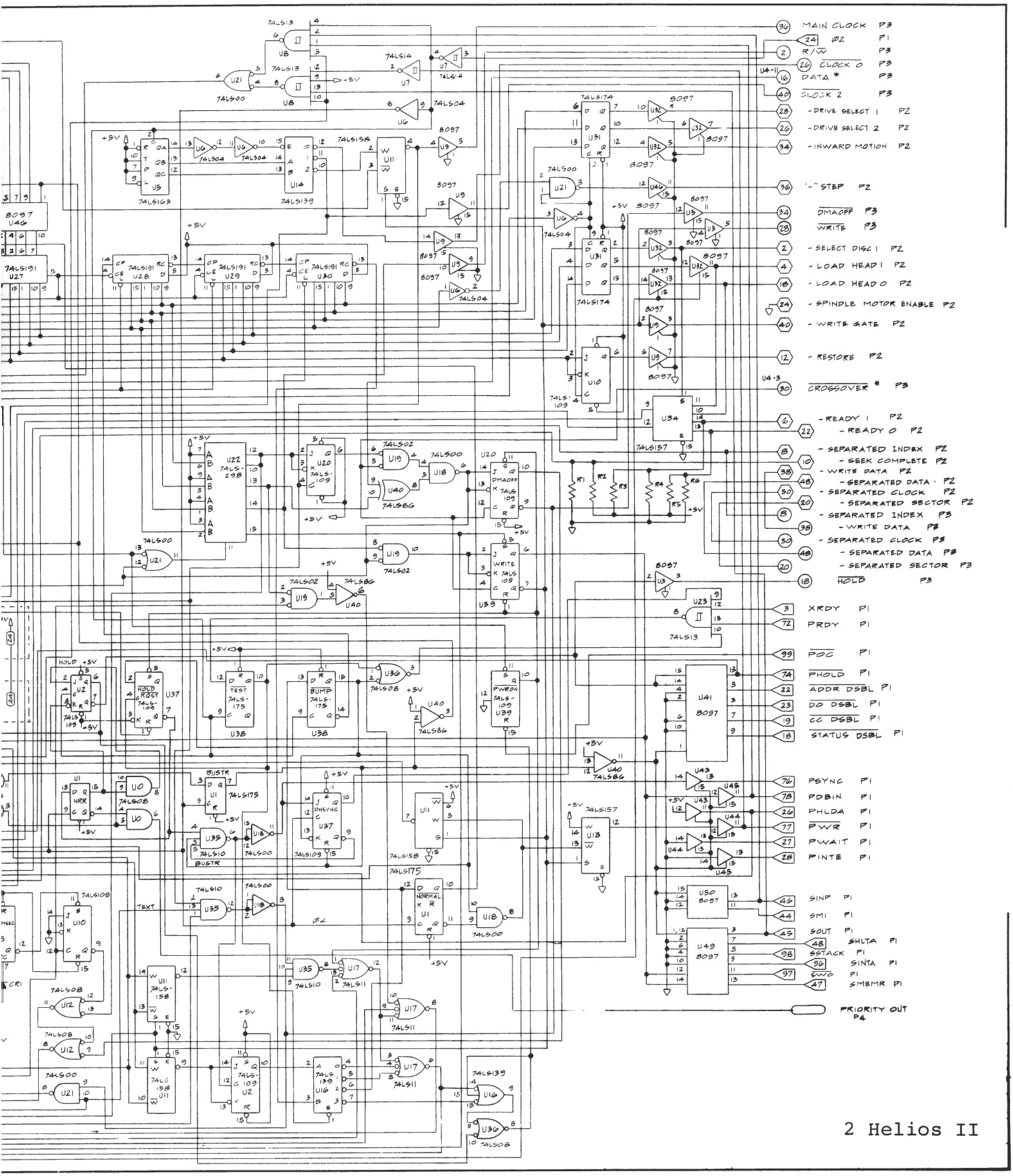
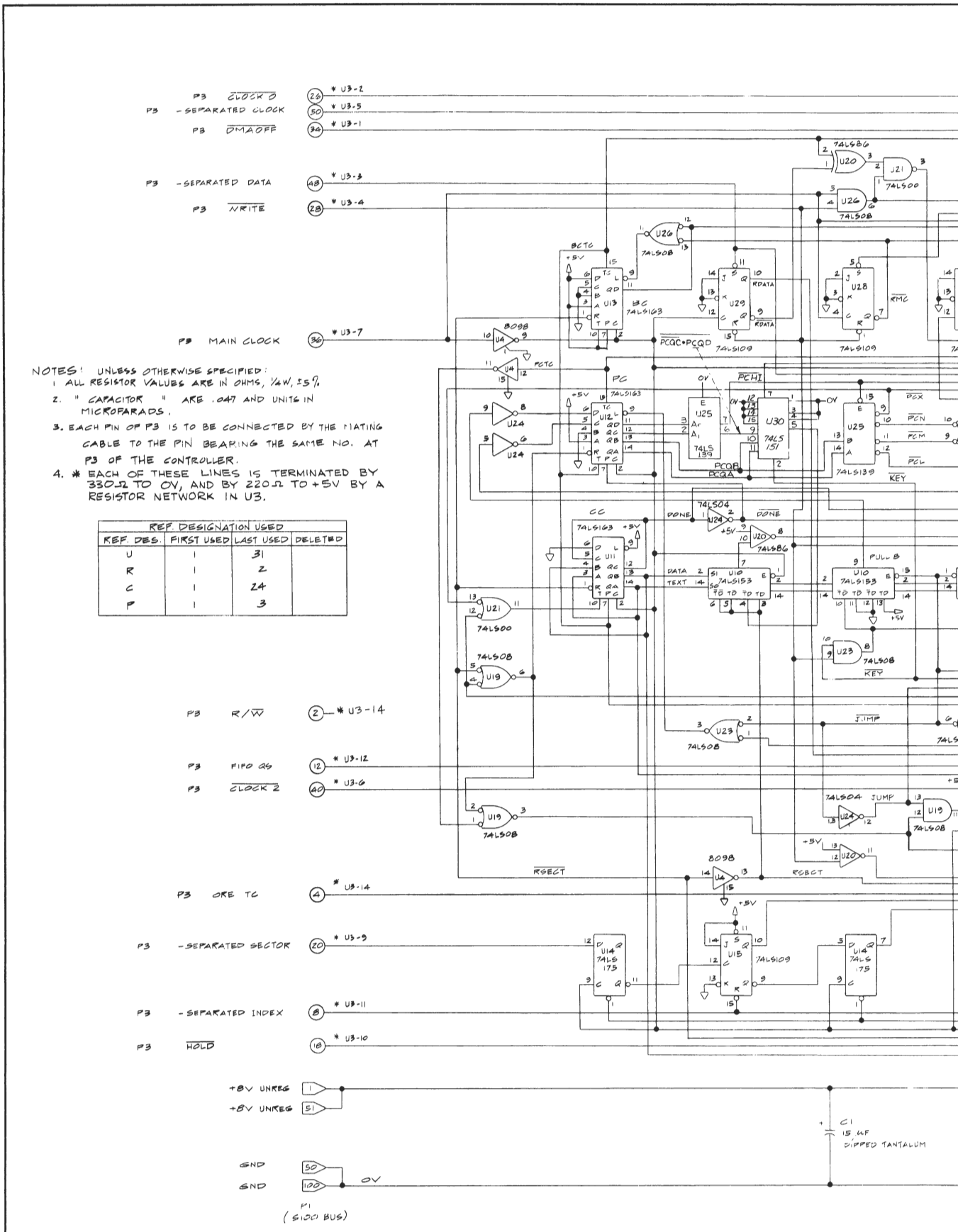


Fig. 8-11 Controller PCB, Schematic (301002E)

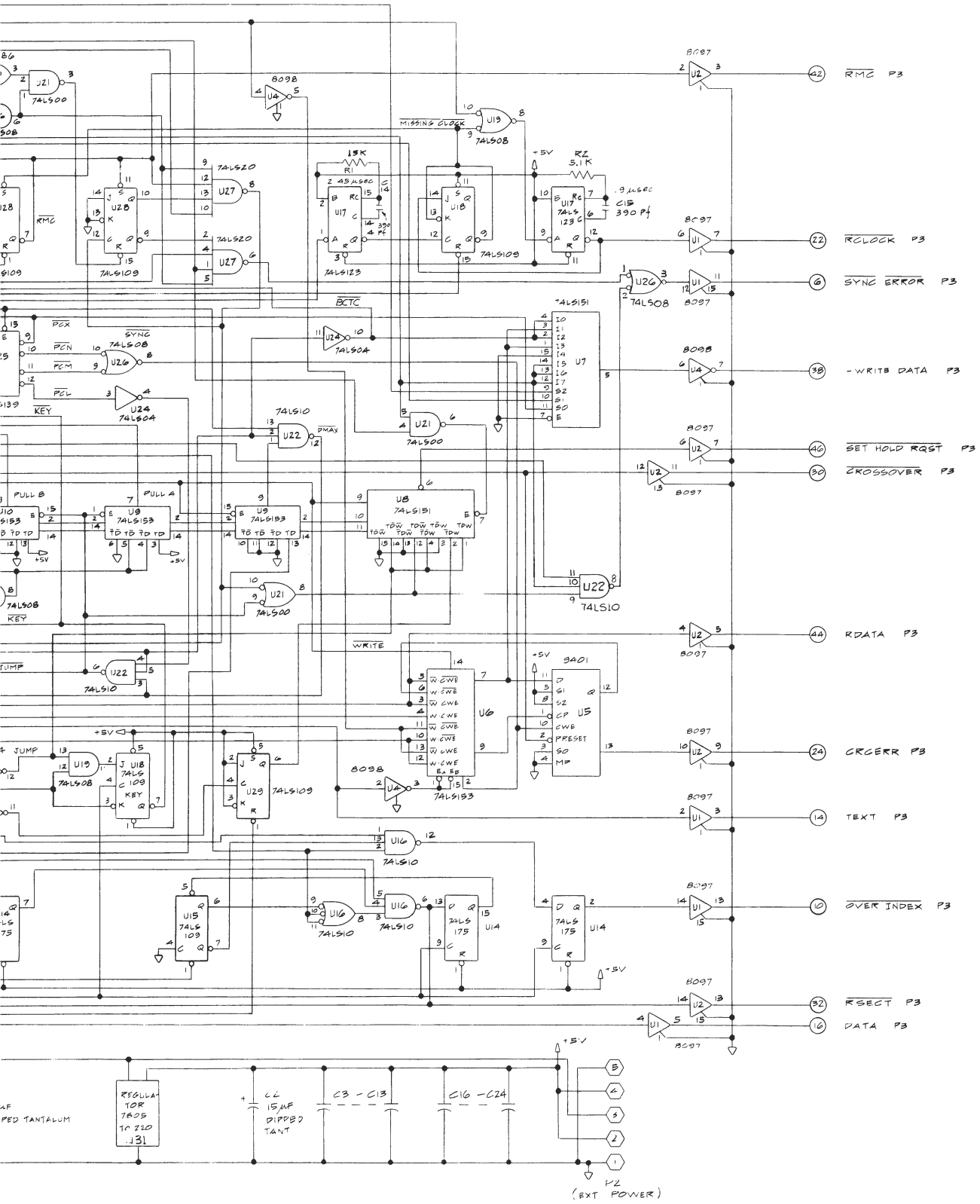


NOTES: UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%.
2. " CAPACITOR " ARE .047 AND UNITS IN MICROFARADS.
3. EACH PIN OF P3 IS TO BE CONNECTED BY THE MATING CABLE TO THE PIN BEARING THE SAME NO. AT P3 OF THE CONTROLLER.
4. * EACH OF THESE LINES IS TERMINATED BY 330Ω TO 0V, AND BY 220Ω TO +5V BY A RESISTOR NETWORK IN U3.

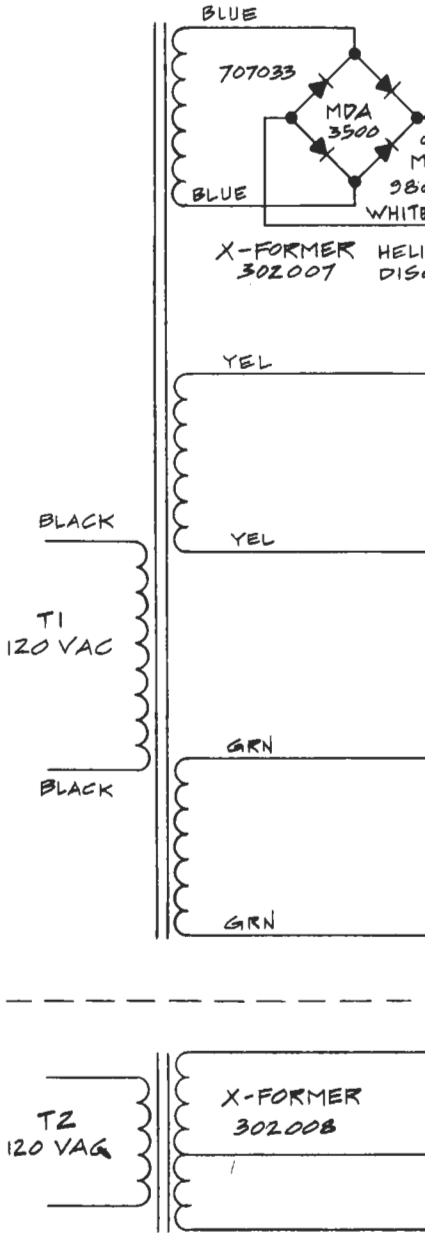
REF. DESIGNATION USED

REF. DES.	FIRST USED	LAST USED	DELETED
U	1	31	
R	1	2	
C	1	24	
P	1	3	



2 Helios II

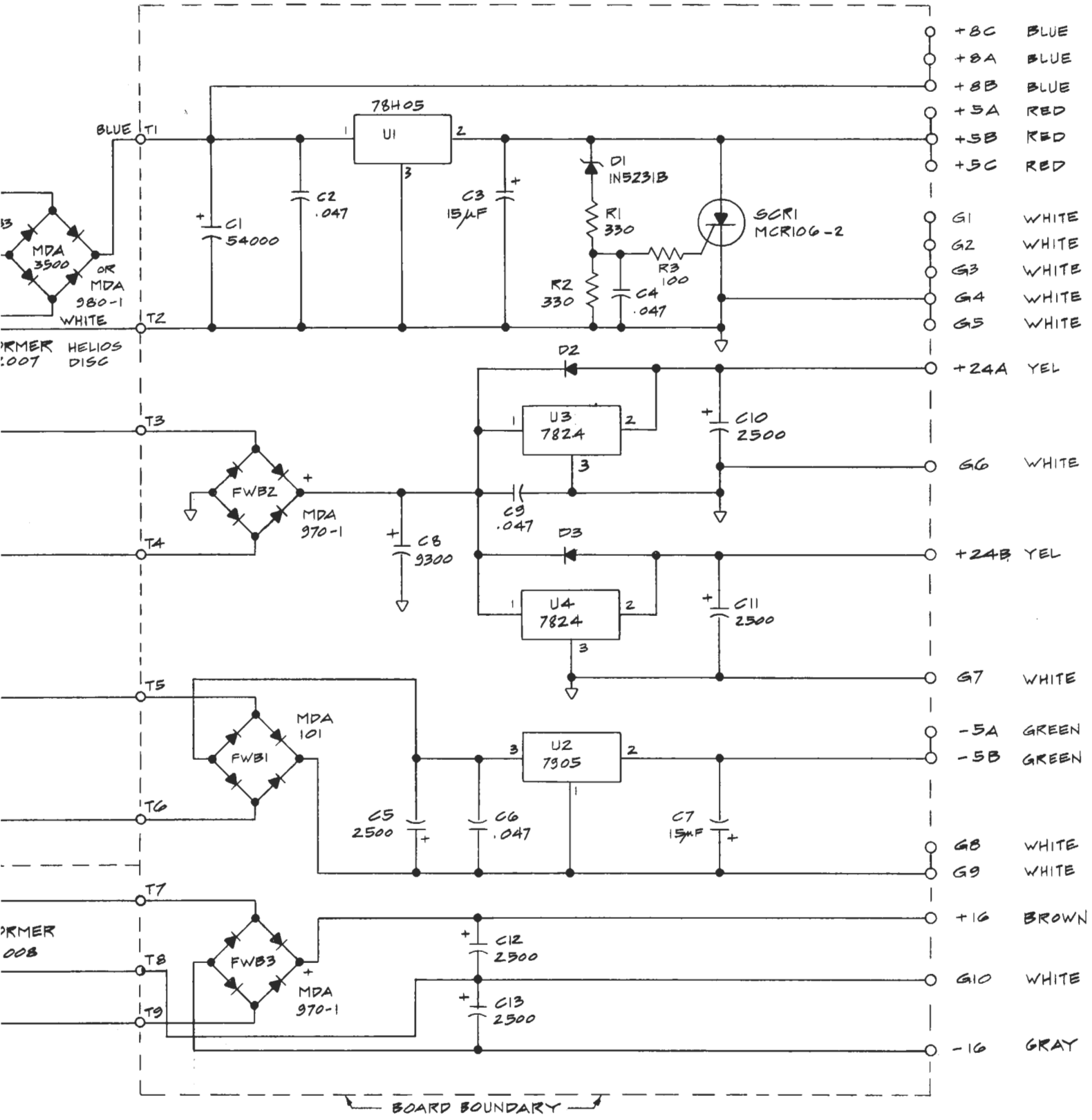
Fig. 8-12 Formatter PCB, Schematic (301005D)



NOTES:

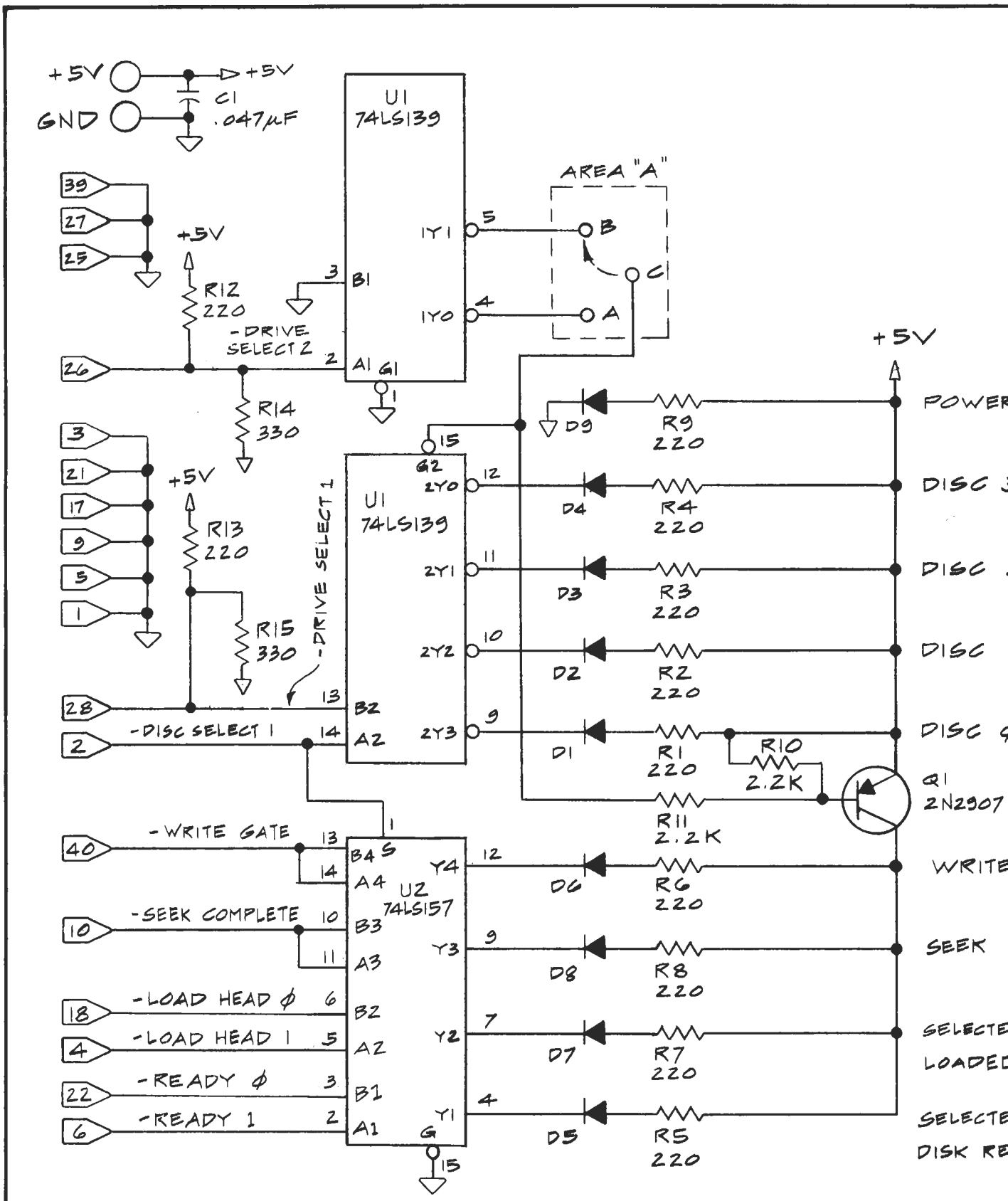
1. UNLESS OTHERWISE SPECIFIED

   A. ALL RESISTOR VALUES ARE G
   B. ALL CAPACITOR VALUES ARE



FIED
IES ARE GIVEN IN OHMS (Ω)
LUES ARE GIVEN IN MICROFARADS (µF)

Fig. 8-13 Regulator PCB, Schematic (302002A)


+5V
GND
C1
.047µF
+5V
U1
74LS139
AREA "A"
39
27
25
+5V
R12
220
-DRIVE SELECT 2
26
R14
330
3
21
17
9
5
1
+5V
R13
220
R15
330
-DRIVE SELECT 1
28
2
-DISC SELECT 1
U1
74LS139
1Y1
1Y0
B1
A1
G1
2Y0
2Y1
2Y2
2Y3
G2
B2
A2
D9
D4
D3
D2
D1
R9
220
R4
220
R3
220
R2
220
R1
220
R10
2.2K
R11
2.2K
Q1
2N2907
+5V
POWER
DISC
DISC
DISC
DISC
40
-WRITE GATE
10
-SEEK COMPLETE
18
-LOAD HEAD ϕ
4
-LOAD HEAD 1
22
-READY ϕ
6
-READY 1
U2
74LS157
B4
A4
B3
A3
B2
A2
B1
A1
S
G
Y4
Y3
Y2
Y1
D6
D8
D7
D5
R6
220
R8
220
R7
220
R5
220
WRITE
SEEK
SELECTE
LOADED
SELECTE
DISK RE

5V

POWER ON

DISC 3 SELECTED

DISC 2 SELECTED

DISC 1 SELECTED

DISC Ø SELECTED

Q1
2N2907

WRITE

SEEK COMPLETE

SELECTED HD.
LOADED

SELECTED
DISK READY

NOTES:

A. UNLESS OTHERWISE SPECIFIED
   1. ALL DIODES ARE LED, MV5752, RED
   2. ALL RESISTOR VALUES IN OHMS, 1/4 W, 5 %
   3. ALL CAPACITOR VALUES IN MICROFARADS

B. I.C. PWR & GND PIN CONNECTION

REF DES.	IC NO.	PIN NO +5V	PIN. NO. GND
U1	74LS139	16	8
U2	74LS157	16	8

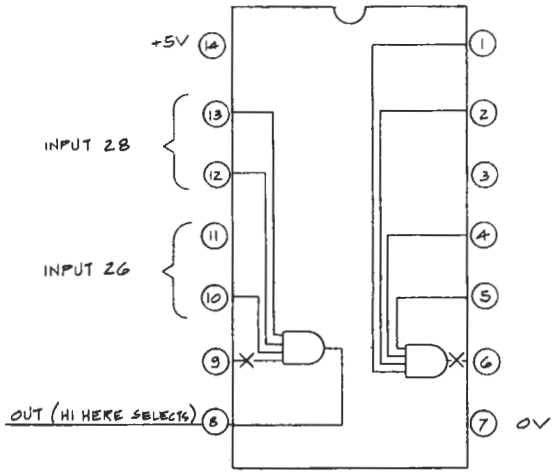
C. COMPONENT REF. DESIGNATION

LAST USED	DELETED
U2	
Q1	
D9	D3 & D4 ON SINGLE DRIVE (-01 & -02) ONLY
R15	R3 & R4 " " " " "
C1	

D. JUMPER B TO C FOR SINGLE OR #1 HELIOS CABINET
   JUMPER A TO C FOR 2ND HELIOS CABINET

Fig. 8-14 Indicator Panel PCB, Schematic (300007E)

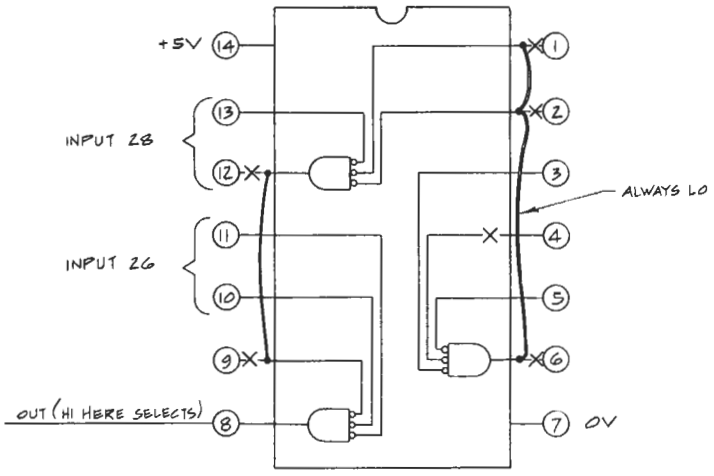
A DUAL FLOPPY DISC DRIVE CONTAINING THIS SELECTOR
IN U11 WILL RESPOND AS UNITS 0 & 1



TO MAKE THIS DEVICE
1. GET A 74LS21
2. CUT OFF PINS 6, 9
3. REMOVE PREVIOUS NOMENCLATURE
4. MARK WITH PT PART NUMBER AND "0-1"

INPUT 2B	INPUT 2G	OUT
LO	LO	LO
LO	HI	LO
HI	LO	LO
HI	HI	[HI]

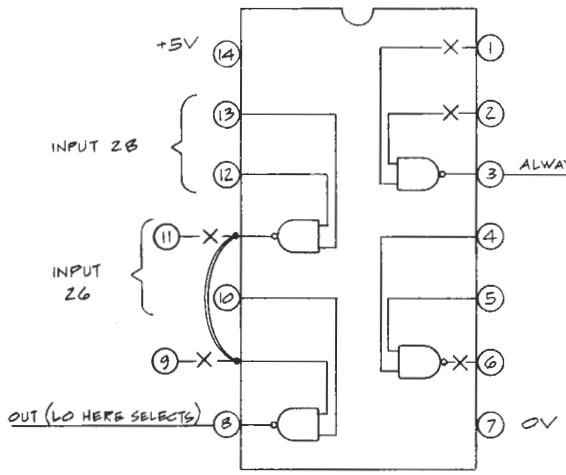
A DUAL FLOPPY DISC DRIVE CONTAINING THIS SELECTOR
IN U11 WILL RESPOND AS UNITS 4 & 5



TO MAKE THIS DEVICE
1. GET A 74LS27
2. CUT OFF PIN 4
3. BEND UP PINS 1, 2, 6 & CONNECT THEM TO
4. BEND UP PINS 9, 12 & CONNECT THEM TOGET
5. REMOVE PREVIOUS NOMENCLATURE
6. MARK WITH PT PART NUMBER AN

INPUT 2B	INPUT 2G	OUT
LO	LO	LO
LO	HI	LO
HI	LO	[HI]
HI	HI	LO

A DUAL FLOPPY DISC DRIVE CONTAINING THIS SELECTOR IN U11 WILL RESPOND AS UNITS 2 & 3

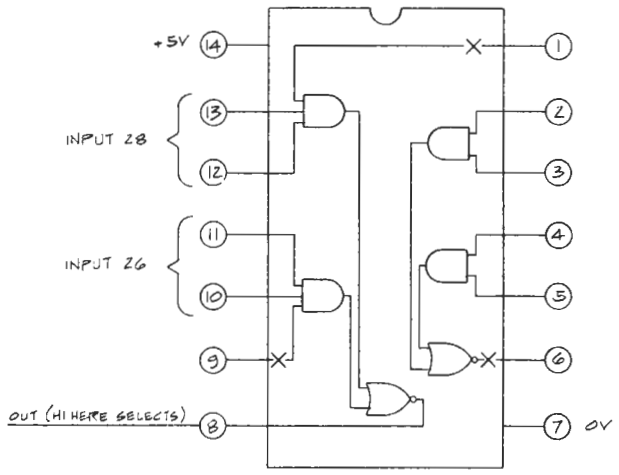


TO MAKE THIS DEVICE
1. GET A 74LS37
2. CUT OFF PINS 1, 2, 6
3. BEND UP PINS 9, 11 & CONNECT THEM TOGETHER
4. REMOVE PREVIOUS NOMENCLATURE
5. MARK WITH PT PART NUMBER AND "2-3"

AND "0-1"

INPUT 2B	INPUT 2G	OUT
LO	LO	HI
LO	HI	[LO]
HI	LO	HI
HI	HI	HI

A DUAL FLOPPY DISC DRIVE CONTAINING THIS SELECTOR IN U11 WILL RESPOND AS UNITS 6 & 7



TO MAKE THIS DEVICE
1. GET A 74LS51
2. CUT OFF PINS 1, 6, 9
3. REMOVE PREVIOUS NOMENCLATURE
4. MARK WITH PT PART NUMBER AND "6-7"

CONNECT THEM TOGETHER
ECT THEM TOGETHER
NCLATURE
BER AND "4-5"

INPUT 2B	INPUT 2G	OUT
LO	LO	[HI]
LO	HI	LO
HI	LO	LO
HI	HI	LO

Fig. 8-15 Selector DIPSs, Schematic Assemblies, (30015-18B)

Table 8-1 Numerical Pin-to-Pin Assignments, Controller P3/Formatter P3 (Cable Assy. 301007, Model 2 and 4)
Note: All odd numbered pins are ground.

PIN #	SIGNAL NAME
2	R/$\overline{W}$
4	ORE·TC
6	$\overline{\text{SYNC ERROR}}$
8	-SEPARATED INDEX
10	$\overline{\text{OVER INDEX}}$
12	FIFO QS
14	TEXT
16	DATA
18	$\overline{\text{HOLD}}$
20	-SEPARATED SECTOR
22	$\overline{\text{RCLOCK}}$
24	CRCERR
26	$\overline{\text{CLOCK Ø}}$
28	$\overline{\text{WRITE}}$
30	$\overline{\text{CROSSOVER}}$
32	$\overline{\text{RSECT}}$
34	$\overline{\text{DMAOFF}}$
36	MAIN CLOCK
38	-WRITE DATA
40	$\overline{\text{CLOCK 2}}$
42	$\overline{\text{RMC}}$
44	RDATA
46	$\overline{\text{SET HOLD RQST}}$
48	-SEPARATED DATA
50	-SEPARATED CLOCK

Table 8-2 Numerical Pin-to-Pin Assignments, Controller/Drive/Indicator Panel
(Cable Assys. 301009 and 300011, Model 2)
Note: All odd numbered pins are ground.

PIN #	SIGNAL	CON-TROLLER P2	DRIVE P1	IND CAT PAN
2	-DISK SELECT 1	X	X	X
4	-LOAD HEAD 1	X	X	X
6	-READY 1	X	X	X
8	-SEPARATED INDEX	X	X	-
10	-SEEK COMPLETE	X	X	X
12	-RESTORE	X	X	-
18	-LOAD HEAD Ø	X	X	X
20	-SEPARATED SECTOR	X	X	-
22	-READY Ø	X	X	X
24	-SPINDLE MOTOR ENABLE	X	X	-
26	-DRIVE SELECT 2	X	X	X
28	-DRIVE SELECT 1	X	X	X
34	-INWARD MOTION	X	X	-
36	-STEP	X	X	-
38	-WRITE DATA	X	X	-
40	-WRITE GATE	X	X	X
48	-SEPARATED DATA	X	X	-
50	-SEPARATED CLOCK	X	X	-

*NOTES

1. See Table 8-1, 8-2 and 7-7 for numerical pin-to-pin assignments.
2. Among the controller, formatter, drive, and indicator panel, all odd numbered pins ar ground. Some indicator panel pins are grounded by the interconnect cable to control ground.
3. For system wiring see Fig. 8-10, System Wiring Diagram.
4. Signals among the controller, formatter, drive and indicator panel are unidirectional
5. Only those signal/pins on the CPU which are used by the controller are listed on this drawing.
6. P1 and P2 on the formatter are alternative DC power sources. (See Section 3, Unpacking and Assembly Tips.)

signments,

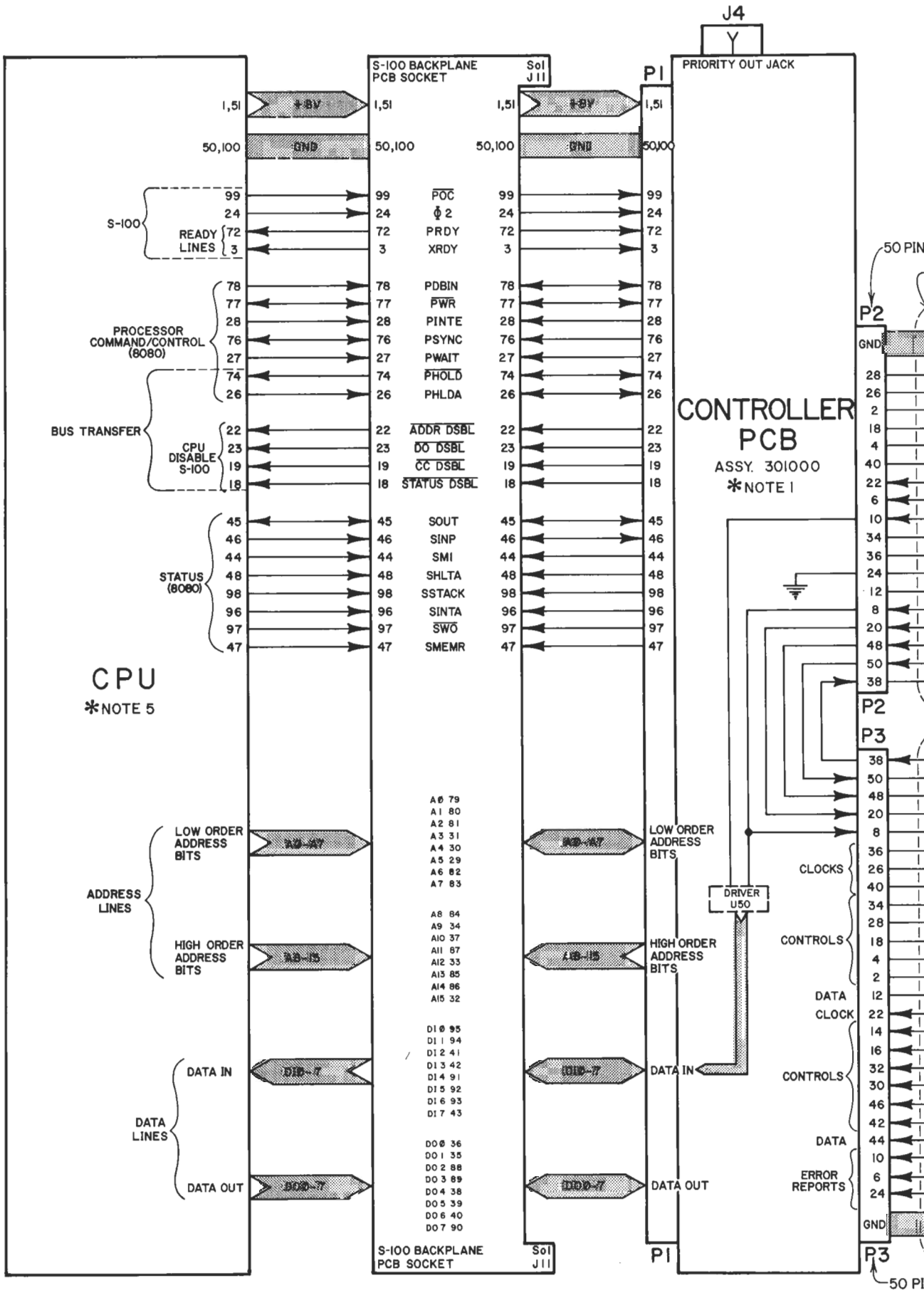
Model 2)
round.

DRIVE P1	INDICATOR PANEL
X	X
X	X
X	X
X	—
X	X
X	—
X	X
X	—
X	X
X	—
X	X
X	X
X	—
X	—
X	—
X	X
X	—
X	—

ed pins are
o controller

lirectional.
ed on this

3, Unpack-



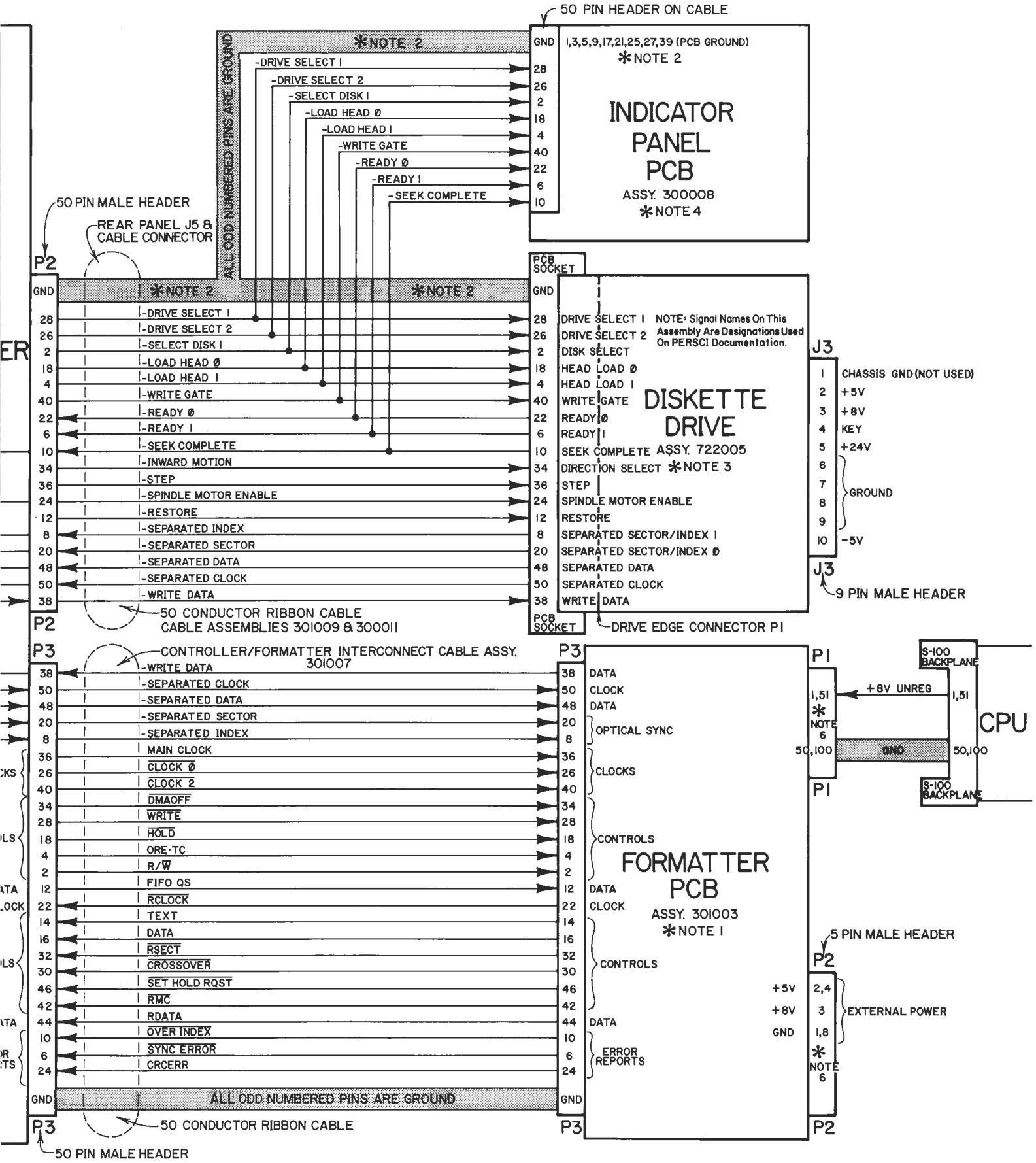


Fig. 8-16 Pin-to-Pin Signal Flow Diagram (I-2-78)

Table 8-3 Key to System Functional Block Diagram

(The encircled key numbers refer to matching numbers on Fig. 8-17, System Block Diagram.)

CONTROLLER PCB

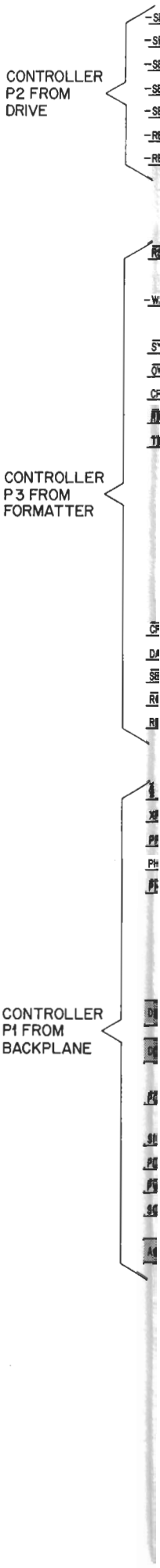
(Refer to Fig. 8-11, Controller PCB Schematic.)

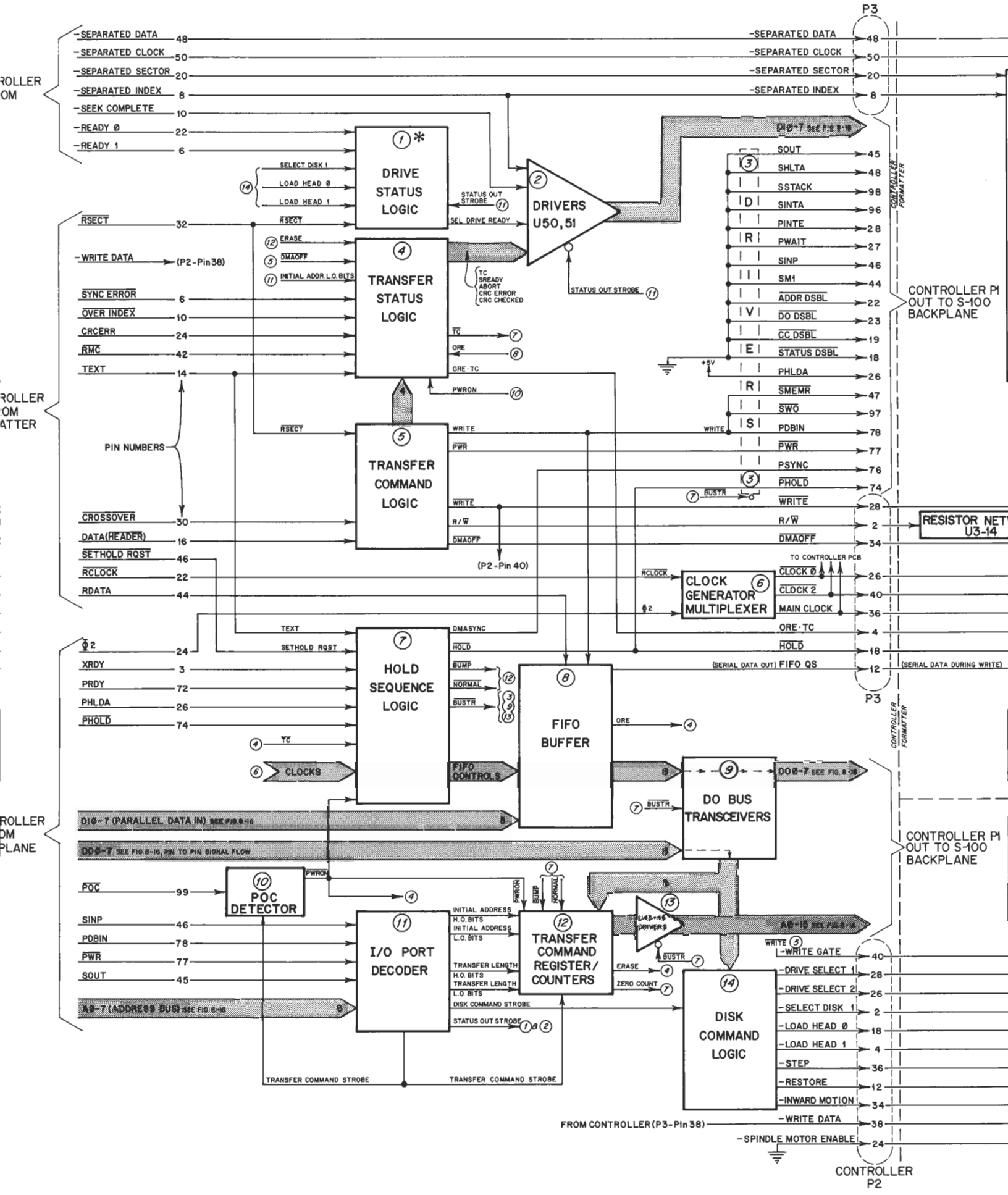
KEY #	NAME OF FUNCTIONAL BLOCK	ICs REPRESENTED
(1)	Drive Status Logic	U10-9,U12-8,11,U15,U34
(2)	S-100 Tri-state Bus Drivers	U50,U51
(3)	S-100 Tri-state Bus Drivers	U41,U43,U44,U45,U49,U50
(4)	Transfer Status Logic	U14,U19,U21,U33
(5)	Transfer Command Logic	U13,U18-6,U19-1,4,10,U20, U21-11,U39-3,U40-8
(6)	Clock Generator/Multiplexer	U5,U6,U7,U11,U14
(7)	Hold Sequence Logic	UØ,U1,U2,U3,U11,U12,U13,U16, U17,U18,U23,U35,U36,U37, U38,U40; Abort Logic: U35-8,12,U17-8, 12,U18-3
(8)	FIFO Buffer	U52,U53
(9)	DO Bus Transceivers	U47,U48
(10)	PWR ON Detector/Clear Generator	U39
(11)	I/O Port Decoder	U6,U7,U8,U21,U23,U42
(12)	Transfer Command Register/Counters	U22,U24 through U30
(13)	S-100 Tri-state Address Bus Drivers	U41,U43 through U46,U49,U50
(14)	Disk Command Logic	U10-6,U21-3,U31

FORMATTER PCB

(Refer to Fig. 8-12, Formatter PCB Schematic.)

KEY #	NAME OF FUNCTIONAL BLOCK	ICs REPRESENTED
(15)	Sector/Index Logic	U14,U15,U16
(16)	Clock Detector/Conditioner	U17,U18,U19,U28
(17)	Read Data Conditioner	U29
(18)	Sync Detector	U20,U21,U22,U26,U27,U28
(19)	State Counter Logic	(Refer to Fig. 7-4.)
(20)	Write Multiplexer	U7
(21)	CRC Generator/Detector	U4,U5,U6
(22)	Indicator Panel PCB	(Refer to Fig. 8-14, Indicator Panel PCB, Schematic.)
(23)	Diskette Drive Assembly	(Refer to schematics in the Helios II Service Manual.)




-SEPARATED DATA 48
-SEPARATED CLOCK 50
-SEPARATED SECTOR 20
-SEPARATED INDEX 8
-SEEK COMPLETE 10
-READY Ø 22
-READY 1 6
RSECT 32
-WRITE DATA (P2-Pin38)
SYNC ERROR 6
OVER INDEX 10
CRCERR 24
RMC 42
TEXT 14
PIN NUMBERS
CROSSOVER 30
DATA(HEADER) 16
SETHOLD RQST 46
RCLOCK 22
RDATA 44
Ø2 24
XRDY 3
PRDY 72
PHLDA 26
PHOLD 74
POC 99
SINP 46
PDBIN 78
PWR 77
SOUT 45
A0-7 (ADDRESS BUS) SEE FIG. 8-16
DI0-7 (PARALLEL DATA IN) SEE FIG. 8-16
DO0-7 SEE FIG. 8-16, PIN TO PIN SIGNAL FLOW
1 * DRIVE STATUS LOGIC
SELECT DISK 1
LOAD HEAD Ø
LOAD HEAD 1
STATUS OUT STROBE 11
SEL DRIVE READY
RSECT
2 DRIVERS U50,51
4 TRANSFER STATUS LOGIC
ERASE 12
DMAOFF 5
INITIAL ADDR L.O. BITS 11
TC
SREADY
ABORT
CRC ERROR
CRC CHECKED
STATUS OUT STROBE 11
TC 7
ORE 8
ORE·TC
PWRON 10
5 TRANSFER COMMAND LOGIC
RSECT
WRITE
PWR
WRITE
R/W
DMAOFF
(P2-Pin 40)
6 CLOCK GENERATOR MULTIPLEXER
RCLOCK
Ø2
7 HOLD SEQUENCE LOGIC
TEXT
SETHOLD RQST
XRDY
PRDY
PHLDA
PHOLD
TC 4
6 CLOCKS
DMASYNC
HOLD
BUMP 12
NORMAL
BUSTR 3 9 13
FIFO CONTROLS
8 FIFO BUFFER
ORE 4
9 DO BUS TRANSCEIVERS
BUSTR 7
10 POC DETECTOR
PWRON
11 I/O PORT DECODER
INITIAL ADDRESS H.O. BITS
INITIAL ADDRESS L.O. BITS
TRANSFER LENGTH H.O. BITS
TRANSFER LENGTH L.O. BITS
DISK COMMAND STROBE
STATUS OUT STROBE 1 & 2
12 TRANSFER COMMAND REGISTER/ COUNTERS
13 DRIVERS
ERASE 4
ZERO COUNT 7
14 DISK COMMAND LOGIC
TRANSFER COMMAND STROBE
TRANSFER COMMAND STROBE
DI0-7 SEE FIG. 8-16
SOUT 45
SHLTA 48
SSTACK 98
SINTA 96
PINTE 28
PWAIT 27
SINP 46
SM1 44
ADDR DSBL 22
DO DSBL 23
CC DSBL 19
STATUS DSBL 18
+5V
PHLDA 26
SMEMR 47
SWO 97
PDBIN 78
PWR 77
PSYNC 76
PHOLD 74
BUSTR 7
WRITE 28
R/W 2
DMAOFF 34
TO CONTROLLER PCB
CLOCK Ø 26
CLOCK 2 40
MAIN CLOCK 36
ORE·TC 4
HOLD 18
(SERIAL DATA OUT) FIFO QS 12
(SERIAL DATA DURING WRITE)
P3
CONTROLLER FORMATTER
CONTROLLER PI OUT TO S-100 BACKPLANE
RESISTOR NET U3-14
A0-15 SEE FIG. 8-16
WRITE 5
-WRITE GATE 40
-DRIVE SELECT 1 28
-DRIVE SELECT 2 26
-SELECT DISK 1 2
-LOAD HEAD Ø 18
-LOAD HEAD 1 4
-STEP 36
-RESTORE 12
-INWARD MOTION 34
-WRITE DATA 38
-SPINDLE MOTOR ENABLE 24
FROM CONTROLLER (P3-Pin 38)
CONTROLLER P2

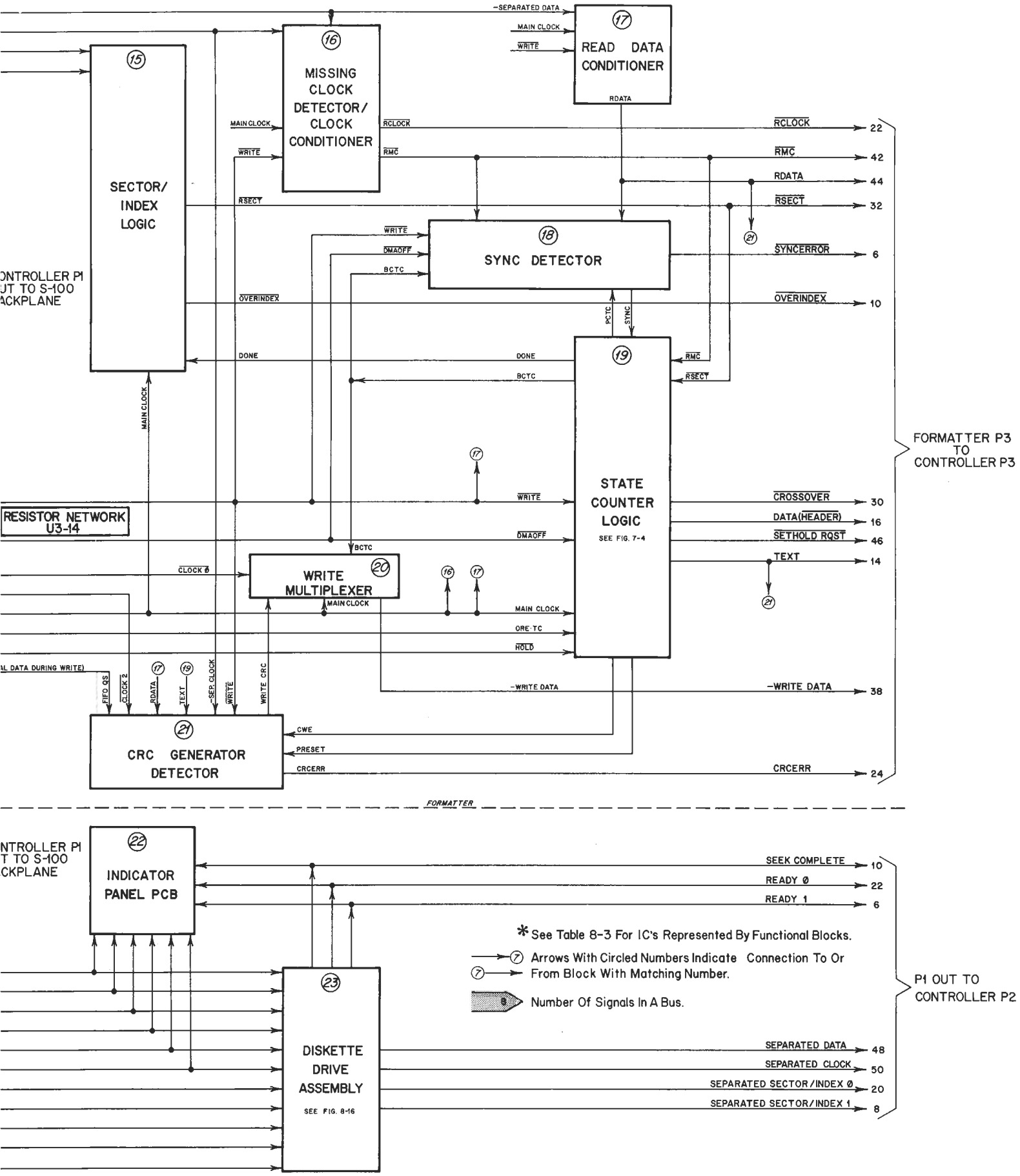
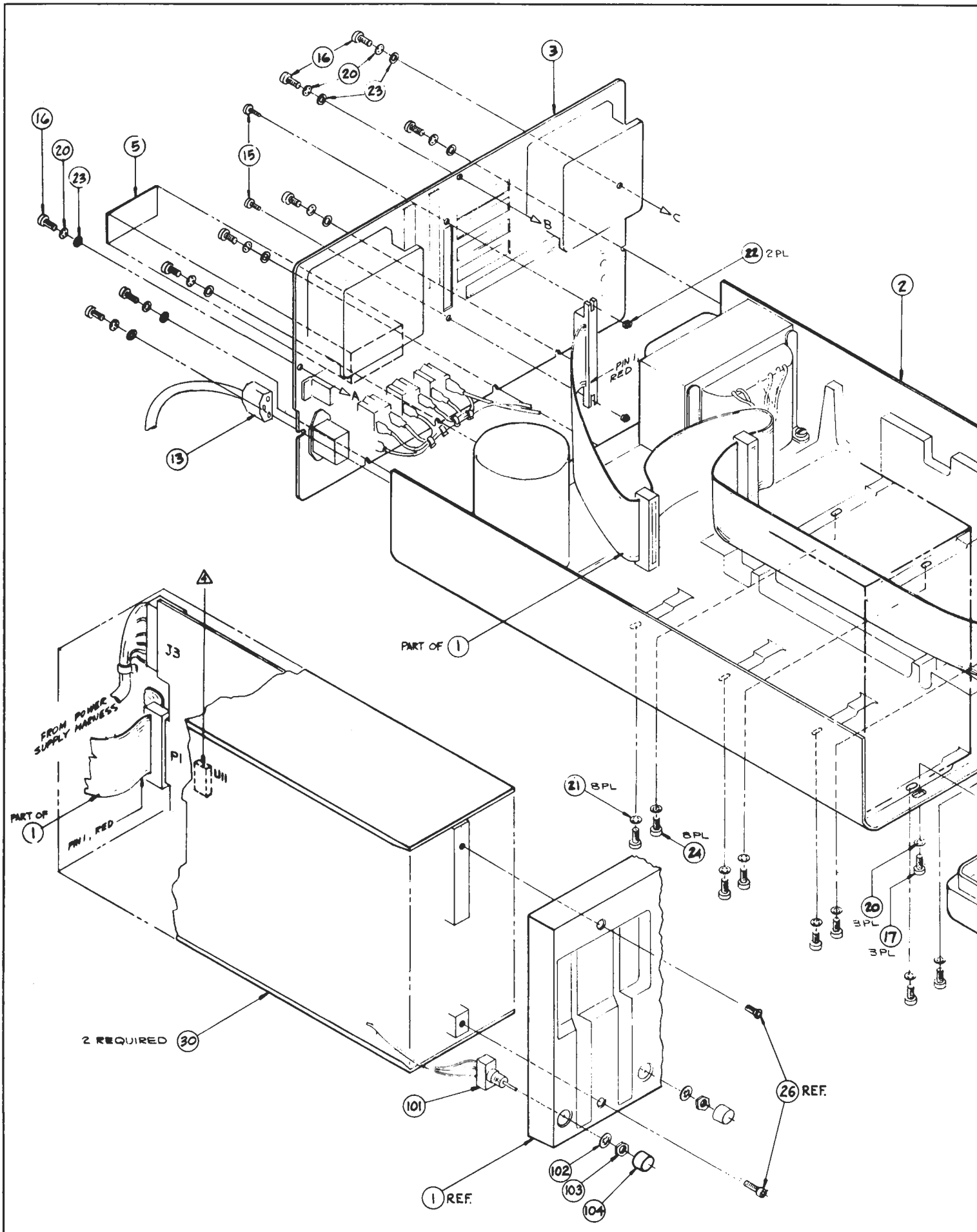
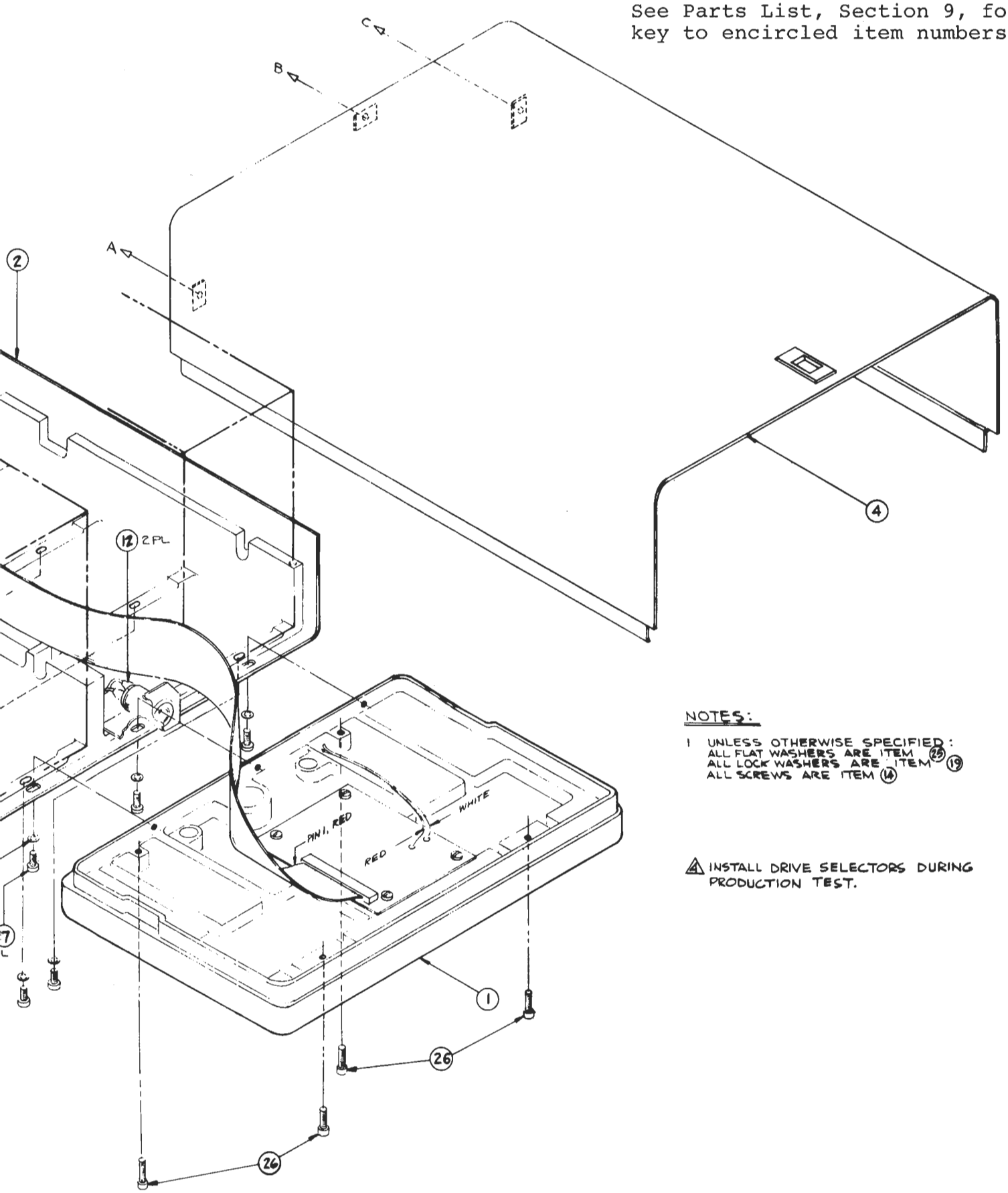


Fig. 8-17 System Block Diagram (I-3-78)


16
20
23
3
5
15
B
C
22 2PL
2
PIN 1 RED
A
13
PART OF 1
4
J3
FROM POWER SUPPLY HARNESS
P1
PART OF 1
PIN 1, RED
21 8PL
8PL
24
20 3PL
17 3PL
2 REQUIRED 30
101
26 REF.
1 REF.
102
103
104

See Parts List, Section 9, for key to encircled item numbers

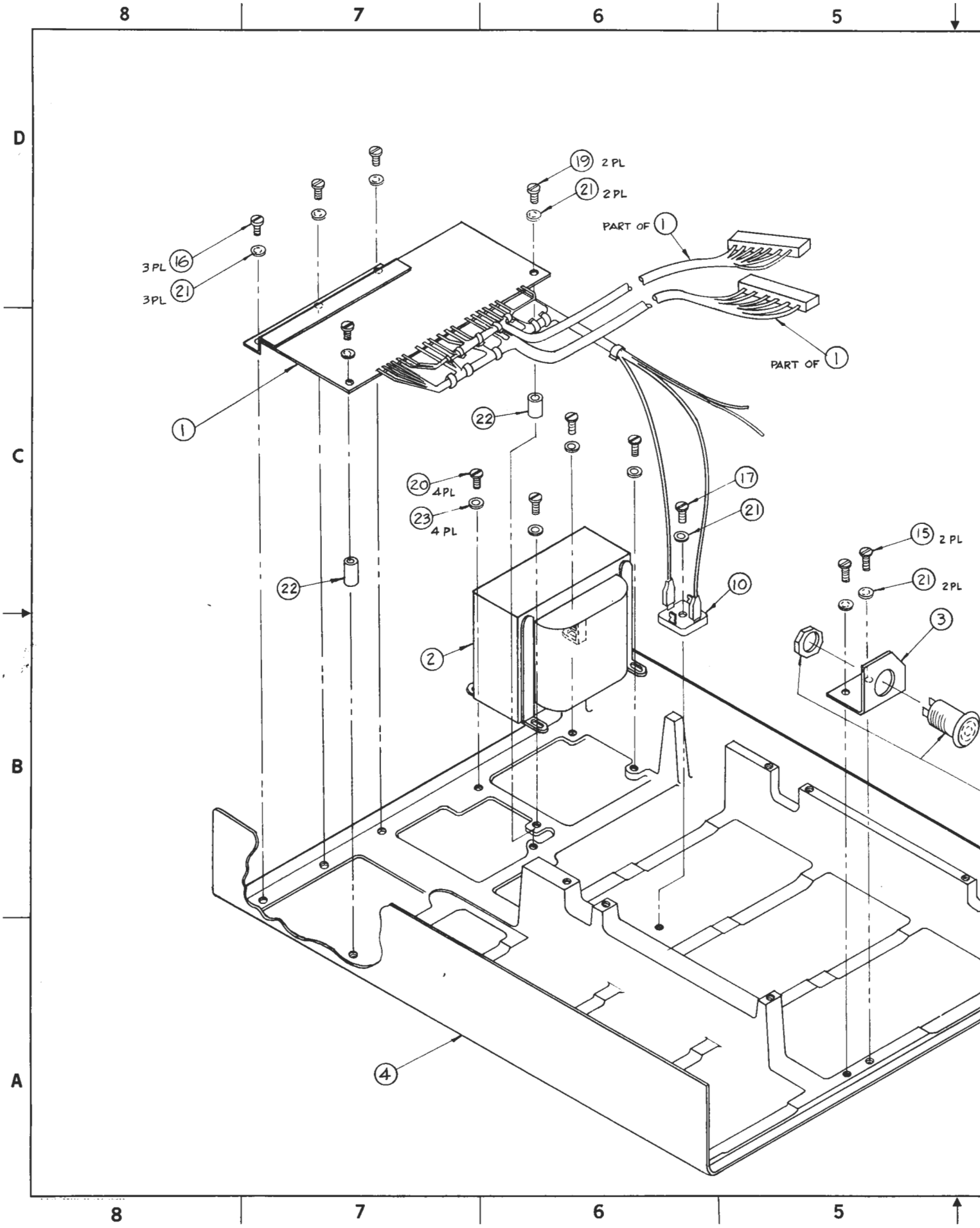


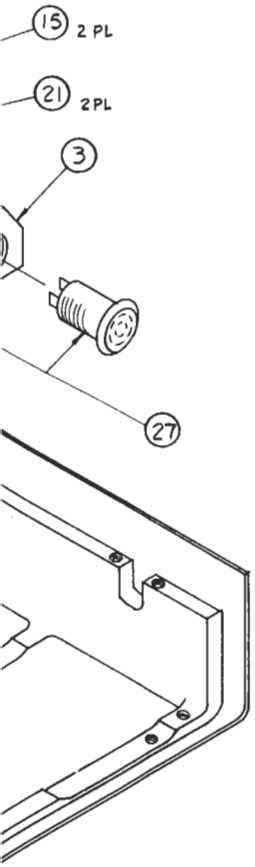
NOTES:

1 UNLESS OTHERWISE SPECIFIED:
ALL FLAT WASHERS ARE ITEM (25)
ALL LOCK WASHERS ARE ITEM (19)
ALL SCREWS ARE ITEM (14)

⚠ INSTALL DRIVE SELECTORS DURING PRODUCTION TEST.

Fig. 8-18 Cabinet Assembly, Model 4, Exploded


8
7
6
5
D
C
B
A
19 2 PL
21 2 PL
PART OF 1
3 PL 16
3 PL 21
PART OF 1
1
22
20 4 PL
23 4 PL
17
21
22
10
15 2 PL
21 2 PL
3
2
4

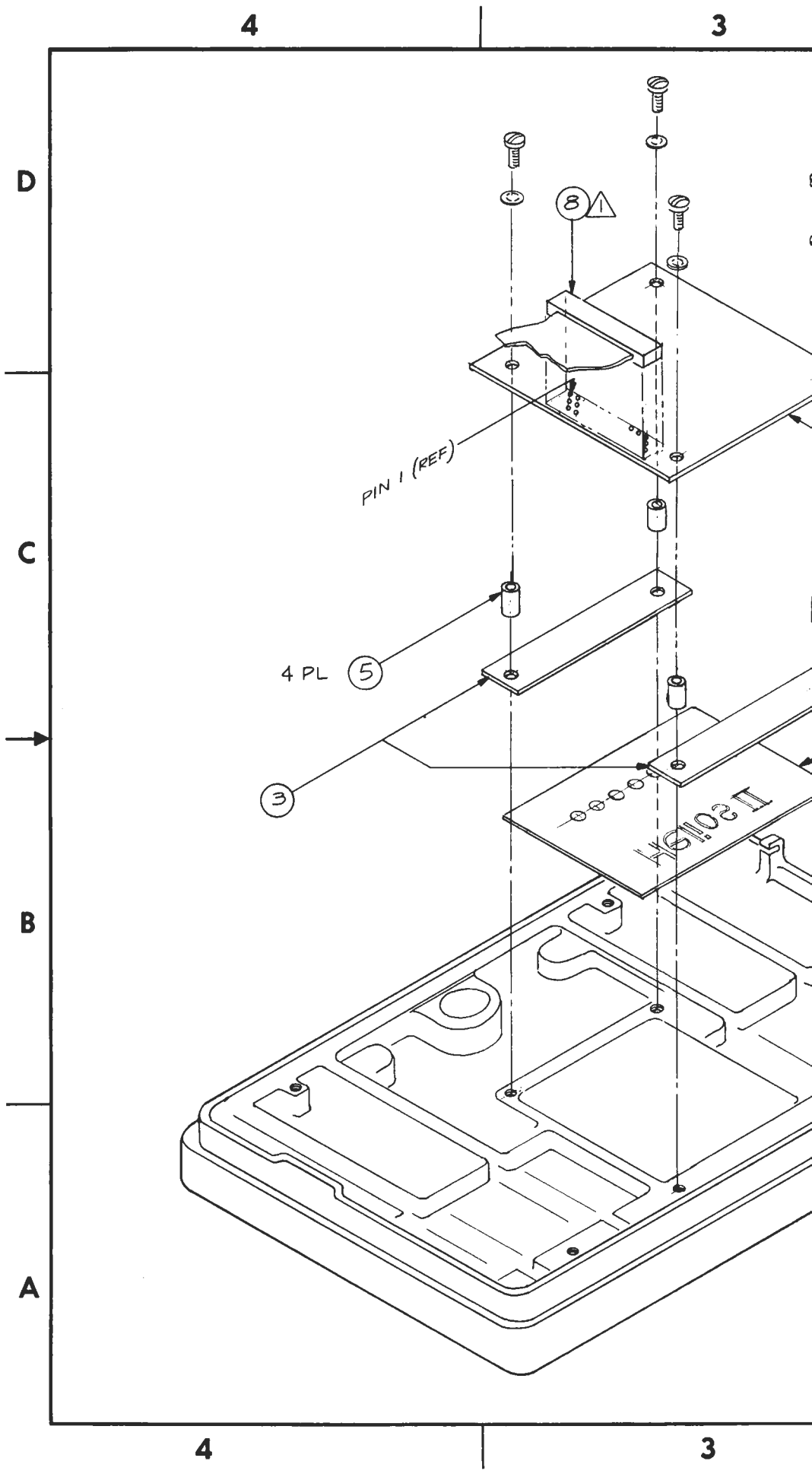


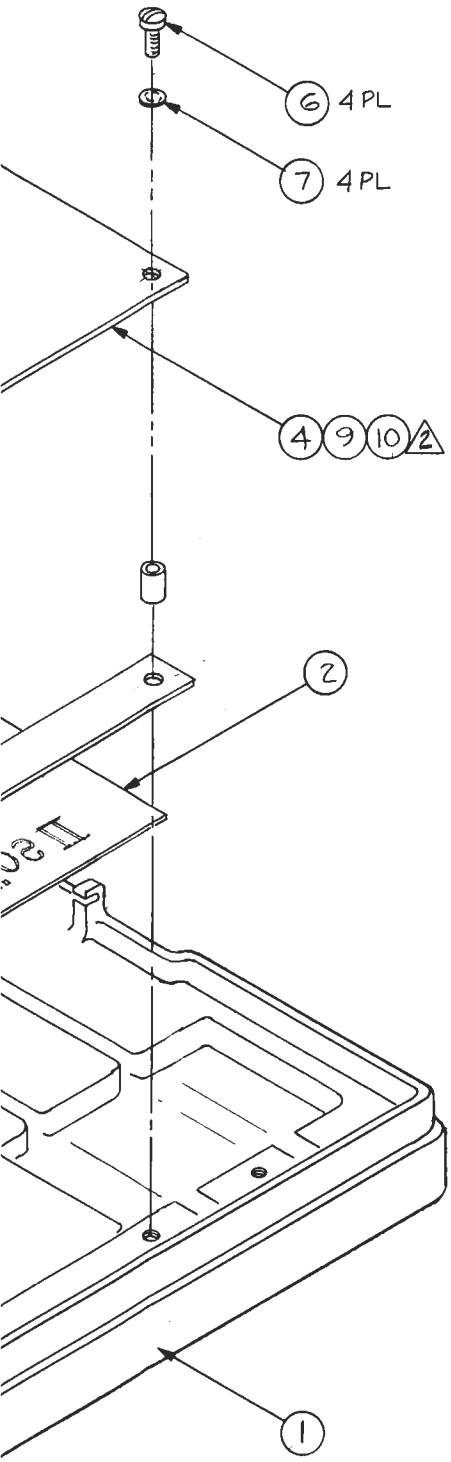
See Parts List, Section 9, for key to encircled item numbers

304020

2 Helios II

Fig. 8-19 Base Assembly, Model 4, Exploded


4
3
D
C
B
A
8
1
PIN 1 (REF)
4 PL
5
3



NOTES:

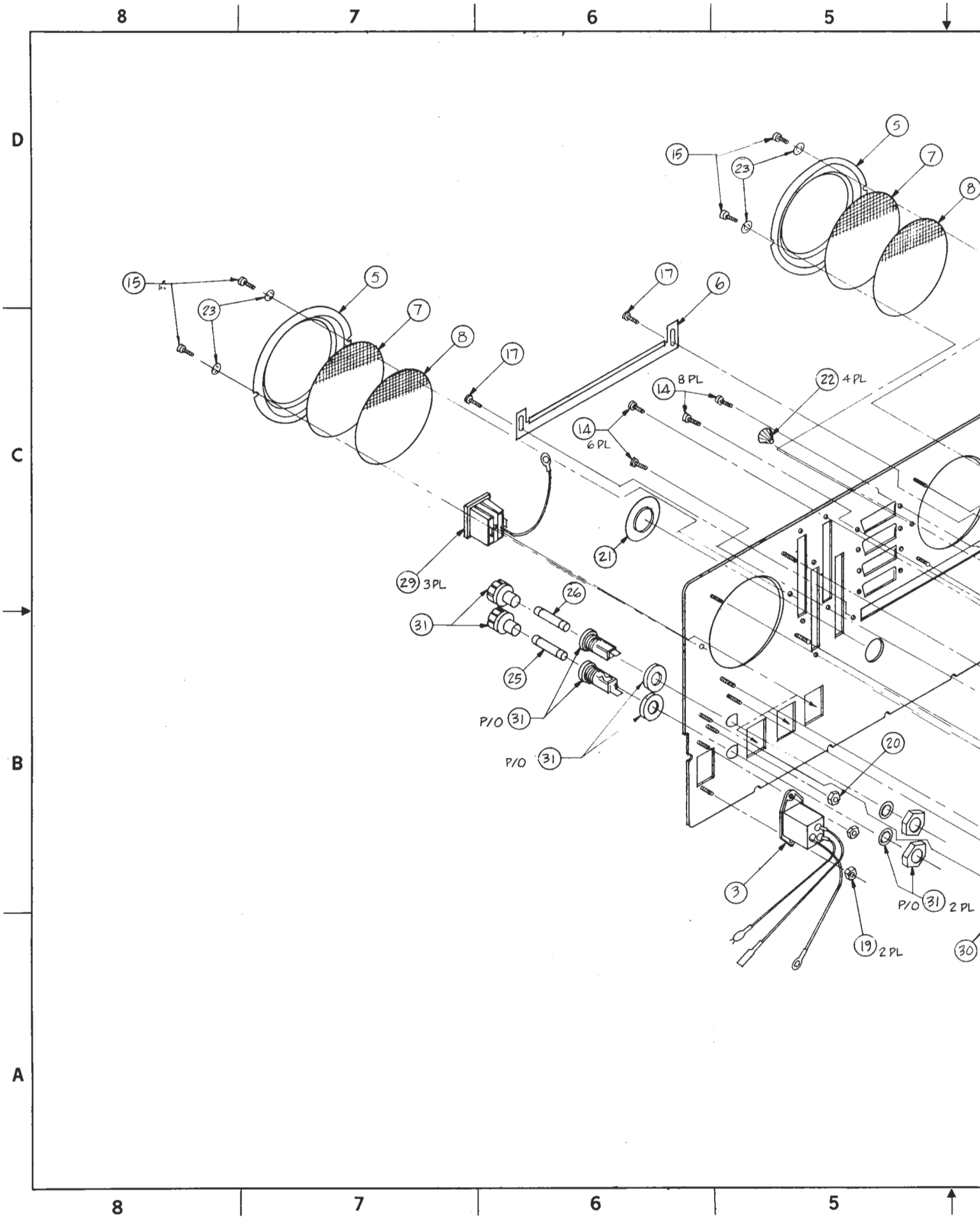
1. SOLDER ITEM 8 TO ITEM 4 BEFORE ITEM 4 IS MOUNTED TO ITEM 1.
2. MOUNT AND SOLDER D3, D4, R3, R4 (ITEMS 9 AND 10) ON P.C. BOARD (ITEM 4) BEFORE MOUNTING ITEM 4 TO ITEM 1.

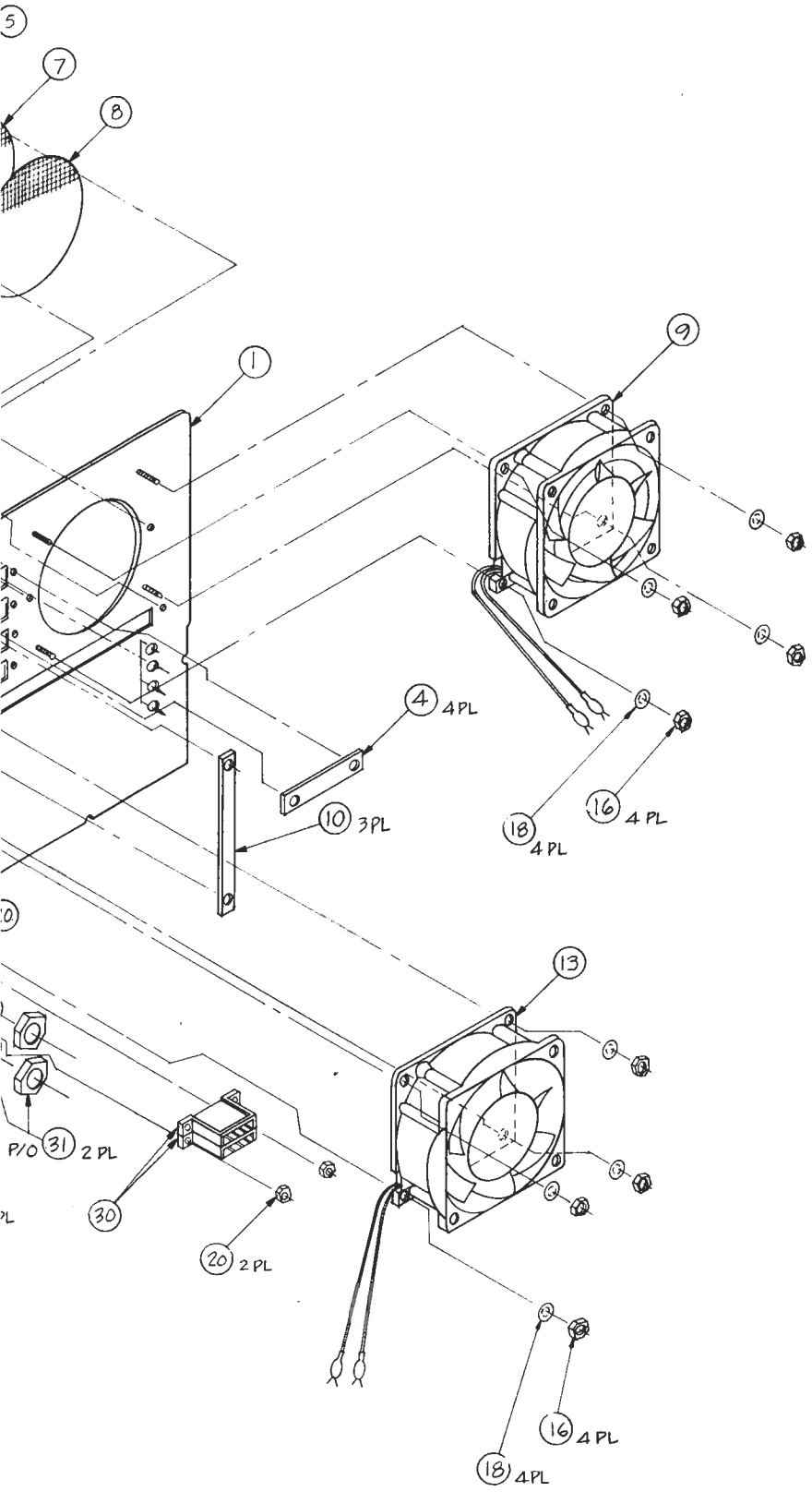
See Parts List, Section 9, for key to encircled item numbers

304010

2 Helios II

Fig. 8-20 Bezel Assembly, Model 4, Exploded


8
7
6
5
D
C
B
A
15
23
5
7
8
17
6
14 8 PL
22 4 PL
14 6 PL
21
29 3 PL
31
26
25
P/O 31
P/O 31
20
3
P/O 31 2 PL
19 2 PL
30



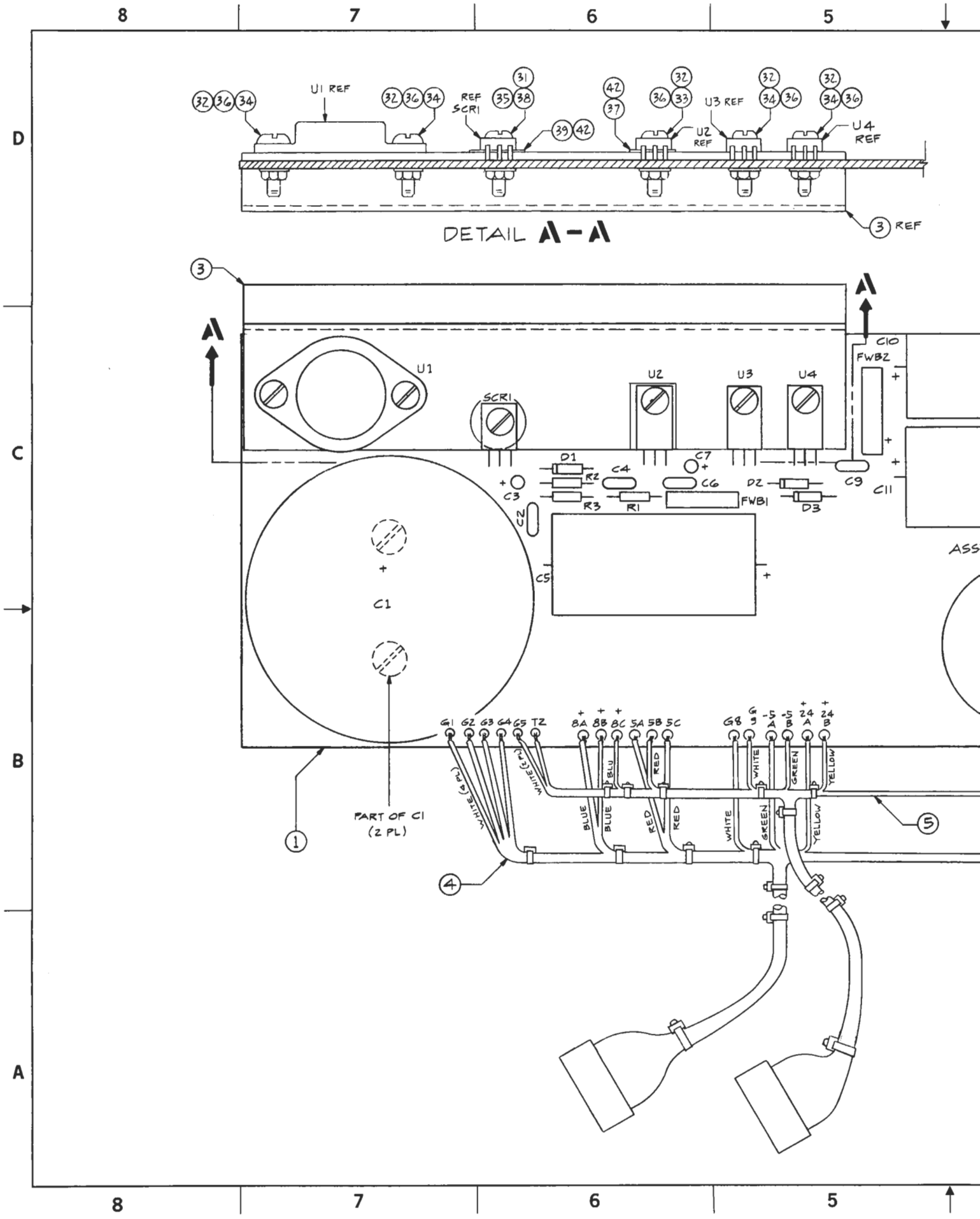
NOTES;
⚠ FOR AC POWER INTERCONNECT CABLE ITEM②, INSTALLATION REFER TO WIRING DIAGRAM 300006.

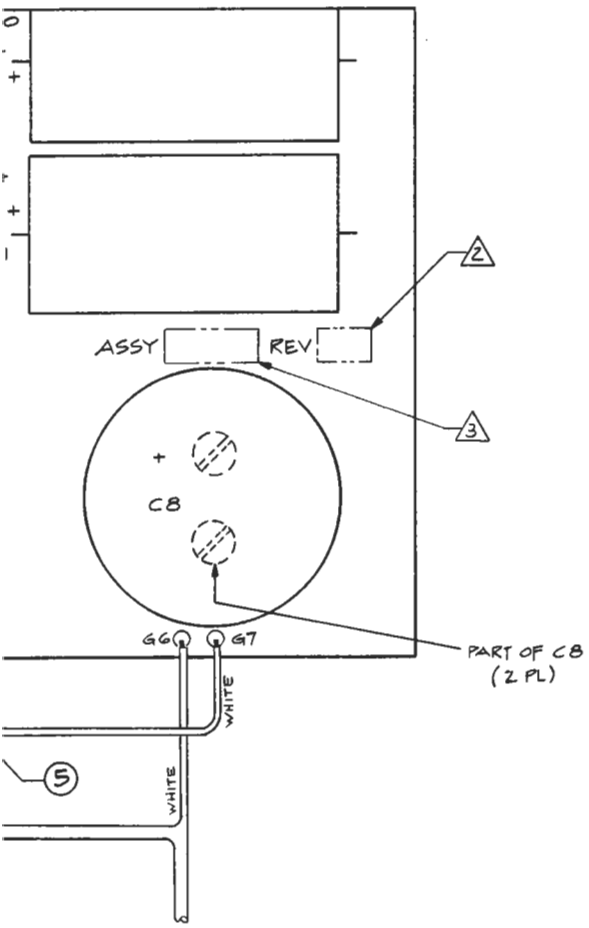
See Parts List, Section 9, for key to encircled item numbers

2 Helios II

304030 A

Fig. 8-21 Rear Panel Assembly, Model 4, Exploded


U1 REF
REF SCR1
U2 REF
U3 REF
U4 REF
3 REF
DETAIL A-A
U1
U2
U3
U4
SCR1
C1
C2
C3
C4
C5
C6
C7
C9
C10
C11
D1
D2
D3
R1
R2
R3
FWB1
FWB2
PART OF C1 (2 PL)
G1 G2 G3 G4 G5 TZ
8A 8B 8C 5A 5B 5C
G8 G9 -5A -5B 24A 24B
WHITE (4 PL)
WHITE (2 PL)
BLUE
RED
WHITE
GREEN
YELLOW



NOTES:

1. THERMAL COMPOUND, ITEM 37, IS TO BE PLACED BETWEEN HEATSINK AND ALL COMPONENTS WHICH ARE MOUNTED TO THE HEATSINK.
2. MARK REV LETTER WITH INDELLIBLE INK IN APPROXIMATE AREA SHOWN.
3. MARK ASSY NO. "304025" IN APPROXIMATE AREA SHOWN.

See Parts List, Section 9, for key to encircled item numbers

2 Helios II

304025 A

Fig. 8-22 Regulator PCB Assembly, Model 4

CONTENTS

SECTION 9 APPENDIX

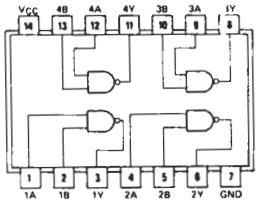
```
                        0000          LST
                        0000 *
                        0000 * THIS JUMP TABLE PROVIDES STANDARD ENTRY
                        0000 *POINTS FOR TEST START-UP AND INPUT/OUTPUT.
                        0000 *
                        0000 *
0006 C3 45 00           0000 BEGIN    JMP     START   TEST ENTRY POINT
                        0000 *
0009 C3 49 11           0000 OSOUT    JMP     CHOUT   CHAR. OUTPUT
                        0000 *
000C C3 53 11           0000 OSIN     JMP     CHIN    CHAR./STATUS CHECK
                        0000 *
000F C3 64 11           0000 INA      JMP     INPUT   STANDARD CHAR. INPUT
                        0000 *
0012 C3 90 11           0000 EORMS    JMP     EXIT    RETURN TO SOLOS/CUTER
                        0000 *
                        0000 *
                        0000          LST
                        0000 * THIS ROUTINE OUTPUTS THE CHAR. IN REG. B
                        0000 *TO THE PSEUDO-PORT DEFINED BY PPORT.
                        0000 *
                        0000 CHOUT    PUSH    D       KEEP IT CLEAN
                        0000          LXI     D,AOUT  ENTRY TABLE OFFSET
                        0000          LDA     PPORT   PSEUDO-PORT #
                        0000          JMP     OSIO
                        0000 *
                        0000 * THIS ROUTINE GETS A CHAR. OR STATUS FROM
                        0000 *THE DEFAULT PSEUDO-PORT. ON RETURN IF THE
                        0000 *ZERO FLAG IS SET REG. A CONTAINS THE CHAR.
                        0000 *ZERO FLAG RESET INDICATES NO CHAR.
                        0000 *
                        0000 CHIN     PUSH    D       KEEP IT CLEAN
                        0000          LXI     D,SINP  ENTRY TABLE OFFSET
                        0000 *
                        0000 * THIS ROUTINE COMPUTES THE ENTRY POINT
                        0000 *ADDRESS, PUTS A RETURN ADDRESS ON THE
                        0000 *STACK, AND JUMPS TO THE ENTRY POINT.
                        0000 *
                        0000 OSIO     PUSH    H       KEEP IT CLEAN TOO
                        0000          LHLD    IOTAB   ENTRY TABLE ADDRESS
                        0000          DAD     D       HL=ENTRY ADDRESS
                        0000          LXI     D,IORTN  OUR RETURN ADDRESS
                        0000          PUSH    D       ONTO STACK
                        0000          PCHL    .       TO I/O ENTRY POINT
                        0000 *
                        0000 * SOLOS/CUTER RETURNS TO THIS POINT WHEN
                        0000 *IT HAS FINISHED PROCESSING AN I/O CALL.
                        0000 *
                        0000 IORTN    POP     H       IT'S CLEAN
                        0000          POP     D       IT'S CLEAN TOO
                        0000          RET     .       I/O FINISHED
                        0000 *
```

```
0000 * THIS ROUTINE WAITS FOR A CHAR. FROM THE
0000 *DEFAULT PSEUDO-PORT. THEN SETS BIT 7 TO
0000 *ZERO,CHECKS FOR AN ESCAPE,AND RETURNS
0000 *WITH THE CHAR. IN REG. B.
0000 *
0000 INPUT   CALL   OSIN    GET CHAR. OR STATUS
0000         JZ     INPUT   NO CHAR. YET
0000 INB     ANI    7FH     SET BIT 7 TO 0
0000         CPI    1BH     ESCAPE ?
0000         JZ     EORMS   YES. GO PROCESS IT
0000         MOV    B,A     NO. PUT CHAR IN REG. B.
0000         RET    .       FINISHED
0000 *
0000         LST
0000 *
0000 * THIS ROUTINE JUMPS TO THE SOLOS/CUTER
0000 * RE-ENTRY POINT.
0000 *
0000 EXIT    LHLD   IOTAB   HL=ENTRY TABLE ADDRESS
0000         INX    H
0000         INX    H
0000         INX    H
0000         INX    H       HL=RE-ENTRY POINT
0000         PCHL   .       JUMP TO SOLOS/CUTER
0000 *
```

74LS00

QUADRUPLE 2-INPUT POSITIVE-NAND GATES

positive logic:
$Y = \overline{AB}$

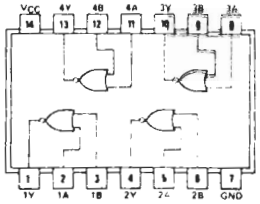


SN5400 (J) SN7400 (J, N)
SN54H00 (J) SN74H00 (J, N)
SN54L00 (J) SN74L00 (J, N)
SN54LS00 (J, W) SN74LS00 (J, N)
SN54S00 (J, W) SN74S00 (J, N)

74LS02

QUADRUPLE 2-INPUT POSITIVE-NOR GATES

positive logic:
$Y = \overline{A+B}$

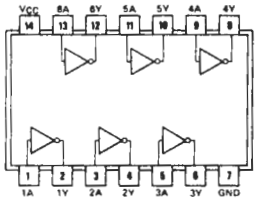


SN5402 (J) SN7402 (J, N)
SN54L02 (J) SN74L02 (J, N)
SN54LS02 (J, W) SN74LS02 (J, N)
SN54S02 (J, W) SN74S02 (J, N)

74LS04

HEX INVERTERS

positive logic:
$Y = \overline{A}$

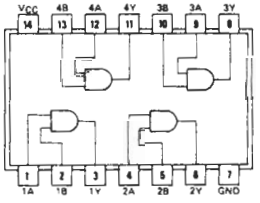


SN5404 (J) SN7404 (J, N)
SN54H04 (J) SN74H04 (J, N)
SN54L04 (J) SN74L04 (J, N)
SN54LS04 (J, W) SN74LS04 (J, N)
SN54S04 (J, W) SN74S04 (J, N)

74LS08

QUADRUPLE 2-INPUT POSITIVE-AND GATES

positive logic:
$Y = AB$

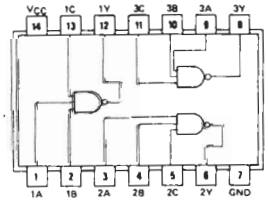


SN5408 (J, W) SN7408 (J, N)
SN54LS08 (J, W) SN74LS08 (J, N)
SN54S08 (J, W) SN74S08 (J, N)

74LS10

TRIPLE 3-INPUT POSITIVE-NAND GATES

positive logic:
$Y = \overline{ABC}$

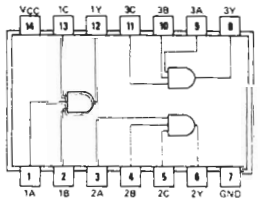


SN5410 (J) SN7410 (J, N)
SN54H10 (J) SN74H10 (J, N)
SN54L10 (J) SN74L10 (J, N)
SN54LS10 (J, W) SN74LS10 (J, N)
SN54S10 (J, W) SN74S10 (J, N)

74LS11

TRIPLE 3-INPUT POSITIVE-AND GATES

positive logic:
$Y = ABC$

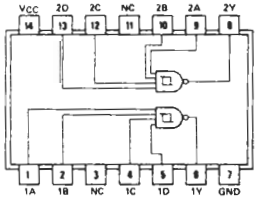


SN54H11 (J) SN74H11 (J, N)
SN54LS11 (J, W) SN74LS11 (J, N)
SN54S11 (J, W) SN74S11 (J, N)

74LS13

DUAL 4-INPUT POSITIVE-NAND SCHMITT TRIGGERS

positive logic:
$Y = \overline{ABCD}$



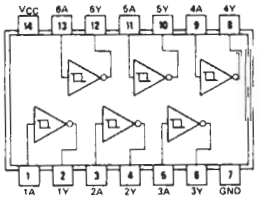
SN5413 (J, W) SN7413 (J, N)
SN54LS13 (J, W) SN74LS13 (J, N)

NC—No internal connection

74LS14

HEX SCHMITT-TRIGGER INVERTERS

positive logic:
$Y = \overline{A}$

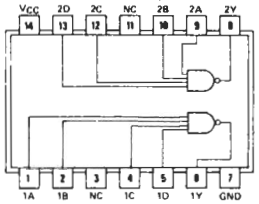


SN5414 (J, W) SN7414 (J, N)
SN54LS14 (J, W) SN74LS14 (J, N)

74LS20

DUAL 4-INPUT POSITIVE-NAND GATES

positive logic:
$Y = \overline{ABCD}$



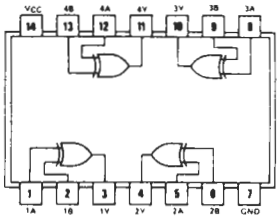
SN5420 (J) SN7420 (J, N)
SN54H20 (J) SN74H20 (J, N)
SN54L20 (J) SN74L20 (J, N)
SN54LS20 (J, W) SN74LS20 (J, N)
SN54S20 (J, W) SN74S20 (J, N)

74LS86 Quad 2-Input Exclusive-OR Gates

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level



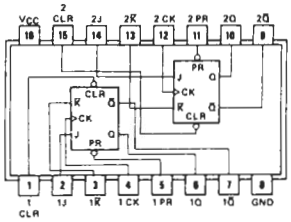
SN54L86 (J) SN74L86 (J, N)

74LS109

DUAL J-$\overline{K}$ POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$



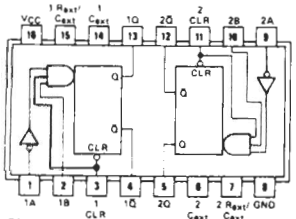
SN54109 (J, W) SN74109 (J, N)
SN54LS109A (J, W) SN74LS109A (J, N)

74LS123

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

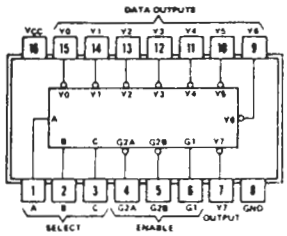
FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎



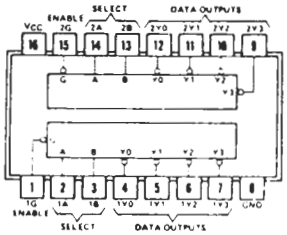
SN54123 (J, W) SN74123 (J, N)
SN54L123 (J) SN74L123 (J, N)
SN54LS123 (J, W) SN74LS123 (J, N)

74LS138 3-8 Line Decoder



SN54LS138 (J, W) SN74LS138 (J, N)
SN54S138 (J, W) SN74S138 (J, N)

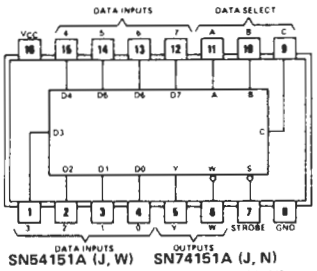
74LS139 Dual 2-to-4 Line Decoder



SN54LS139 (J, W) SN74LS139 (J, N)
SN54S 139 (J, W) SN74S139 (J, N)

74LS151

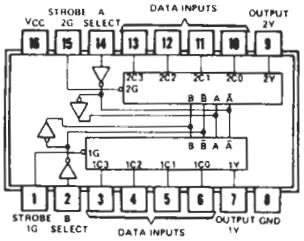
1-OF-8 DATA SELECTORS/MULTIPLEXERS



SN54151A (J, W) SN74151A (J, N)
SN54LS151 (J, W) SN74LS151 (J, N)
SN54S151 (J, W) SN74S151 (J, N)

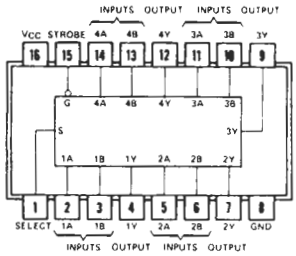
74LS153

DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS



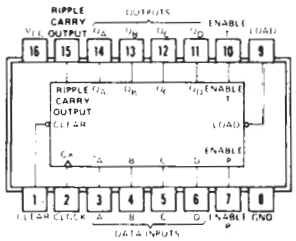
SN54153 (J, W) SN74153 (J, N)
SN54L153 (J) SN74L153 (J, N)
SN54LS153 (J, W) SN74LS153 (J, N)
SN54S153 (J, W) SN74S153 (J, N)

74LS157 Quad 2-to-1 Line Multiplexer
74LS158 Quad 2-to-1 Line Multiplexer, with Inverted Outputs



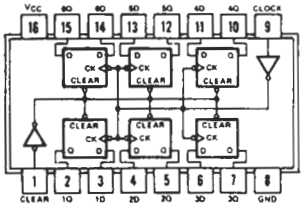
SN54157 (J, W) SN74157 (J, N)
SN54L157 (J) SN74L157 (J, N)
SN54LS157 (J, W) SN74LS157 (J, N)
SN54S157 (J, W) SN54S157 (J, N)
SN54LS158 (J, W) SN74LS158 (J, N)
SN54S158 (J, W) SN74S158 (J, N)

74LS163 Synchronous 4-Bit Binary Counter



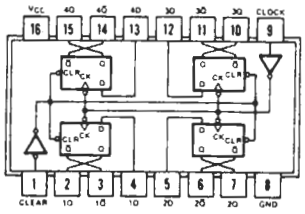
SN54160 (J, W) SN74160 (J, N)
SN54LS160A (J, W) SN74LS160A (J, N)
SN54161 (J, W) SN74161 (J, N)
SN54LS161A (J, W) SN74LS161A (J, N)
SN54162 (J, W) SN74162 (J, N)
SN54LS162A (J, W) SN74LS162A (J, N)
SN54S162 (J, W) SN74S162 (J, N)
SN54163 (J, W) SN74163 (J, N)
SN54LS163A (J, W) SN74LS163A (J, N)
SN54S163 (J, W) SN74S163 (J, N)

74LS174 Hex D Flipflop



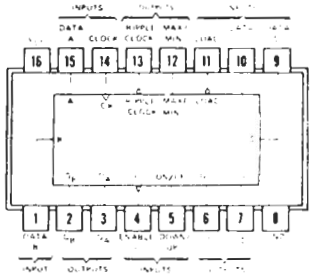
SN54174 (J, W) SN74174 (J, N)
SN54LS174 (J, W SN74LS174 (J, N)
SN54S174 (J, W) SN74S174 (J, N)

74LS175 Quad D Flipflop



SN54175 (J, W) SN74175 (J, N)
SN54LS175 (J, W) SN74LS175 (J, N)
SN54S175 (J, W) SN74S175 (J, N)

74LS191 Synchronous Up/Down Counter



SN54190 (J, W) SN74190 (J, N)
SN54LS190 (J, W) SN74LS190 (J, N)
SN54191 (J, W) SN74191 (J, N)
SN54LS191 (J, W) SN74LS191 (J, N)

74LS279

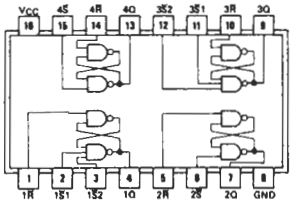
QUAD $\overline{S}$-$\overline{R}$ LATCHES

DIODE-CLAMPED INPUTS
TOTEM-POLE OUTPUTS

FUNCTION TABLE

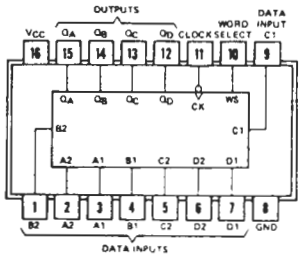
INPUTS $\overline{S}$	INPUTS $\overline{R}$	OUTPUT Q
H	H	Q_0
L	H	H
H	L	L
L	L	H*

H = high level
L = low level
Q_0 = the level of Q before the indicated input conditions were established.
* This output level is pseudo stable; that is, it may not persist when the $\overline{S}$ and $\overline{R}$ inputs return to their inactive (high) level.
† For latches with double $\overline{S}$ inputs:
H = both $\overline{S}$ inputs high
L = one or both $\overline{S}$ inputs low



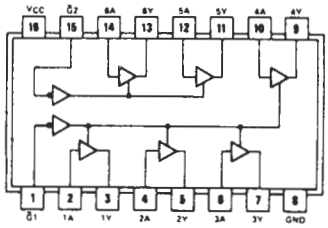
SN54279 (J, W) **SN74279 (J, N)**
SN54LS279 (J, W) **SN74LS279 (J, N)**

74LS298 Quad 2-Input Multiplexer, with Storage



SN54298 (J, W) **SN74298 (J, N)**
SN54LS298 (J, W) **SN74LS298 (J, N)**

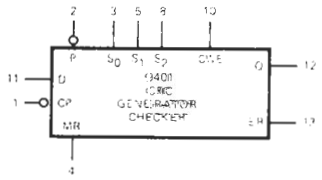
8T97 (74LS367) High Speed Hex Buffer/Inverter



SN54367A (J, W) **SN74367A (J, N)**
SN54LS367 (J, W) **SN74LS367 (J, N)**

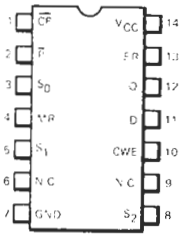
9401 C.R.C. Generator

LOGIC SYMBOL



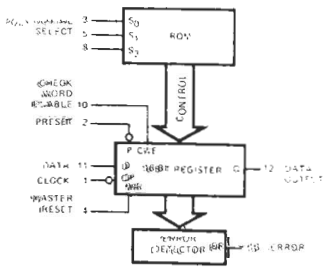
V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAM DIP (TOP VIEW)



Pins 6 and 9 not connected.

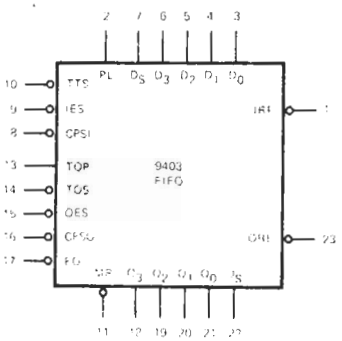
BLOCK DIAGRAM



V_{CC} = 14
GND = 7

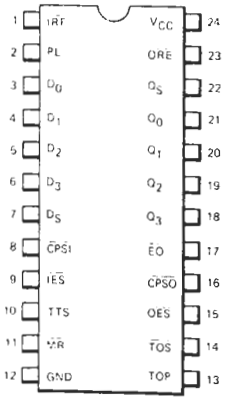
9403 4 x 16 FIFO Buffer

LOGIC SYMBOL

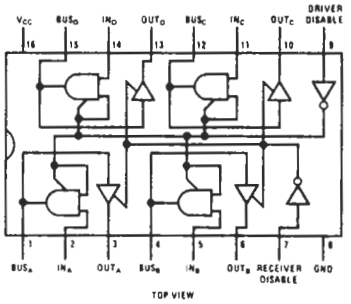


V_{CC} = Pin 24
GND = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



8833 Quad Tri-State Party Line Transceiver



TOP VIEW

Order Number DS7833J, DS8833J, DS8833N or DS7833W

general description

This family of TRI-STATE Party Line Transceivers offer extreme versatility in bus organized data transmission systems. The data bus may be unterminated, or terminated dc or ac, at one or both ends. Drivers in the third (high impedance) state load the data bus with a negligible leakage current. The receiver input current is low allowing at least 100 driver/receiver pairs to utilize a single bus. The bus loading is unchanged when V_{CC} = 0V. The receiver incorporates hysteresis to provide greater noise immunity. All devices utilize a high current TRI-STATE output driver. The DS7833/DS8833 and DS7835/DS8835 employ TRI-STATE outputs on the receiver also.

The DS7833/DS8833 are non-inverting quad transceivers with a common inverter driver disable control and a common inverter receiver disable control.

The DS7835/DS8835 are inverting quad transceivers with a common inverter driver disable control and a common inverter receiver disable control.

KEY NUMBERS

The encircled item numbers, in the first column of the parts list, refer to the encircled matching key numbers on the assembly drawings of the same name. Assembly drawings are found in Section 8, Drawings.

STANDARD PARTS AND EQUIVALENTS

The standard vendor part number is underlined and is the first part number in the field called "Standard Vendor Part and Equivalent(s)." Equivalent parts, if any, follow the standard vendor part number.

PARTS LIST - SYSTEM ASSEMBLY, MODEL 2 (301006A)

ITEM #	PART #	QTY	DESCRIPTION	
(1)	301000	1	Assy, PCB, Controller, Helios II	Separate Parts List follows.
(2)	301003	1	Assy, PCB, Formatter	
(3)	301007	1	Assy Cable, Disk Controller/ Formatter Interconnect	
(4)	301009	1	Assy Cable, Disk Controller/Cabinet	
(5)	300000	1	Cabinet Assembly (See separate parts list.)	

PARTS LIST - CABINET ASSEMBLY, MODEL 2 (300000C)

ITEM #	PART #	QTY	DESCRIPTION
1	301006	1	Assy, Controller — Separate Parts List follows.
(2)	302004	1	Assy, Base — Separate Parts List follows.
(3)	306000	1	Assy, Bezel — Separate Parts List follows.
(4)	307000	1	Assy, Top Cover
(5)	305000	1	Assy, Rear Panel (See separate Parts List.)
6	730009	1	Helios II, Disk Memory System Manual (Includes PTDOS User's Manual)
(7)	722005	1	Disk Drv, Dual
(8)	718001	1	Cable, AC Pwr, 3 Wire
9	720003	6	PHMS, 4-40 x 5/16"
(10)	720016	3	PHMS, 6-32 x 1/4"
(11)	720069	4	PHMS, 8-32 x 5/8"
(12)	720018	3	PHMS, 6-32 x 7/16"
(13)	720041	7	ITLW, #6
(14)	720038	8	ITLW, #4
(15)	720051	4	ITLW, #8
16	720070	6	FW, Zinc, #4
(17)	720067	3	FW, #6
(18)	720072	1	Screw, 8-32 x 1", Blk Cap
(19)	300003	1	Label, Serial Number, Helios II
(20)	716016	2	Tubing, Shrink, 3/16 x 1"
(21)	720020	1	PHMS, 6-32 x 1/2"
(22)	720056	2	#4 Kep Nut
(23)	720005	2	PHMS, 4-40 x 1/2"
24	701109	1	Dual 4-Input AND, 74LS21
25	727030	1	PTDOS 1.4 System Diskette
26	722021	1	Flexible Disk, Blank
27	727026	1	Cassette, Disk Sys. Test
(101)	PERSCI-100026	2	Momentary Switch, Push.
(102)	720058	2	ITLW #12 (Part of 101)
(103)	—	2	#12 Hexnut (Part of 101)
(104)	—	2	Pushbutton switch cover (Part of 101)

PARTS LIST - BASE ASSEMBLY, MODEL 2 (302004D)

ITEM #	PART #	QTY	DESCRIPTION
1	302008	1	Fab, Base
2	302005	1	Trans., Pwr., Helios II
3	302000	1	Assy, PCB, Reg., Helios II (See separate parts list.)
4	302007	1	Fab, Bracket, Keyswitch
5	703033	1	MDA3500, DIO, Br. Rect. 50PIV, 35A
6	723006	1	Switch, AC Pwr, Key
7	720017	3	PHMS, 6-32 x 5/16"
8	720041	8	ITLW, #6
9	720048	2	Spacer, RND, CLR, #6 x 3/8"
10	720032	4	PHMS, 8-32 x 1/2"
11	720051	4	ITLW, #8
12	720022	2	PHMS, 6-32 x 3/4"
14	720018	3	PHMS, 6-32 x 7/16"
15	720050	1	Spacer, Insul., Cir. #4 x 1/8

PARTS LIST - BEZEL ASSEMBLY, MODEL 2 (306000E)

ITEM #	PART #	QTY	DESCRIPTION
1	306001	1	Fab, Bezel, Helios II, One Drive
2	306003	1	Fab, Logo Panel, Helios II, Model 2
3	306005	2	Fab, Plex Retainer
4	300008	1	Assy, PCB, Indicator Panel (See separate parts list.)
5	720054	4	Spacer, 1/4" OD, 1/2" Long
6	720068	4	PHMS, 4-40 x 3/4
7	720001	4	PHMS, 4-40 x 3/16
8	720038	8	ITLW, #4
9	300011	1	Assy, Cable, Indicator/Signal

PARTS LIST - REAR PANEL ASSEMBLY, MODEL 2 (305000E)

Note: Item numbers correspond to the encircled key numbers on the exploded view of the rear panel, Fig. 8-5.

ITEM #	PART #	QTY	DESCRIPTION
1	305002	1	Rear Panel
4	305004	1	AC Power Interconn Cable
5	305008	4	Cover Plate D Connector
6	305014	3	Cover Plate, 50 Pin Conn
7	305010	1	Clamp
10	720001	14	PHMS, 4-40 x 3/16
11	720016	2	PHMS, 6-32 x 1/4
12	720041	4	ITLW, #6
13	720056	2	Nut, Kep, #4
14	720057	3	Nut, Kep, #6
15	105033	1	Fan, Assy, 3" Leads
16	720011	4	Hex nut, 6-32
17	723013	1	Fuse, Cart, 7A, SLO BLO
18	723018	1	Fuse, Cart, 3.2A, SLO BLO
19	305006	1	Filter, EMI
20	724003	3	Outlet, AC, Aux
21	724005	2	Comm Block, AC, 5 POS
22	724007	2	Fuse Holder, Cart, 3AG
23	720066	4	Insert 1/4" Round
24	720065	1	Insert 5/8" Round
25	720064	1	Insert 3" Round
27	720002	2	PHMS, 4-40 x 1/4"
28	305009	1	Filter Frame
29	305011	1	Filter Element
30	305012	1	Filter Screen
26	720038	2	ITLW, #4

PARTS LIST - CONTROLLER PCB ASSEMBLY (301000G)

ITEM #	PART #	QTY	REFERENCE CODE	STANDARD PART # & EQUIVALENT(S)	DESCRIPTION
(1)	301001	1			Fab, PCB, Controller, REV C
4	301002	REF			Schematic Dia, Controller
6	701090	2	U18,21	74LS00	Quad 2-Input NAND
7	701092	1	U19	74LS02, 9LS02	Quad 2-Input NOR
8	701094	1	U6	74LS04	Hex Inverter
9	701098	3	UØ,12,36	74LS08	Quad 2-Input AND
10	701100	1	U35	74LS10	Triple 3-Input NAND
11	701102	1	U17	74LS11	Triple 3-Input AND
12	701104	2	U8,23	74LS13	Dual 4-Input NAND
13	701106	1	U7	74LS14	Hex Inv, Schmitt
14	701118	1	U40	74LS86	Quad 2-Input EX-OR
15	701120	5	U2,10,20, U37,39	74LS109	Dual J-K FF
16	701122	1	U15	74LS123	Dual Retrig One-Shot
17	701128	1	U42	74LS138	3-to-8 Line Decoder
18	701130	2	U14,16	74LS139	Dual 2-to-4 Line Decoder
19	701138	2	U13,34	74LS157	Quad 2-to-1 Line MPX
20	701140	1	U11	74LS158	Quad 2-Input Inv MPX
21	701142	1	U5	74LS163	Synch 4 Bit Bin CNTR
22	701144	1	U31	74LS174	Hex D FF
23	701146	2	U1,38	74LS175, 25LS175	Quad D FF
24	701148	7	U24-30	74LS191	Synch UP/DN CNTR
25	701152	1	U33	74LS279	Quad S-R Latches
26	701156	1	U22	74LS298	Quad 2-MPX, Store
27	701177	2	U47,48	8833	Quad T-S XCVR, 16P
28	701186	11	U3,9,32,41, U43-46,49-51	8T97, DM8097(NA) 74367	High Speed Hex Buf/Inv
29	701196	2	U52,53	9403	4 x 16 FIFO Buf
30	701162	2	U54,55	7805,LM340T-5	Volt Reg, +5V, TO-220
33	702002	1	Q1	2N2222	Trans, NPN
36	703005	1	CR1	1N4148	Diode, Sil, SW
39	705022	3	R1,4,5		Res, 220Ω, CF, 1/4W, 5%
40	705025	3	R2,3,6		Res, 330Ω, CF, 1/4W, 5%
41	705061	2	R8,9		Res, 10KΩ, CF, 1/4W, 5%
42	705087	1	R7		Res, 1.5MΩ, CF, 1/4W, 5%
43	705096	1	U4	761-5-R-220/330	Res, 220/330Ω, DIP, NET
46	707023	18	C3-7,10-22		Cap, .047µf, Disk Cer, +80 -20%
47	707032	2	C9,23		Cap, 1.0µf, Tant, 35V, 10%
48	707034	1	C1		Cap, 2.2µf, Tant, 10%
49	707036	2	C2,8		Cap, 15µf, Tant, 20V, 10%
(52)	713004	13			Socket, DIP, 14P, Sldr
(53)	713006	39			Socket, DIP, 16P, Sldr
(54)	713013	4			Socket, Strip, 12P, Sldr
(55)	713018	3			Pins, Augat AG716, Pin, Rcpt, 16P
56	717050	1	P4		Connector Pin
57	717049	1	P4		Recpt, TP, PC, RT Ang, ORN
(58)	721022	1			Heatsink
(59)	720020	2			PHMS, 6-32 x 1/2"

ITEM #	PART #	QTY	REFERENCE CODE	STANDARD PART # & EQUIVALENT(S)	DESCRIPTION
(60)	720011	2			HN, 6-32
(61)	720041	2			ITLW, #6
62	717003	2	P2,3		Header, Male PC Mount, 50 Pin
(64)	711004	1			Label, Assy. Rev, 1/4"
(65)	716027-5	A/R			Wire, SS, Insul, 22 AWG
(67)	716007-5	A/R			Wire, SS, Insul, 24 AWG

PARTS LIST - FORMATTER PCB ASSEMBLY (301003E)

ITEM #	PART #	QTY	REFERENCE CODE	STANDARD PART # & EQUIVALENT(S)	DESCRIPTION
1	301004	1			PCB, Formatter
3	301005	REF			Schematic, Formatter
5	701090	1	U21	74LS00	Quad 2-Input NAND
6	701094	1	U24	74LS04	Hex Inv
7	701098	3	U19,23,26	74LS08	Quad 2-Input AND
8	701100	2	U16,22	74LS10	Triple 3-Input NAND
9	701108	1	U27	74LS20	Dual 4-Input NAND
10	701118	1	U20	74LS86	Quad 2-Input EX-OR
11	701120	4	U15,18,28, U29	74LS109	Dual J-K FF
12	701122	1	U17	74LS123	Dual Retrig One-Shot
13	701130	1	U25	74LS139	Dual 2-to-4 Line DEC
14	701132	3	U7,8,30	74LS151	8-to-1 Line MPX
15	701134	3	U6,9,10	74LS153	Dual 4-to-1 Line MPX
16	701142	3	U11,12,13	74LS163	Synch 4-Bit Binary CNTR
17	701146	1	U14	74LS175	Quad D FF
18	701162	1	U31	7805, LM340T-5	Volt Reg, +5V, TO-220
19	701186	2	U1,2	8T97, 8097, 74367	Hex Buffer/Inv
20	701188	1	U4	8T98, 8098, NT98, 74368	Hex Buf/Inv
21	701194	1	U5	9401, MW4101, SY2401	C.R.C. GEN
24	705096	1	U3	CTS 761-5-R 220/330	Res, DIP, NET, 220/330Ω
25	705056	1	R2		Res, 5.1KΩ, CF, 1/4W, 5%
26	705065	1	R1		Res, 15KΩ, CF, 1/4W, 5%
29	707007	2	C14,15		Cap, 390pf, MICA, 5%
30	707023	20	C3-13,16-24		Cap, .047µf, Disk Cer, +80 -20%
31	707032	1	C2		Cap, 1.0µf, TANT, 35V, 10%
32	707036	1	C1		Cap, 15µf, TANT, 20V, 10%
(35)	713004	10			Socket, DIP, 14P, Sldr
(36)	713006	20			Socket, DIP, 16P, Sldr
37	717015	1			Header, M, 5P, 90°
(38)	720002	1			PHMS, 4-40 x 1/4"
(39)	720010	1			HN, 4-40
(40)	720038	1			ITLW, #4
42	717003	1	P3		Header, Male PC Mount, 50 Pin

PARTS LIST - REGULATOR PCB ASSEMBLY, MODEL 2 (302000D)

ITEM #	PART #	QTY	REFERENCE CODE	DESCRIPTION
(1)	302001	1		Fab, PCB, Regulator, REV C
(2)	302010	1		Assy, Cable, Helios Power
(3)	302003	1		Fab, Heatsink
5	302002	REF		Schematic, Power Supply, Helios II
6	701163	1	U1	78H05 Volt Reg, +5V, 5A
7	701165	1	U2	7905µC Volt Reg, -5V, TO-220 or LM 320T-5
8	701167	1	U3	7824µC Volt Reg, +24V, TO-220 or LM340T-24
11	703003	1	D2	IN4001 Diode, SIL, PWR
12	703011	1	D1	IN5231B Diode, Zen, 5.1V, 1/2W, 5%
13	703027	1	SCR1	MCR 106-2, SCR, 60PIV, 4A, 10632
14	703029	1	FWB1	Diode, Br Rect, 50PIV, 1.5A
15	703031	1	FWB2	Diode, Br Rect, 50PIV, 4A
18	705017	1	R3	Res, 100Ω, CF, 1/4W, 5%
19	705025	2	R1,2	Res, 330Ω, CF, 1/4W, 5%
22	707023	4	C2,4,6,9	Cap, .047µf, Disk CER +80 -20%
23	707036	2	C3,7	Cap, 15µf, TANT, 20V, 10%
24	707041	2	C5,10	Cap, 2500µf, ALUM, 25V
25	707045	1	C8	Cap, 10,000µf, ALUM, 40V
26	707049	1	C1	Cap, 54,000µf, ALUM, 15V
(28)	720062	1		Washer, MICA
(29)	720010	1		HN, #4-40
(30)	720011	4		HN, #6-32
(31)	720019	1		PHMS, NYL, 6-32 x 1/2
(32)	720020	3		PHMS, 6-32 x 1/2
(33)	720038	1		ITLW, #4
(34)	720041	4		ITLW, #6
(35)	720046	1		Washer, MICA, TO-220
(36)	720053	1		PHMS, NYL, #4-40 x 1/2
(37)	721000	A/R		Heatsink Compound (See Kit P/L)

PARTS LIST - INDICATOR PANEL PCB ASSEMBLY, MODEL 2 (300008F)

ITEM #	PART #	QTY	REFERENCE CODE	STANDARD PART # & EQUIVALENT(S)	DESCRIPTION
(1)	300009	1			Fab, PCB, Indicator Panel, REV D
3	300007	REF			Schematic, Indicator Panel
5	701130	1	U1	74LS139	Dual 2-to-4 Line DEC
6	701138	1	U2	74LS157	Quad 2-to-1 Line MPX
9	702004	1	Q1	2N2907	Trans, PNP
12	703017	9	D1-9	MV5752	LED, RED
15	705022	11	R1-9, R12,13		Res, 220, CF, 1/4W, 5%
16	705049	2	R10,11		Res, 2.2K, CF, 1/4W, 5%
17	705025	2	R14,15		Res, 330Ω, CF, 1/4W, 5%
20	707023	1	C1		Cap, .047µf, Disk Cer, +80 -20%
(25)	716000	A/R			Wire, Solid, Bare, 24 AWG(BUS)

PARTS LIST - SYSTEM ASSEMBLY, MODEL 4 (304000A)

ITEM #	PART #	QTY	DESCRIPTION
1	304005	1	Assy, Helios II Cabinet, Model 4 (See separate parts list.)
2	301000	1	Assy, PCB, Controller (See Model 2)
3	301003	1	Assy, PCB, Formatter (See Model 2)
4	301007	1	Assy, Cable, Cont/Form.
5	301009	1	Assy, Cable, Cont/Cab.
9	722021	1	Flexible Disk Blank
10	727026	1	Cassette, Disk System Test
11	727030	1	PTDOS 1.4 System Disk
13	304004	REF	Drawing Tree
14	300015		Selector, Ø-1
15	300016		Selector, 2-3
16	300017		Selector, 4-5
17	300018		Selector, 6-7

Refer to 4.2.2, Multi-Drive System Configuration

PARTS LIST - CABINET ASSEMBLY, MODEL 4 (304005A)

ITEM #	PART #	QTY	DESCRIPTION	
1	304010	1	Assy, Bezel, Helios II, Model 4	See Separate Parts Lists
2	304020	1	Assy, Base, Helios II, Model 4	
3	304030	1	Assy, Rear Panel, Helios II, Model 4	
4	307000	1	Fab, Top Cover, Helios II	
5	300003	1	Label, Serial, Helios II	
12	716016	A/R	Tubing, Shrink, 3/16 O.D.	
13	718001	1	AC Power Cable, 3 Wire	
14	720003	6	PHMS, 4-40 x 5/16"	
15	720005	2	PHMS, 4-40 x 1/2"	
16	720016	3	PHMS, 6-32 x 1/4"	
17	720018	3	PHMS, 6-32 x 7/16"	
19	720038	6	ITLW, #4	
20	720041	6	ITLW, #6	
21	720051	8	ITLW, #8	
22	720056	2	#4 Kep Nut	
23	720067	3	Washer, Flat, #6	
24	720069	8	PHMS, #8-32 x 5/8"	
25	720070	6	Flatwasher, #4, Zinc	
26	720072	2	Screw, 8-32 x 1", Black Cap	
30	722005	2	Disk Drive, Dual Diskette	
101	PERSCI-100026	4	Momentary Switch, Push.	
102	720058	4	ITLW #12 (Part of 101)	
103	—	4	#12 Hexnut (Part of 101)	
104	—	4	Pushbutton switch cover (Part of 101)	

PARTS LIST - BASE ASSEMBLY, MODEL 4 (304020A)

ITEM #	PART #	QTY	DESCRIPTION
1	304025	1	Assy, PCB, Reg., Helios II, Model 4 (See separate parts list.)
2	302005	1	Transformer, Pwr, Helios II
3	302007	1	Fab, Bracket, Keyswitch
4	302008	1	Fab, Base, Helios II
10	703033	1	Diode, Br Rect, 50PIV, 35A
15	720016	2	PHMS, 6-32 x 1/4"
16	720017	3	PHMS, 6-32 x 5/16"
17	720018	1	PHMS, 6-32 x 7/16"
19	720022	2	PHMS, 6-32 x 3/4"
20	720032	4	PHMS, 8-32 x 1/2"
21	720041	8	ITLW, #6
22	720048	2	Spacer, Rnd, CLR #6 x 3/8"
23	720051	4	ITLW, #8
26	721000	A/R	Heat Sink Compound
27	723006	1	Switch, AC Pwr, Key

PARTS LIST - BEZEL ASSEMBLY, MODEL 4 (304010A)

ITEM #	PART #	QTY	DESCRIPTION
1	306007	1	Fab, Bezel, Helios II, Model 4
2	306009	1	Fab, Logo Panel, Helios II, Model 4
3	306004	2	Fab, Plex Retainer
4	300008	1	Assy, PCB, Indicator Panel (See Model 2)
5	720054	4	Spacer, 1/4" OD, 1/2" Long
6	720068	4	PHMS, 4-40 x 3/4
7	720038	4	ITLW, #4
8	304011	1	Assy, Cable, Ind/Sig, Model 4

PARTS LIST - REAR PANEL, MODEL 4 (304030A)

ITEM #	PART #	QTY	DESCRIPTION
1	305002	1	Fab, Rear Panel, Helios II
2	305004	1	Assy, Cable, AC Pwr Int. ⚠1
3	305006	1	Assy, RFI Filter
4	305008	4	Fab, Cover Plate, D Con.
5	305009	2	Fab, Filter Frame
6	305010	1	Fab, Clamp, Flat Cable
7	305011	2	Fab, Filter Element
8	305012	2	Fab, Filter Screen
9	305013	1	Assy, Fan 12-inch Leads
10	305014	3	Fab, Cover Plate, 50 Pin Con.
13	105033	1	Assy, Fan 3.5-inch Leads
14	720001	14	PHMS, 4-40 x 3/16"
15	720002	4	PHMS, 4-40 x 1/4"
16	720011	8	HN, 6-32
17	720016	2	PHMS, 6-32 x 1/4"
18	720041	8	ITLW, #6
19	720056	2	#4 Kep Nut
20	720057	3	#6 Kep Nut
21	720065	1	Insert, 5/8" Hole Plug
22	720066	4	Hole Plug, 1/4", Blk
23	720038	4	ITLW, #4
25	723013	1	Fuse, Cart, 7A Slo-Blo
26	723018	1	Fuse, Cart, 3.2A Slo-Blo
29	724003	3	Outlet, AC Power, Aux.
30	724005	2	Comm. Block, AC 5 POS
31	724007	2	Fuse Holder, Cart, 3 AG

PARTS LIST - REGULATOR PCB ASSEMBLY (304025A)

ITEM #	PART #	QTY	REFERENCE CODE	STANDARD PART # & EQUIVALENT(S)	DESCRIPTION
(1)	302001	1			Fab, PCB, Regulator, Rev.
2	302002	REF			Schematic, Power Supply, Helios II
(3)	302003	1			Fab, Heat Sink
(4)	302010	1			Assy, Cable, Helios II Pwr, Model 2
(5)	302011	1			Assy, Cable, Helios II Pwr, Model 4
8	701163	1	U1	78H05	Volt Reg, +5 V, 5A
9	701165	1	U2	7905UC, TO-220	Volt Reg, -5 V
10	701167	2	U3,4	7824UC, TO-220	Volt Reg
13	703003	2	D2,3		1N4001 Diode, SIL, Pwr
14	703011	1	D1		1N5231B Diode, ZEN, 5.1V, 1/2 W, 5%
15	703027	1	SCR1	MCR 106-2	SCR, 60 PIV, 4A
16	703029	1	FWB1		Diode, Br Rect, 50 PIV, 1.5A
17	703031	1	FWB2		Diode, Br Rect, 50 PIV, 4A
20	705017	1	R3		Res, 100, CF, 1/4 W, 5%
21	705025	2	R1,2		Res, 330, CF, 1/4 W, 5%
24	707023	4	C2,4,6,9		Cap, .047 µf, Disk Cer, +80 -20%
25	707036	2	C3,7		Cap, 15 µf, TANT, 20 V, 10%
26	707041	2	C5,10,11		Cap, 2500 µf, Alum, 25 V
27	707045	1	C8		Cap, 10 K µf, Alum, 40 V
28	707049	1	C1		Cap, 54 K µf, Alum, 15 V
(31)	720010	1			HN, #4-40
(32)	720011	5			HN, #6-32
(33)	720019	1			PHMS, Nyl, 6-32 x 1/2
(34)	720020	4			PHMS, 6-32 x 1/2
(35)	720038	1			ITLW, #4
(36)	720041	5			ITLW, #6
(37)	720046	1			Washer, MICA, TO-220
(38)	720053	1			PHMS, #4-40 x 1/2
(39)	720062	1			Washer, MICA
42	721000	A/R			Heat Sink Compound

SECTION 10 UPDATES

10.0 PREFACE

Electronics is a very fast moving field. Development of new products, and improvements in the old products proceeds at an unprecedented rate. The continuing development of the Helios II is no exception. Better parts become available and are included, experience yields circuit improvements, and new circuitry is developed. This process generates changes much more frequently than this manual is reprinted. As a result, we include the improvements as blue update sheets, added to this section as they become available. Be sure to integrate this information into the body of the manual before beginning, by making indicated changes in the text, adding or replacing pages, or making notes referring you to the update page.

If you have a question as to the currency of a particular page of text, look in the lower left-hand corner of the page. The initial version of the page will have this corner blank. When the contents of the page have changed, the new version will have "REV A" in this corner; a third version will have "REV B," and so forth. When a whole new page and page number are added, the corner is blank.

A "2" in the corner means 2nd revised printing of the entire manual.