Processor Technology

PARTS LIST: 4KRA STATIC READ/WRITE MEMORY

	Item	Quantity
	4KRA printed circuit board	1
IC pack #1:	DM7400N or SN74LS00N	1
	DM74L00N or SN74LS00N	1
	DM7432N or SN74LS32N	1
	DM8097N or 8T97B	2
	DM8131N	1
	DM8836N	1
	DM8837N	1
MOS IC packs:	AM91L02APC or SYP21L02B	4 packs/ 8 per pack = 32
Bag #1:	6-32x½" pan head screws	3
	6-32 hex nuts	3
	#6 lock washers	3
	LM340T-5.0 IC regulator	1
	100 ohm 5% ¼W resistor	2
	2.2K ohm 5% ¼W resistor	2
	solder	
	jumper wire	
Bag #2:	0.1 mfd disk ceramic capacitor	26
	1 mfd 20VDC tantalum electrolytic capacitor	1
	15 mfd 20VDC tantalum electrolytic capacitor	1
Bag #3:	heatsink	1

PROCESSOR TECHNOLOGY CORPORATION 2465 FOURTH STREET BERKELEY CA 94710 . (415) 549 0857

MOS Cautionary Information

Care is necessary in the handling of the MOS devices used in this kit. Many MOS devices are sensitive to static electricity and leakage voltages which may be present on ungrounded soldering irons, etc. While most of these devices incorporate internal protection against overvoltage damage, it is important to remember that damage is a possibility. Cotton clothing should be worn rather than synthetics when handling MOS devices. Soldering irons having grounded tips (through a three-wire cord) are preferable. Keep the MOS devices inside their anti-static carriers until ready for use. Static sensitivity decreases after the devices are soldered into a circuit card.

1. Board Orientation: The front surface of the printed circuit card is indicated by the word "FRONT" just above the center of the edge connector fingers. All components will be inserted from this side.
2. TTL Device Loading: Refer to the diagram of component location enclosed, and to the section on "Loading DIP Devices." Insert the following I.C.'s in the following locations:

	I.C. type	Location
( )	DM74LOON	IC 41
( )	DM74109N	IC 40
	or DM8214	
	(Note: This I.C. is used only in the 4KRA-1 and 4KRA-2 versions. The location is left blank in the 4KRA-4 version.)	
( )	DM8836N	IC 39
( )	DM8097N	IC 38
( )	DM8097N	IC 37
( )	DM7432N	IC 36
( )	DM7400N	IC 35
( )	DM8131N	IC 34
( )	DM8837N	IC 33

Pin 1 is located at the lower left hand corner of these locations, and is indicated by a small etched "1" on all locations except 35.

3. ( ) Solder these I.C.'s to the card, being careful to avoid solder bridges between pins.

NOTE: Solder at the back side of the board only. All holes are plated through.

4. MOS device loading: Refer to the component location diagram. Positioning the devices so that pin 1 is at the lower left hand corner, insert 91LO2APC I.C.'s starting at location 1 and proceeding across the board to the left. There will be 8, 16, or 32 of these I.C.'s included with the kit:

	kit version	number of I.C.'s	number of rows filled
( )	4KRA-1	8	1
	4KRA-2	16	2
	4KRA-4	32	4

( )After these I.C.'s have been loaded, solder them to the card, being careful to observe the precautions concerning MOS devices as well as avoiding solder bridges.

5. Disc capacitor loading:
   ( ) Insert 0.1 uf disc ceramic capacitors in the following locations:
      ( ) C1 through C30. Note: position C2 through C8 and C10 through C30 so that they fit between the I.C.'s without touching. This requires that the leads be bent as shown in fig. (1). Hold each capacitor in place as it is installed by bending the leads apart underneath the board. Don't be alarmed if you can't find C9; there is no C9.
      ( ) Insert C33 through C42 in their proper positions.
   ( ) Solder the leads of all the capacitors and trim the excess lead lengths as close to the board as possible.

LOADING DIP (DUAL IN-LINE PACKAGE) DEVICES

Most DIP devices have their leads spread so that they can not be dropped straight into the board. They must be "walked in" using the following procedure:

(1) Orient the device properly. Pin 1 is indicated by a small embossed dot on the top surface of the device at one corner. Pins are numbered counterclockwise from pin 1.

(2) Insert the pins on one side of the device into their holes on the printed circuit card. Do not press the pins all the way in, but stop when they are just starting to emerge from the opposite side of the card.

(3) Exert a sideways pressure on the pins at the other side of the device by pressing against them where they are still wide below the bend. Bring this row of pins into alignment with its holes in the printed circuit card and insert them an equal distance, until they begin to emerge.

(4) Press the device straight down until it seats on the points where the pins widen.

(5) Turn the card over and select two pins at opposite corners of the device. Using a fingernail or a pair of long-nose pliers, push these pins outwards until they are bent at a 45 degree angle to the surface of the card. This will secure the device until it is soldered.

SOLDERING TIPS

(1) Use a low-wattage iron — 25 watts is good. Larger irons run the risk of burning the printed-circuit board. Don't try to use a soldering gun, they are too hot.

(2) Use a small pointed tip and keep it clean. Keep a damp piece of sponge by the iron and wipe the tip on it after each use.

(3) Use 60-40 rosin-core solder ONLY. DO NOT use acid-core solder or externally applied fluxes. Use the smallest diameter solder you can get.

NOTE: DO NOT press the top of the iron on the pad or trace. This will cause the trace to "lift" off of the board which will result in permanent damage.

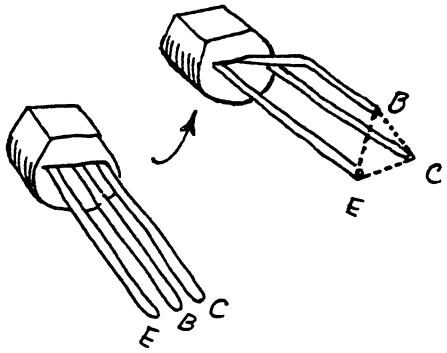
(4) In soldering, wipe the tip, apply a light coating of new solder to it, and apply the tip to both parts of the joint, that is, both the component lead and the printed-circuit pad. Apply the solder against the lead and pad being heated, but not directly to the tip of the iron. Thus, when the solder melts the rest of the joint will be hot enough for the solder to "take," (i.e., form a capillary film).

(5) Apply solder for a second or two, then remove the solder and keep the iron tip on the joint. The rosin will bubble out. Allow about three or four bubbles, but don't keep the tip applied for more than ten seconds.

(6) Solder should follow the contours of the original joint. A blob or lump may well be a solder bridge, where enough solder has been built upon one conductor to overflow and "take" on the adjacent conductor. Due to capillary action, these solder bridges look very neat, but they are a constant source of trouble when boards of a high trace density are being soldered. Inspect each integrated circuit and component after soldering for bridges.

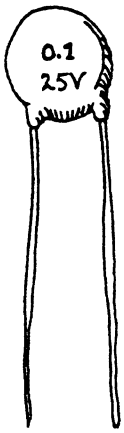
(7) To remove solder bridges, it is best to use a vacuum "solder puller" if one is available. If not, the bridge can be reheated with the iron and the excess solder "pulled" with the tip along the printed circuit traces until the lump of solder becomes thin enough to break the bridge. Braid-type solder remover, which causes the solder to "wick up" away from the joint when applied to melted solder, may also be used.

IDENTIFICATION OF COMPONENTS

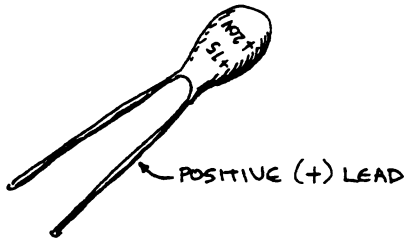


transistor - TO-92 package (plastic)

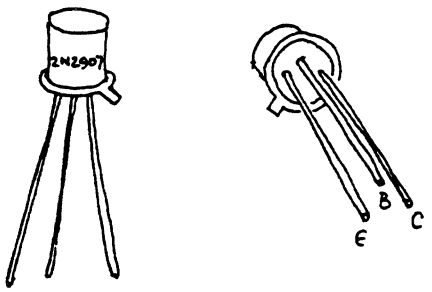
transistor - TO-18 package (metal can)

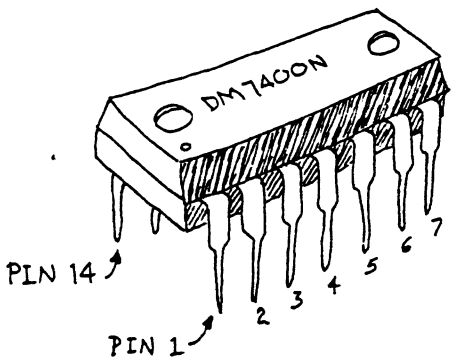


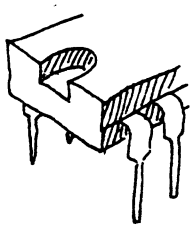
ceramic disc capacitor



dipped tantalum electrolytic capacitor

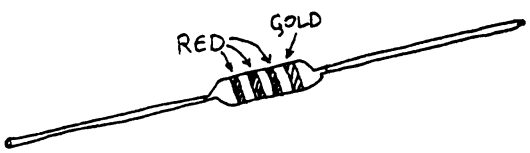






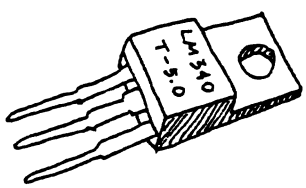
NOTE: PIN 1 MAY BE INDICATED BY CORNER DOT OR CUT-OUT.

dual-inline-package (DIP) integrated circuit
8,14,16,24 or 40 pins (14 pin shown)



carbon film resistor 5% (gold) or 10% (silver)

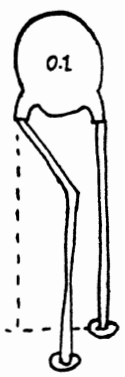
metal film 1% precision resistor



regulator IC or power transistor (TO-220)

6. Tantalum capacitor installation:
   ( ) Install 1.0 uf, 20 volt tantalum capacitors C31 and C32 as shown on the component location diagram. The positive lead of these capacitors, as indicated by a "+" on the body of the capacitor, is connected to the printed circuit traces on the top side of the board.
   ( ) Bend the leads outwards underneath the board and solder. Trim the leads as close to the board as possible.
   ( ) Install the 15 uf, 20 volt tantalum capacitor C43 in the location shown in the component location diagram. The positive lead connects to the printed circuit trace on the bottom side of the card, through the hole which has a square area around it on the top side.
   ( ) Bend and solder the leads to this capacitor as above. Trim the leads as close to the board as possible.

fig. 1 - lead formation,



capacitors C2-C8, C10-C30

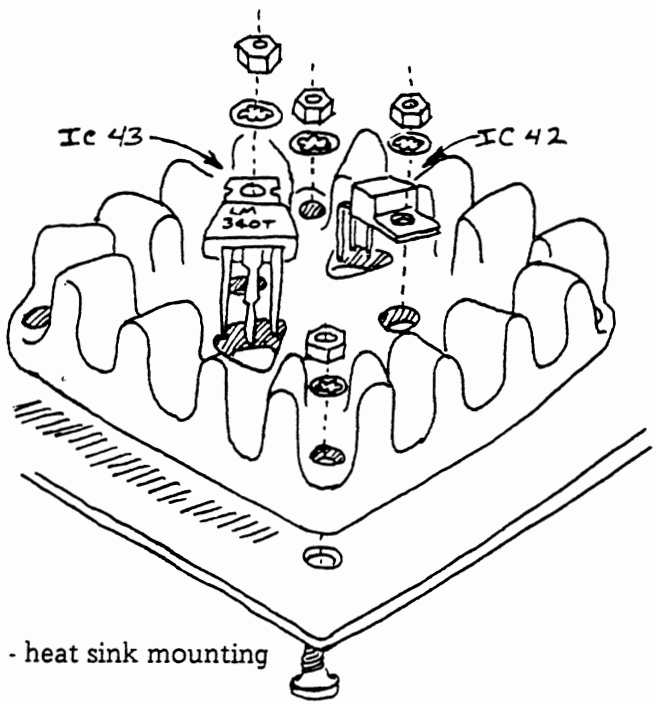


fig. 2 - heat sink mounting

7. Resistor Installation: Referring to the component location diagram, install resistors R1 through R4 as follows:

	resistor value	color code	location
( ) ( )	2,200 ohms	red-red-red-gold	R1, R2
( ) ( )	100 ohms	brown-black-brown-gold	R3, R4

   ( ) Solder and trim leads.

8. Heat Sink Installation:
   ( ) Install the black, finned heat sink on the top side of the card, flat face down, with all holes lined up. Secure the heat sink to the card with the two 6-32 machine screws, using lockwashers underneath the nuts. Install the screws with their heads on the underside of the card. Do not tighten screws completely until regulator I.C.'s are installed.
9. Regulator Installation: Refer to Fig. 2. Position I.C.'s 43 and 42 (LM340T-5.0) over their mounting locations on the heat sink and observe how the leads must be bent to engage their holes on the card. The center lead must be bent at a point approximately 0.2 inches further away from the body of the regulator. Use of silicone heatsink compound is recommended between the regulator I.C.'s and the heatsink.
   ( ) Bend the leads and adjust them, if necessary, so that the regulators may be mounted to the heat sink *without the leads touching the heat sink.*
   ( ) Secure the regulators with 6-32 machine screws, using lockwashers under the nuts. Insert the screws from the bottom side of the card.
   ( ) Solder the leads of the regulators and clip the excess off as close to the card as possible.

10. ( ) Install Augat receptacle pins in address-select holes as follows:
    ( ) Wedge the board between two objects so that it stands slightly off vertical with the top side up.
    ( ) The Augat receptacle pins are mounted on a DIP-style metal carrier. Pull off one pin and insert it from the top side of the board into one of the address-selection holes. The fit will be loose.
    ( ) Carefully solder the pin to the pad. The pin will end up out of perpendicular to the board.
    ( ) Insert a component lead into the receptacle. Reheat the solder and, using the component lead, adjust the position of the receptacle until it is more nearly perpendicular to the board. Allow the solder to solidify while holding the pin as steady as possible. A mottled or crystallized solder joint indicates a "cold joint" and should be reheated.
    ( ) When all the pins have been installed, check carefully for cold joints or solder bridges.

4KRA — OPERATING RESTRICTIONS

1. Take care not to attach clip leads to the top edge of the card when the unit is powered. This will short the +8 volt bus to ground.
2. Due to regulator current limitations, no more than 8 additional standard 2102 - type RAM chips may be installed on a —1 or —2 versions. Low power units, available from Processor Technology, are necessary for operation of a full card (4K).
3. If RAM chips with worst case access times of greater than 500 nsec and less than 1.0 microsecond are used, the board must be strapped for one waiting state.

   If RAM chips with worst case access times of 1.0 to 1.5 microseconds are used, the board must be strapped for two waiting states.

4KRA
ADDRESS RANGE SELECTION

The starting address of the 4KRA is selected by the connection of four jumpers at the lower right-hand corner of the board. Each of the four round pads on the upper row has two oval pads below it. The left-hand pad of the pair on the bottom row is connected to a trace on the top side of the card. This set of pads will be designated H. The other set of pads, which connect to the ground trace on the bottom side of the board, will be designated L. (See fig. 4).

Using short lengths of bare wire, #24 or 26, make the connections as indicated in the chart below. Only the indicated addresses are available for starting addresses; no intermediate addresses may be used.

Starting Address					
Decimal	Octal	A15	A14	A13	A12
0	0	L	L	L	L
4,096	10,000	L	L	L	H
8,192	20,000	L	L	H	L
12,288	30,000	L	L	H	H
16,384	40,000	L	H	L	L
20,480	50,000	L	H	L	H
24,576	60,000	L	H	H	L
28,672	70,000	L	H	H	H
32,768	100,000	H	L	L	L
36,864	110,000	H	L	L	H
40,960	120,000	H	L	H	L
45,056	130,000	H	L	H	H
49,152	140,000	H	H	L	L
53,248	150,000	H	H	L	H
57,344	160,000	H	H	H	L
61,440	170,000	H	H	H	H

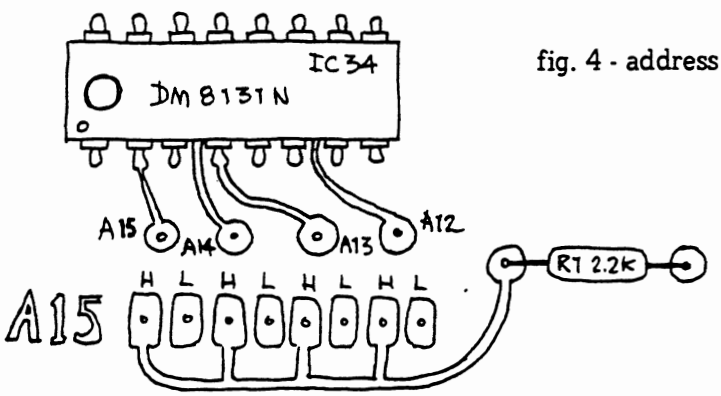


fig. 4 - address selection jumpers

WAIT STATE SELECTION (See fig. 3)

Since the RAM chips shipped by Processor Technology are specified for operation at 500 nanoseconds, no waiting time is required. The circuit is set up for this condition by connecting a jumper wire between the "W" pad above I.C.39 and the "N" pad to its left just next to the 2.2K resistor.

If slower RAM chips are installed in a −1 or −2 card, the waiting time may have to be enabled. To do this, the jumper is removed from "N" to "W", and a jumper is installed from "Y" to "W". The number of wait states, each .5 micro-second, is determined by the numbered pad (2 or 1) connected to the "W" pad below the I.C. 40. If waiting time is enabled, one of these must be connected.

W = wait
N = no
Y = yes

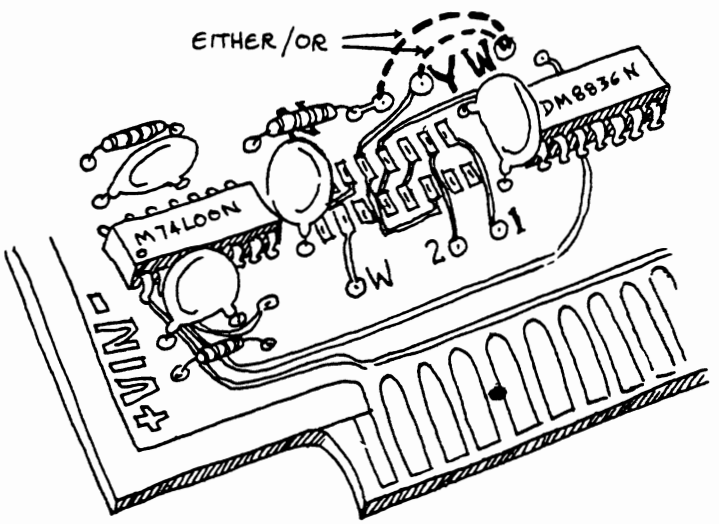


fig. 3 - optional wait state jumpers
connect from "W" to "N" for normal operation
connect from "W" to "Y" for wait states (IC 40 must be installed)

Address lines AØ through A9 are connected directly from the bus to the 10 address input pins of each random-access memory (RAM) chip on this module. Likewise, each line of the data-out bus DO Ø through 7 connects directly to one chip in each "page" of memory represented by eight chips. Each chip in the page therefore stores one bit of the word.

Only one page is selected at a time, however, and that page alone reads information to or writes information from the data busses. The data outputs of the RAMs are "tri-state" types which "float" in a high-impedance condition when they are not selected. They may therefore be connected in parallel from one page to the next, so that only that bit of the selected page sends data out.

Data from the RAMs is sent out to the 8097 tri-state bus drivers IC37 and IC38. These drivers are enabled only if the output from pin 6 of IC36 is low. IC36 is a 7432 positive-OR gate which can also be viewed as a negative-AND gate, whose output will be "low" only if both inputs are "low". Thus, the output pin 6 will be "low" only if pins 1, 2, and 5 are also "low".

This condition exists when (a) SMEMR is "high", (b) PDBIN is "high", and (c) the output pin 9 of comparator IC34 is "low". (a) and (b) occur when the processor requests memory data. (c) occurs when the address bits on address bus line A12 through A15 match the setup of the jumpers 12 through 15. Thus, the first two conditions occur for any memory read operation, but condition (c) occurs only when this particular memory module is addressed.

Address bits A1Ø and A11 choose the page of memory to be accessed. They are decoded into one of four outputs by IC33 and IC35. A "select page" signal from IC35 is a "low" level and may occur on only one of its outputs at a time. Each output of IC35 is connected to all the "chip enable" pins of a page of RAM.

Thus, A12 through A15 select the card, A1Ø and A11 select the page, and AØ through A9 select the word within the page to be read. The data is presented to the bus drivers IC37 and IC38, which gate the data out to the DI bus when that data is requested by the processor (SMEMR and PDBIN).

The RAM chips supplied with the 4KRA are guaranteed to provide settled data within one CPU cycle time (500 nanoseconds). When such fast RAMs are used, the "W" jumper which selects waiting time is connected to the "N" terminal, which connects a "high" level to pin 12 of IC38. When this section of the bus driver is enabled ("low" level on pin 15) by a "low" level on the output (pin 9) of the 8131 comparator IC34, the XRDY signal to the bus is driven "high". Therefore, the memory card sends a "ready" signal back as soon as it is addressed. The data will be ready before the processor is.

If, however, other 2102-type RAM chips are used having slower access time, one or two "wait" cycles must be allowed to pass before the CPU is allowed to accept the data. 74109 IC40 comprises a two-bit shift register which may be selected to give a "high" level at pin 6 after one or two PSYNC pulses. The 74109 IC40 is a dual J-K flip-flop with positive clock. The outputs of each section change on the low- to-high transition of the clock signal depending on the condition of the J and $\overline{K}$ inputs. The changes occur according to the following table:

J low, $\overline{K}$ high ..... no change
J high, $\overline{K}$ high ..... Q goes "high"
J low, $\overline{K}$ low ..... Q goes "low"
J high, $\overline{K}$ low ..... Q changes to the opposite level.

When PSYNC goes "high" section 2 is reset, if it was not already reset. Pin 6 goes "low" and since both J and $\overline{K}$ inputs to section 1 are now "low", section 1 Q goes "low" on the high-to-low transition of $\phi 2$ clock.

When PSYNC goes "low" section 2 may change state on the next high-to-low $\phi 2$ transition. If the J input (pin 2) is high, section 2 will be "set" on the next high-to-low transition of $\phi 2$. This will happen if the jumper is connected from W to "1". The same clock transition will cause section 1 to change state. Note that the "old" data at the output of section 2 is what counts for this clock transition. The "new" data does not appear at the outputs until some time after the clock transition.

Now both sections are set. Since pin 2 is now "low" and pin 3 "high", section 2 will remain this way until PSYNC resets it. The same conditions hold true at the inputs to section 1, so it will remain without changing state.

If the jumper was connected to "2" (pin 10), then section 2 would not set on the first clock pulse after PSYNC. Section 1 would still change state on this transition, however. The conditions would then be correct to allow section 2 to set on the next clock pulse. Section 1 would change state again on that transition. The two sections would then "lock up" with section 1 reset and section 2 set.

Thus, if IC40 is installed and the wait states are jumpered in, pin 6 will go "high" on the first high-to-low transition of $\phi 2$ after PSYNC if 1 wait state is selected. Pin 6 will go "high" on the second high-to-low transition of $\phi 2$ after PSYNC if 2 wait states have been selected. Pin 6 will in either case remain "high" until the next PSYNC.

The "write" sequence of events is similar to the "read" sequence except that "MWRI" is high instead of "SMEMR". The output drivers IC 37 and IC 38 are disabled, and the low-active "write" input of the RAMs is driven "low" for the duration of MWRI pulse. The timing of this pulse is controlled by the CPU.

In order for this to happen, pin 8 of IC 41 must be "low". IC 41 is wired as a latch which may be set or reset by the PROT or UN PROT inputs when the board is selected (pin 9 of IC 34 "low"). The resistor-capacitor networks guard against noise pulses setting the latch. When the latch is set by the "PROT" input, pin 8 is "high" and pin 6 is "low". This inhibits the "write" pulse and sends a low-active PS signal out via IC 38. This signal notifies the CPU that the page of memory is protected.

Since no "master clear" signal exists on the card, it is necessary to issue the proper "protect" and "unprotect" signals to memory when first powering the computer.

4K MEMORY TEST PROGRAM

The 4K memory test program provides an effective test of any 4K segment of memory. The incrementing pattern used for the test will find errors in any but the most cantankerous, pattern sensitive, dynamic memory.

The test is performed in two segments, write and read. Write begins at the bottom of the 4K address (LOAD) writing zero and then writes an incrementing bit pattern to the "top." After each location is then read and compared to its proper pattern, and if no errors are found, the starting pattern is incremented and the test is performed again.

This read, write sequence continues until an error is found or the machine is halted. If an error is found all information relating to the error is saved in locations 000–006.

ADDRESS

5	High Address Error Pointer
4	Low Address Error Pointer
3	Write Data
2	Read Data (Error)
1	Page Down Count

To use the program clear memory locations 0000–0006 and load the hex code starting from location 0007. As the code is entered check the address for each input as a test of proper code and location. After all code is entered check each location for the proper bits.

Then press the reset and run switches and the test should then proceed as indicated by the address lights.

NOTE: A full test of all 256 bit patterns to all 4096 locations takes about 30 seconds with fast memory. This test should be repeated for one hour with the cover to the computer in place.

Processor Technology Corp.
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APPENDIX I

```
0000                    0000 *    <<< 4K MEMORY TEST PROGRAM    >>>
0000                    0001 *
0000                    0002 *  ASSEMBLED ON SOFTWARE PACKAGE #1
0000                    0003 *
0000                    0004 *    PROCESSOR TECHNOLOGY CORP.
0000                    0005 *    2465 FOURTH STREET
0000                    0006 *    BERKELEY, CALIF.    94710
0000                    0007 *
0000                    0008 LOAD EQU 4096
0000                    0009 TOP EQU 32
0000                    0010 SP EQU 6
0000                    0015 *
0000                    0020  ORG 7
0007                    0025 *
0007 31 06 00           0030 START   LXI  SP, 6   SET UP ERROR CATCH
000A AF                 0035         XRA  A       CLEAR REG A
000B 47                 0040         MOV  B,A     CLEAR B
000C                    0045 *
000C 21 00 10           0050 OVER    LXI  H, LOAD  LOAD ADDRESS
000F 48                 0053         MOV  C,B     FIRST WRITE DATA
0010 71                 0055 WRITE   MOV  M,C     PUT IN MEMORY
0011 23                 0060         INX  H       NEXT ADDR
0012 0C                 0065         INR  C       NEXT WRITE DATA
0013 7C                 0070         MOV  A,H
0014 FE 20              0075         CPI  TOP     IS H OVER THE TOP?
0016 C2 10 00           0080         JNZ  WRITE   IF NOT THEN MORE
0019                    0081 *
0019                    0082 *    READ TEST ROUTINE
0019                    0083 *
0019 78                 0085         MOV  A,B     GET FIRST WRITE DATA
001A 0E 04              0090         MVI  C,4     C HOLDS PAGE COUNT
001C 21 00 10           0095         LXI  H, LOAD  LOAD ADDRESS
001F                    0096 *
001F 11 00 04           0100 NEXT    LXI  D, 1024  D-E COUNT K'S
0022 BE                 0110 READ    CMP  M        IS DATA OK?
0023 C2 3B 00           0112         JNZ  ERROR IF NOT CATCH IT
0026 1D                 0115         DCR  E
0027 C2 2E 00           0118         JNZ  OKTES
002A 15                 0120         DCR  D       ANOTHER PAGE DOWN
002B CA 33 00           0125         JZ   ONEK    COUNT K'S
002E                    0133 *
002E 23                 0135 OKTES   INX  H       NEXT ADDRESS
002F 3C                 0140         INR  A
0030 C3 22 00           0145         JMP  READ
0033                    0146 *
0033 0D                 0150 ONEK    DCR  C       ONE MORE K DOWN
0034 C2 1F 00           0155         JNZ  NEXT    MORE K'S TO COUNT
0037 04                 0157         INR   B
0038 C3 0C 00           0160         JMP  OVER
003B                    0170 *
003B                    0175 *      ERROR STUFF ROUTINE
003B                    0180 *
003B                    0185 *   ADDRESS
003B                    0186 *    5  HAS HIGH ERROR ADDR
003B                    0187 *    4  HAS LOW   "  "
003B                    0188 *    3  HAS WRITE DATA
003B                    0189 *    2  HAS READ DATA (ERROR)
003B                    0190 *    0  HAS PAGE DOWN COUNT
003B                    0210 *
003B                    0215 *
003B E5                 0216 ERROR   PUSH  H    STUFF ADDRESSES
003C 57                 0220         MOV  D,A   GET WRITE DATA
003D 5E                 0225         MOV  E,M   GET READ DATA
003E D5                 0230         PUSH  D    PUT ON STACK
003F C5                 0235         PUSH  B    ALL OF IT
0040 76                 0240 AHHHH   HLT        STOP THIS NONSENSE
0041                    0245 *
0041                    0250 *
```

JUMP

C3	JMP	Adr
C2	JNZ	
CA	JZ	
D2	JNC	
DA	JC	
E2	JPO	
EA	JPE	
F2	JP	
FA	JM	
E9	PCHL	

CALL

CD	CALL	Adr
C4	CNZ	
CC	CZ	
D4	CNC	
DC	CC	
E4	CPO	
EC	CPE	
F4	CP	
FC	CM	

RETURN

C9	RET
C0	RNZ
C8	RZ
D0	RNC
D8	RC
E0	RPO
E8	RPE
F0	RP
F8	RM

RESTART

C7	RST	0
CF	RST	1
D7	RST	2
DF	RST	3
E7	RST	4
EF	RST	5
F7	RST	6
FF	RST	7

ROTATE†

07	RLC
0F	RRC
17	RAL
1F	RAR

CONTROL

00	NOP
76	HLT
F3	DI
FB	EI

MOVE IMMEDIATE

06	MVI	B,	D8
0E	MVI	C,	
16	MVI	D,	
1E	MVI	E,	
26	MVI	H,	
2E	MVI	L,	
36	MVI	M,	
3E	MVI	A,	

Acc IMMEDIATE*

C6	ADI	D8
CE	ACI	
D6	SUI	
DE	SBI	
E6	ANI	
EE	XRI	
F6	ORI	
FE	CPI	

LOAD IMMEDIATE

01	LXI	B,	D16
11	LXI	D,	
21	LXI	H,	
31	LXI	SP,	

DOUBLE ADD†

09	DAD	B
19	DAD	D
29	DAD	H
39	DAD	SP

STACK OPS

C5	PUSH	B
D5	PUSH	D
E5	PUSH	H
F5	PUSH	PSW
C1	POP	B
D1	POP	D
E1	POP	H
F1	POP	PSW*
E3	XTHL	
F9	SPHL	

SPECIALS

EB	XCHG	
27	DAA*	
2F	CMA	
37	STC†	
3F	CMC†	

INPUT/OUTPUT

D3	OUT	D8
DB	IN	D8

MOVE

40	MOV	B,B	
41	MOV	B,C	
42	MOV	B,D	
43	MOV	B,E	
44	MOV	B,H	
45	MOV	B,L	
46	MOV	B,M	
47	MOV	B,A	
48	MOV	C,B	
49	MOV	C,C	
4A	MOV	C,D	
4B	MOV	C,E	
4C	MOV	C,H	
4D	MOV	C,L	
4E	MOV	C,M	
4F	MOV	C,A	
50	MOV	D,B	
51	MOV	D,C	
52	MOV	D,D	
53	MOV	D,E	
54	MOV	D,H	
55	MOV	D,L	
56	MOV	D,M	
57	MOV	D,A	

MOVE (cont)

58	MOV	E,B
59	MOV	E,C
5A	MOV	E,D
5B	MOV	E,E
5C	MOV	E,H
5D	MOV	E,L
5E	MOV	E,M
5F	MOV	E,A
60	MOV	H,B
61	MOV	H,C
62	MOV	H,D
63	MOV	H,E
64	MOV	H,H
65	MOV	H,L
66	MOV	H,M
67	MOV	H,A
68	MOV	L,B
69	MOV	L,C
6A	MOV	L,D
6B	MOV	L,E
6C	MOV	L,H
6D	MOV	L,L
6E	MOV	L,M
6F	MOV	L,A
70	MOV	M,B
71	MOV	M,C
72	MOV	M,D
73	MOV	M,E
74	MOV	M,H
75	MOV	M,L

77	MOV	M,A
78	MOV	A,B
79	MOV	A,C
7A	MOV	A,D
7B	MOV	A,E
7C	MOV	A,H
7D	MOV	A,L
7E	MOV	A,M
7F	MOV	A,A

ACCUMULATOR*

80	ADD	B
81	ADD	C
82	ADD	D
83	ADD	E
84	ADD	H
85	ADD	L
86	ADD	M
87	ADD	A
88	ADC	B
89	ADC	C
8A	ADC	D
8B	ADC	E
8C	ADC	H
8D	ADC	L
8E	ADC	M
8F	ADC	A
90	SUB	B
91	SUB	C
92	SUB	D
93	SUB	E
94	SUB	H
95	SUB	L
96	SUB	M
97	SUB	A
98	SBB	B
99	SBB	C
9A	SBB	D
9B	SBB	E
9C	SBB	H
9D	SBB	L
9E	SBB	M
9F	SBB	A
A0	ANA	B
A1	ANA	C
A2	ANA	D
A3	ANA	E
A4	ANA	H
A5	ANA	L
A6	ANA	M
A7	ANA	A
A8	XRA	B
A9	XRA	C
AA	XRA	D
AB	XRA	E
AC	XRA	H
AD	XRA	L
AE	XRA	M
AF	XRA	A
B0	ORA	B
B1	ORA	C
B2	ORA	D
B3	ORA	E
B4	ORA	H
B5	ORA	L
B6	ORA	M
B7	ORA	A
B8	CMP	B
B9	CMP	C
BA	CMP	D
BB	CMP	E
BC	CMP	H
BD	CMP	L
BE	CMP	M
BF	CMP	A

INCREMENT**

04	INR	B
0C	INR	C
14	INR	D
1C	INR	E
24	INR	H
2C	INR	L
34	INR	M
3C	INR	A
03	INX	B
13	INX	D
23	INX	H
33	INX	SP

DECREMENT**

05	DCR	B
0D	DCR	C
15	DCR	D
1D	DCR	E
25	DCR	H
2D	DCR	L
35	DCR	M
3D	DCR	A
0B	DCX	B
1B	DCX	D
2B	DCX	H
3B	DCX	SP

LOAD/STORE

0A	LDAX	B
1A	LDAX	D
2A	LHLD	Adr
3A	LDA	Adr
02	STAX	B
12	STAX	D
22	SHLD	Adr
32	STA	Adr

PSEUDO INSTRUCTION

ORG	Adr	
END		
EQU	D16	
DS	D16	
DB	D8	[,]
DW	D16	[,]

CONSTANT DEFINITION

0BDH	Hex
1AH	
105D	Decimal
105	
72O	Octal
72Q	
11011B	Binary
00110B	
'TEST'	ASCII
'A' 'B'	

OPERATORS

+

STANDARD SETS

A	SET	7
B	SET	0
C	SET	1
D	SET	2
E	SET	3
H	SET	4
L	SET	5
M	SET	6
SP	SET	6
PSW	SET	6

D8 constant, or logical arithmetic expression that evaluates to an 8 bit data quantity.

all Flags (C,Z,S,P) affected

D16 = constant, or logical/arithmetic expression that evaluates to a 16 bit data quantity.

† = only CARRY affected

Adr = 16 bit address

** = all Flags except CARRY affected; (exception: INX & DCX affect no Flags)

00	NOP		28	---		50	MOV	D,B	78	MOV	A,B	A0	ANA	B	C8	RZ		F0	RP
01	LXI	B,D16	29	DAD	H	51	MOV	D,C	79	MOV	A,C	A1	ANA	C	C9	RET		F1	POP PSW
02	STAX	B	2A	LHLD	Adr	52	MOV	D,D	7A	MOV	A,D	A2	ANA	D	CA	JZ		F2	JP Adr
03	INX	B	2B	DCX	H	53	MOV	D,E	7B	MOV	A,E	A3	ANA	E	CB	---		F3	DI
04	INR	B	2C	INR	L	54	MOV	D,H	7C	MOV	A,H	A4	ANA	H	CC	CZ	Adr	F4	CP Adr
05	DCR	B	2D	DCR	L	55	MOV	D,L	7D	MOV	A,L	A5	ANA	L	CD	CALL	Adr	F5	PUSH PSW
06	MVI	B,D8	2E	MVI	L,D8	56	MOV	D,M	7E	MOV	A,M	A6	ANA	M	CE	ACI	D8	F6	ORI D8
07	RLC		2F	CMA		57	MOV	D,A	7F	MOV	A,A	A7	ANA	A	CF	RST	1	F7	RST 6
08	---		30	---		58	MOV	E,B	80	ADD	B	A8	XRA	B	D0	RNC		F8	RM
09	DAD	B	31	LXI	SP,D16	59	MOV	E,C	81	ADD	C	A9	XRA	C	D1	POP	D	F9	SPHL
0A	LDAX	B	32	STA	Adr	5A	MOV	E,D	82	ADD	D	AA	XRA	D	D2	JNC	Adr	FA	JM Adr
0B	DCX	B	33	INX	SP	5B	MOV	E,E	83	ADD	E	AB	XRA	E	D3	OUT	D8	FB	EI
0C	INR	C	34	INR	M	5C	MOV	E,H	84	ADD	H	AC	XRA	H	D4	CNC	Adr	FC	CM Adr
0D	DCR	C	35	DCR	M	5D	MOV	E,L	85	ADD	L	AD	XRA	L	D5	PUSH	D	FD	---
0E	MVI	C,D8	36	MVI	M,D8	5E	MOV	E,M	86	ADD	M	AE	XRA	M	D6	SUI	D8	FE	CPI D8
0F	RRC		37	STC		5F	MOV	E,A	87	ADD	A	AF	XRA	A	D7	RST	2	FF	RST 7
10	---		38	---		60	MOV	H,B	88	ADC	B	B0	ORA	B	D8	RC			
11	LXI	D,D16	39	DAD	SP	61	MOV	H,C	89	ADC	C	B1	ORA	C	D9	---			
12	STAX	D	3A	LDA	Adr	62	MOV	H,D	8A	ADC	D	B2	ORA	D	DA	JC	Adr		
13	INX	D	3B	DCX	SP	63	MOV	H,E	8B	ADC	E	B3	ORA	E	DB	IN	D8		
14	INR	D	3C	INR	A	64	MOV	H,H	8C	ADC	H	B4	ORA	H	DC	CC	Adr		
15	DCR	D	3D	DCR	A	65	MOV	H,L	8D	ADC	L	B5	ORA	L	DD	---			
16	MVI	D,D8	3E	MVI	A,D8	66	MOV	H,M	8E	ADC	M	B6	ORA	M	DE	SBI	D8		
17	RAL		3F	CMC		67	MOV	H,A	8F	ADC	A	B7	ORA	A	DF	RST	3		
18	---		40	MOV	B,B	68	MOV	L,B	90	SUB	B	B8	CMP	B	E0	RPO			
19	DAD	D	41	MOV	B,C	69	MOV	L,C	91	SUB	C	B9	CMP	C	E1	POP	H		
1A	LDAX	D	42	MOV	B,D	6A	MOV	L,D	92	SUB	D	BA	CMP	D	E2	JPO	Adr		
1B	DCX	D	43	MOV	B,E	6B	MOV	L,E	93	SUB	E	BB	CMP	E	E3	XTHL			
1C	INR	E	44	MOV	B,H	6C	MOV	L,H	94	SUB	H	BC	CMP	H	E4	CPO	Adr		
1D	DCR	E	45	MOV	B,L	6D	MOV	L,L	95	SUB	L	BD	CMP	L	E5	PUSH	H		
1E	MVI	E,D8	46	MOV	B,M	6E	MOV	L,M	96	SUB	M	BE	CMP	M	E6	ANI	D8		
1F	RAR		47	MOV	B,A	6F	MOV	L,A	97	SUB	A	BF	CMP	A	E7	RST	4		
20	---		48	MOV	C,B	70	MOV	M,B	98	SBB	B	C0	RNZ		E8	RPE			
21	LXI	H,D16	49	MOV	C,C	71	MOV	M,C	99	SBB	C	C1	POP	B	E9	PCHL			
22	SHLD	Adr	4A	MOV	C,D	72	MOV	M,D	9A	SBB	D	C2	JNZ	Adr	EA	JPE	Adr		
23	INX	H	4B	MOV	C,E	73	MOV	M,E	9B	SBB	E	C3	JMP	Adr	EB	XCHG			
24	INR	H	4C	MOV	C,H	74	MOV	M,H	9C	SBB	H	C4	CNZ	Adr	EC	CPE	Adr		
25	DCR	H	4D	MOV	C,L	75	MOV	M,L	9D	SBB	L	C5	PUSH	B	ED	---			
26	MVI	H,D8	4E	MOV	C,M	76	HLT		9E	SBB	M	C6	ADI	D8	EE	XRI	D8		
27	DAA		4F	MOV	C,A	77	MOV	M,A	9F	SBB	A	C7	RST	0	EF	RST	5		

D8 = constant, or logical/arithmetic expression that evaluates to an 8 bit data quantity.

D16 = constant, or logical/arithmetic expression that evaluates to a 16 bit data quantity.

Adr = 16 bit address

HEX-ASCII TABLE

Printing		Characters	
30	0	40	@
31	1	20	space
32	2	21	!
33	3	22	"
34	4	23	#
35	5	24	$
36	6	25	%
37	7	26	&
38	8	27	'
39	9	28	(
		29	)
41	A	2A	*
42	B	2B	+
43	C	2C	,
44	D	2D	-
45	E	2E	.
46	F	2F	/
47	G	3A	:
48	H	3B	;
49	I	3C	<
4A	J	3D	=
4B	K	3E	>
4C	L	3F	?
4D	M	5B	[
4E	N	5C	\
4F	O	5D	]
50	P	5E	↑ (^)
51	Q	5F	← (-)
52	R		
53	S		
54	T		
55	U		
56	V		
57	W		
58	X		
59	Y		
5A	Z		

HEX-ASCII TABLE

Non-Printing

00	NULL
07	BELL
09	TAB
0A	LF
0B	VT
0C	FORM
0D	CR
11	X-ON
12	TAPE
13	X-OFF
14	
1B	ESC
7D	ALT MODE
7F	RUB OUT

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CORRECTIONS – 2KRO AND 4KRA

In an effort to make our devices completely pin-compatible with the original manufacturer's equipment, a design error of the original equipment was incorporated into the design of our cards. The signal which is driving pin 72, PRDY, should instead be driving pin 3, XRDY; Method 2. This correction may be accomplished using one of two methods (BUT NOT BOTH).

MASTER BOARD CORRECTION – METHOD 1

( ) Locate the cable wire going to point 72 on the Mother Board within the computer.

( ) Remove the wire from point 72 and solder into point 3 on the Mother Board.

PROCESSOR TECHNOLOGY BOARD CORRECTION – METHOD 2

To correct this, refer to the enclosed diagram and perform the following modifications:

( ) Locate pin 72 on the back side of the board. Cut the trace between this pin and the feed-through hole above it.

( ) Cut a piece of solid insulated wire, 24 gauge or smaller, long enough to reach from this feed-through to pin 3.

( ) Strip one end of this wire to a length of 1/8 inch and tin it. Solder this end from the top side of the card to the feed-through hole.

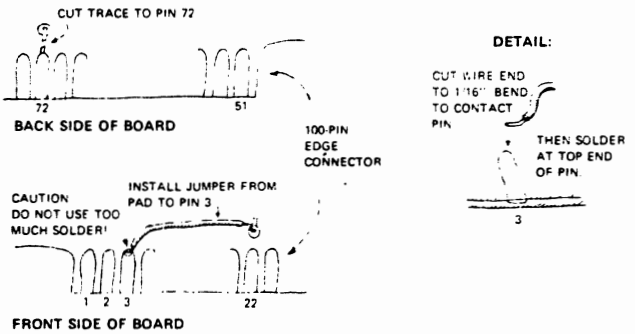
( ) Strip the other end of the wire to a length of 1/16 inch and tin it.

( ) Bending the wire so that it will lie close to the card, position this end so that it will lie in contact with the rounded end of pin 3.

( ) Using very little solder and taking care to avoid spreading solder too far down the pin, tin a small area at the rounded end of pin 3.

( ) Place the wire end in contact with this tinned area of pin 3 and heat the two with the soldering iron until the solder melts. Remove the iron and allow the solder to solidify while holding the wire steady.
NOTE: When soldering to gold-plated printed-circuit connector contacts it is essential that the soldering iron not make contact with any area which will enter the connector. Solder coatings cannot be removed from gold and defeat the purpose of the gold plating, which is to prevent oxidation of contacts.

( ) On the device schematic diagram, change pin 72, PRDY to pin 3, XRDY.



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Technical Bulletin

TB 101

PROBLEM

The unpredictability of power failure in a volatile memory system can result in a loss of irreplaceable information. Hours of work, as represented by a nicely debugged program, can be wiped out in an instant with a power failure lasting only long enough for the lights to blink.

SOLUTION

The simple modification described in this bulletin can prevent the loss of stored data during loss-of-power and power interrupt conditions. This is accomplished with the use of low-power 91L02A Memory I.C.'s provided with the Processor Technology 4KRA. These I.C.'s will operate in a low power stand-by mode which further reduces energy requirements.

In the stand-by mode, the memory supply power is reduced to approximately 2 volts, which is provided by a storage battery. The battery is continuously charged during normal operation at a 10 to 30 hour rate from the CPU Display and Control Panel Supply, and automatically changes to the stand-by mode when normal power is interrupted or removed.

Data integrity will be retained as long as the stand-by power is available; each 4K memory card consumes slightly over one watt of power. If a 4 Amp Hr battery is used, it will provide from five to ten hours of stand-by power. This time can be extended by the use of a battery with greater storage capacity.

Retaining data with stand-by power will be useless if, when power is restored to the CPU, a random operation rewrites retained data improperly. This problem is solved by using an initializing circuit to set the memory "protect" mode. This is accomplished with an RC network: Parallel a .1 Mfd disc capacitor with a 10K resistor. Ground one end and connect the other end to pin 10 of IC 41. Refer to Figures 2 and 3.

NOTE: If some applications require a "non-protect" initializing, this can be accomplished by connecting the same network to pin 4 instead of pin 10 of IC 41. A simple switch could be used to implement mode selection from "protect" to "non-protect" power-up initialization.

LIMITATIONS

The battery backup supply described in this bulletin is not by itself adequate for complete power-fail protection. When battery backup is used, the 4KRA memory modules will retain data correctly only if the computer is in the stopped condition. For complete power-fail protection, a priority interrupt to the processor is necessary, along with suitable software routines for storing the CPU status in non-volatile memory and appropriate circuitry for fast detection of actual power failure. A comprehensive discussion of power fail-restart interrupt operation is beyond the scope of this bulletin.

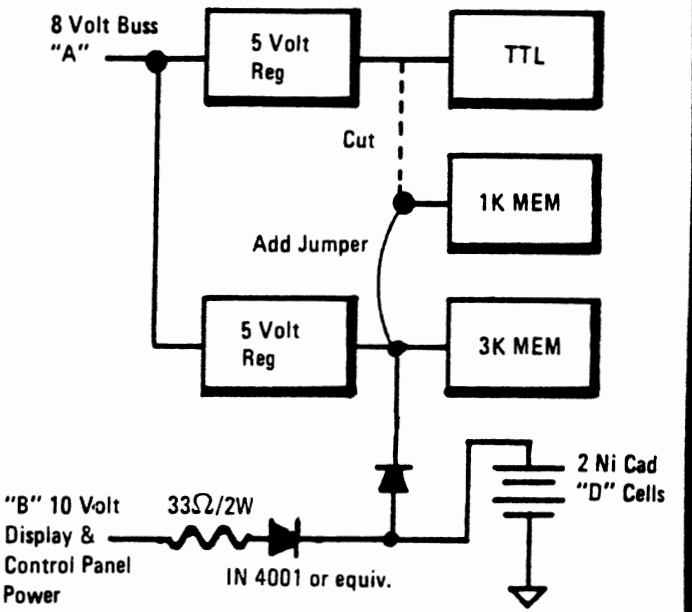

Figure 1

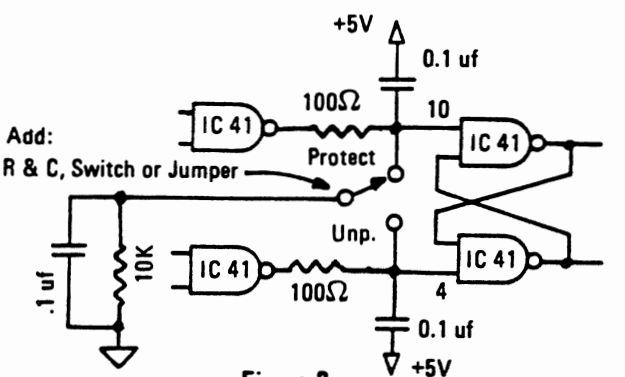

Figure 2

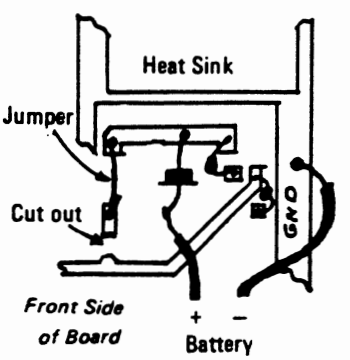

Figure 4

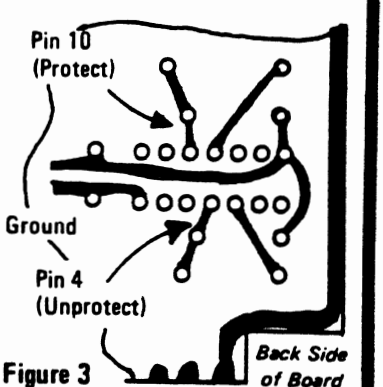

Figure 3

PROCESSOR TECHNOLOGY CORP.
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