ExpandoRAM II

OPERATIONS MANUAL

SD #7140042

SD SYSTEMS
P.O. Box 28810, Dallas, Texas 75228

OPERATIONS
MANUAL

EXPANDORAM II
EXPANDABLE RANDOM ACCESS MEMORY

REVISION C
MARCH 1981

LIMITED WARRANTY

All SD Systems products assembled by SD personnel and functionally tested at our facility are warranted for a period of ninety (90) days from date of purchase to be free from defects of material and workmanship. Kits or other products functionally unfinished or semi-finished at the time of shipment from our facility are warranted for the same period in regard to material defects only, with no warranty, expressed or implied, covering workmanship of others. Should an SD Systems product fail to perform to specifications, obtain a Returned Material Authorization number from your dealer or from SD Systems. Include this number in all correspondence and with the returned product. Ship the item prepaid to SD Systems and it will, at our option, be repaired or replaced free of charge, provided the unit is received during the warranty period. Testing or repair work performed upon returned kits or other products assembled wholly or partially by others will be subject to a $35.00 minimum service charge unless such products are found to be non-functional due to defects in material purchased from SD Systems.

In order to validate this warranty, the enclosed warranty card must be returned to SD Systems. If no warranty card is on file at the time of product return, dated proof of purchase will be required.

This warranty is invalid if product has been misused or modified. Warranty is limited to replacement of defective parts and no responsibility is assumed for damage to other equipment.

THERE ARE NO UNDERSTANDINGS, AGREEMENTS, REPRESENTATIONS, OR WARRANTIES, EXPRESSED OR IMPLIED, INCLUDING ANY REGARDING FITNESS FOR A PARTICULAR PURPOSE, NOT SPECIFIED IN THE WARRANTY.

TABLE OF CONTENTS

SECTION I

1-0 INTRODUCTION

The EXPANDORAM II board provides a low cost means for expanding Random Access Memory capability for computers utilizing the S-100 bus structure.

The EXPANDORAM II is optimized for operation with SD Systems' SBC-100/200. The EXPANDORAM II uses the Z-80 refresh signal and will operate at 4 MHZ if sufficiently fast rams are used.

1-1 GENERAL DESCRIPTION

The EXPANDORAM II board is a high performance dynamic RAM board using state-of-the-art MOS dynamic memory devices. The EXPANDORAM II may be configured to have a memory capacity of 16K, 32K, 48K, or 64K bytes of memory using the MK 4116 (16,384X1 MOS dynamic RAM) or 64K, 128K, 192K, or 256K bytes of memory using the MK4164 (65,536X1 MOS dynamic RAM) memories. Other notable features of the EXPANDORAM II board include:

(1) Phantom output disable or manual switch selectable output disable.

(2) Typical power dissipation of 5 watts

(3) 4 MHZ operation

(4) Port Addressable board select for multi-user system

(5) With 4164's, 4-64K banks are available

1-2 PHYSICAL

The EXPANDORAM II board is implemented on a single 5.25" x 10.0" x 0.65" Printed Circuit board. The board requires three DC voltages at levels of +7V to +10V, +14V to +18V, and -14V to -18V. The EXPANDORAM II board is interfaced to the system by connector J-1. Table 1-1 lists the overall specifications for the EXPANDORAM II board.

TABLE 1-1

SPECIFICATIONS

Memory Capacity	Up to 65,536 bytes (16K RAM) Up to 262,144 bytes (64K RAM)
Memory Access	200 ns max.
Memory Cycle	375 ns min.
Interface Levels	TTL Compatible
Power (2 us memory cycle)	+7V to +10V @ 400mA (max) +14V to +2-V @ 200mA (max) -14V to -20V @ 30mA (max)
Physical Dimensions	5.25" x 10.0" x .65"
Operating Temperature	0 degree C to 50 degree C

TABLE 1-2
CONNECTOR J1 PIN OUT
FOR 32K/64K EXPANDORAM II

PIN #	SIGNAL NAME	DIRECTION	DESCRIPTION
1,51	+8V to 10V		Power
2	+14V to 20V		Power
52	-14V to -20V		Power
25	Ø1	Input	Phase 1 clock
27	P WAIT	Input	Wait
79,80,81, 31,30,29, 82,83	A0-A7	Input	Address bus bits 0-7
84,34,37, 87,33,85, 86,32	A8-A15	Input	Address bus bits 8-15
36,35,88, 89,38,39, 40,90	D0-0 to D0-7	Input	Data bus in
95,94,41, 42,91,92, 93,43	DI-0 to DI-7	Output	Data bus out
44	SM1	Input	Machine cycle one
47	MEMR	Input	Memory read
66	RFSH	Input	Refresh (Z80 CPU card)
68	MEMW	Input	Memory write
72	PRDY	Output	Ready
78	PDBIN	Input	Data bus in
100,50	GROUND		
45	SOUT	Input	Port Output
99	POC	Input	Power on Clear
67	PHANTOM	Input	Phantom Disable

SECTION 2

2-0 FUNCTIONAL DESCRIPTION

The major functions of the EXPANDORAM II board are shown in figure 2-1. The following functions make up the memory interface: memory array, memory decode and control, address multiplexer, and data buffer.

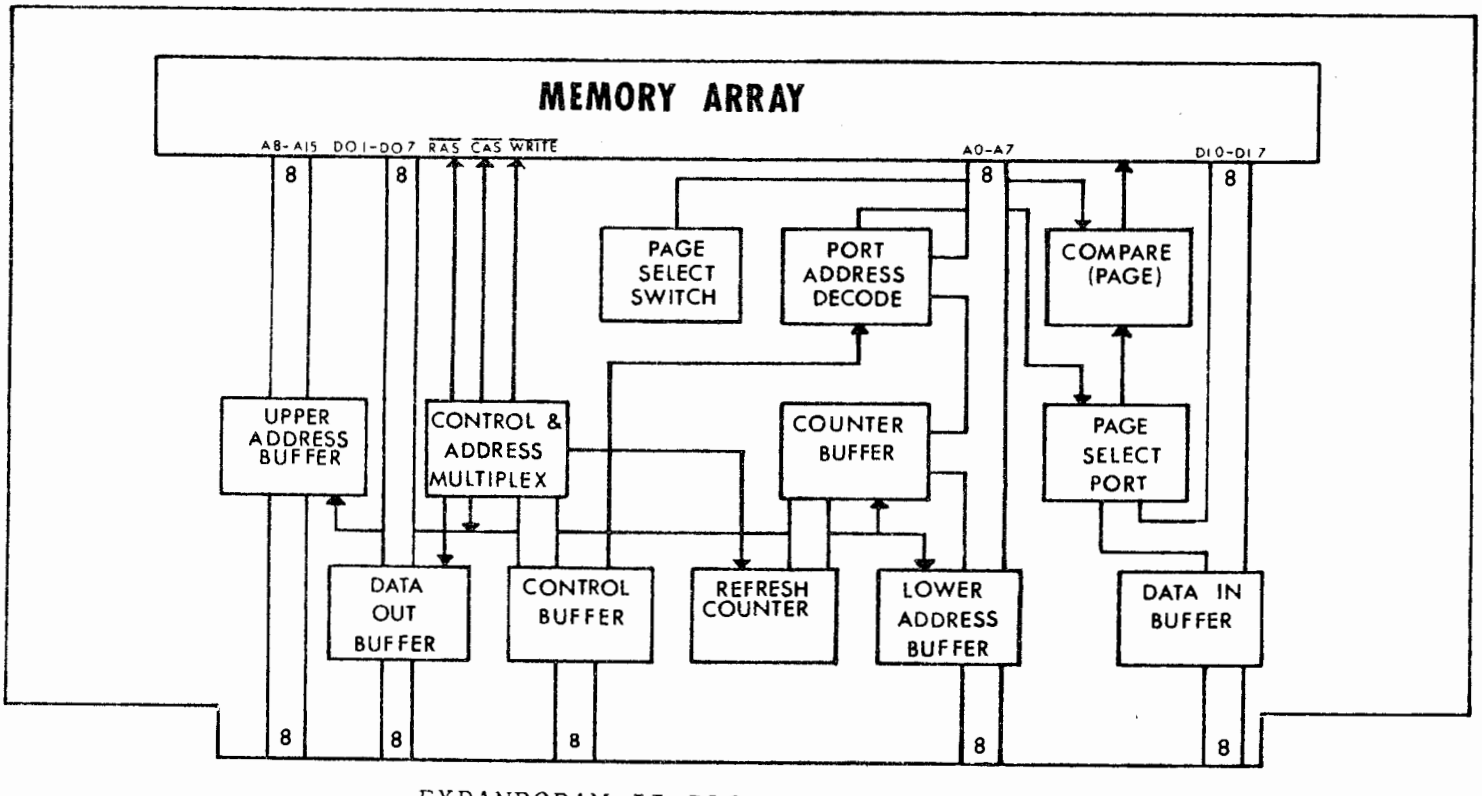
Memory Array - The memory array consists of up to 32 (16K or 64K) dynamic random access memory elements. Each 16K has a 16,384 x 1 bit capacity, while the 64K has a 65,536 x 1 bit capacity. The 32 (16K or 64K) RAMS are organized into four banks of eight RAMS each. The eight RAMS each contribute one bit to an addressable location. The total storage capacity of the EXPANDORAM II is 64,536 or 262,144 bytes, depending on the type of memory device used (16K or 64K).

Memory Decode and Control - The memory decode and control section is responsible for generating the timing signals for the memory array, address multiplexer, and data buffer. Timing within the memory decode and control section is generated by a TTL compatible delay line. An 82S130 PROM is used to select the proper banks according to the address lines, board select switches, and the board select latch. (See Section 4 for more details on Proms).

Address Multiplexer - The address multiplexer is responsibile for taking the address bits from the address bus buffers and multiplexing the proper row and column address into the memory array under control of the memory decode and control section.

Data Buffers - The data buffers, controlled by the memory decode and control section, isolate the memory array from the data bus.

Port FF Board Select - The port FF board select decodes port FF and latches the output data on the board.



EXPANDORAM II BLOCK DIAGRAM

Figure 2-1

3-0 CONSTRUCTION

The EXPANDORAM II board kit is intended for those persons who have had some prior experience with kit building and digital electronics. If you do not fall into this category, it is highly recommended that you find an experienced person to help you assemble and check out the board.

Appendix E shows the parts list for the EXPANDORAM II board. Double check all parts against the parts list.

3-1 ASSEMBLY PROCEDURE

(1) Install and solder the IC sockets in their proper locations as follows:

( ) 14-Pin - U1,U3-U7,U9,U10,U12,U17-U19,U21,U22,U58
( ) 16-Pin - U8,U11,U13,U15,U16,U26-U57
( ) 20-Pin - U14,U20,U23-U25

NOTE: No sockets for U2 or DIP switch S3.

(2) Install and solder the resistors as follows:

( ) R1, R4 33 Ohm (Orange, Orange, Black)

( ) R2, R6, R8 1K Ohm (Brown, Black, Red)

( ) R3 3.3K Ohm (Orange, Orange, Red)

( ) R5 150 Ohm (Brown, Green, Brown)

( ) R7 10K Ohm (Brown, Black, Orange)

( ) R9 470 Ohm (Yellow, Violet, Brown)

( ) R10 200 Ohm (Red, Black, Brown)

( ) Resistor packs: RP1 3, 4, 5 10 Pin SIP - 3.3K
RP2 6 Pin SIP - 3.3K

NOTE: Pin 1 of each SIP is designated by a notch or a dot on one end of the package.

(3) Install and solder diodes CR1, and CR2 with the banded end as shown on the PC board.

( ) CR1 1N751
( ) CR2 1N914 or 1N4148

(4) Install and solder the capacitors as follows:

( ) C1,C5,C8,C12,C14,C16 10MF Tantalum (Note Polarity)

( ) C2,C4,C6,C7,C9,C10,C13,C17-64 .1MF MICA

( ) C15,C3 200PF MICA

(5) Install and solder the two voltage regulators with the heatsink, using the 6-32 hardware supplies. NOTE: There are two types of voltage regulators, a +5V and a +12V. Be sure that the regulators are installed as shown on the Assembly Drawing.

( ) VR1 +5V 7805 or LM 340T-5

( ) VR2 +12V 7812 or LM 340T-12

(6) Install two PCB ejectors using pins (See Assembly Drawing).

(7) Install and solder DIP switch.

( ) S3 Observe the proper position of the PC board (the ON side should be toward the top of the board).

(8) Install and solder the delay line (U2) observing the location of pin 1

( ) U2 (DDU-4-5250 or PE21214 or TTLDL250)

(9) Double check all solder connections for cold solder joints, unsoldered connections, or shorted connections.

3-2 CHECK OUT PROCEDURE

(1) Install the board in the computer and measure the output of the

+5V and +12V regulators, VR1 and Vr2,

( ) VR1 = 5 volts

( ) VR2 = 12 volts

(2) Measure the power supply voltages in the memory array. (Any of the memory array IC sockets can be used.)

( ) Pin 1 U29 = -5V

( ) Pin 8 U29 = +12V

( ) Pin 9 U29 = +5V

NOTE: DO NOT PROCEED WITH BOARD CHECK-OUT UNTIL ALL POWER SUPPLY VOLTAGES ARE CORRECT. The TTL logic and MOS memories can be permanently damaged if improper voltages are applied.

(3) Install the IC's in their sockets observing the Pin 1 designation on each socket on the PC board.

( ) U1	74LSØØ	( ) U14	74LS244
( ) U3	74LS1Ø	( ) U15	33 Ohm DIP
( ) U4	74LS2Ø	( ) U16	74LS162
( ) U5	74LSØØ	( ) U17	74LSØØ
( ) U6	74LS74	( ) U18	74LS14
( ) U7	74LSØ2	( ) U19	74LS3Ø
( ) U8	82S130	( ) U20	74LS373
( ) U9	74LS393	( ) U21	74LS74
( ) U10	74LSØØ	( ) U22	74LS14
( ) U11	74LS368	( ) U23	74LS244
( ) U12	74LS14	( ) U24	74LS244
( ) U13	74LS174	( ) U25	74LS244
		( ) U58	74LS122

*( ) U26-33 (Bank 0) RAM

*( ) U34-41 (Bank 1) RAM

*( ) U42-49 (Bank 2) RAM

*( ) U50-57 (Bank 3) RAM

*NOTE: If less than 64K is being installed on the board then refer to Section IV under ADDRESSING SWITCH to determine in which Bank the memory should be installed.

(4) Double check all IC's for proper orientation and location.

(5) Refer to UTILIZATION SECTION for proper configuration of jumper options, and connect jumper options as required.

(6) Install board into computer and turn on power.

(7) By using front panel or monitor program, deposit data into a memory location that falls within the boundaries of the EXPANDORAM II board. Now examine the same location in which data was deposited. If the proper data is not read back, power the system down and double check the following:

(1) Check ADDRESSING DIP Switch and board Select Dip Switch for the correct settings.

(2) Check jumper options.

(8) Reinstall the board and once again try to write and read data from the EXPANDORAM II board by the use of a front panel or monitor program. If some of the data bits appear to be stuck, power down the board and examine the memory array for bent pins, or a defective

memory device. If the board does not respond in any way to write or read data, then examine the TTL IC's for bent pins or improper insertions into the socket.

(9) If the read/write test is successful, verify that memory on the EXPANDORAM II can be accessed in every bank of memory that is installed on the board.

(10) If all banks can be written to and read back properly, complete check-out of the board by loading the memory test that is shown in Appendix A. Execute the test and verify that all locations within the memory array are functional.

NOTE: When executing the memory diagnostic, it is recommended that the memory board not be on an extender card. Use of an extender card may introduce external noise into the board.

SECTION 4

4-0 UTILIZATION

This section will explain the various options for the EXPANDORAM II memory card.

4-1 16K or 64K DEVICE SELECTION JUMPERS

Two types of RAMS may be used with the EXPANDORAM II. These are the 16K RAM (4116) and the 64K (4164). The board comes in a standard configuration that uses 16K RAMS. In order to use the 64K RAMS the following cuts and connections must be made:

A. Cut etch between E1 and E2

B. Cut etch between E4 and E5

C. Cut etch between E6 and E8

D. Connect E2 to E3

E. Connect E6 to E7

4-2 PROM INFORMATION

There are two proms available for use with the EXPANDORAM II. These proms perform memory decoding. These are for use with 32K or 48K partition multi-user systems. If the board is used in a single-user environment, either Prom will work. In addition, other Proms may be configured if the user desires.

4-3 SWITCH SETTINGS

The information for the switch settings of S3 for the EXPANDORAM II is given in figure 4-1.

Port FF is used to select the Memory page (32K or 48K) to be accessed by the CPU. Up to 10 pages (0-9) may be in a system simultaneously, by using either 6 Expandoram II boards with a 32K Prom or 8 Expandoram II board with a 48K Prom (user ØAH has 16K positioned at @ CØØØH). The pages are accessed by outputting the page number to port FF. See Figure 4-2 for page mapping and Prom program information.

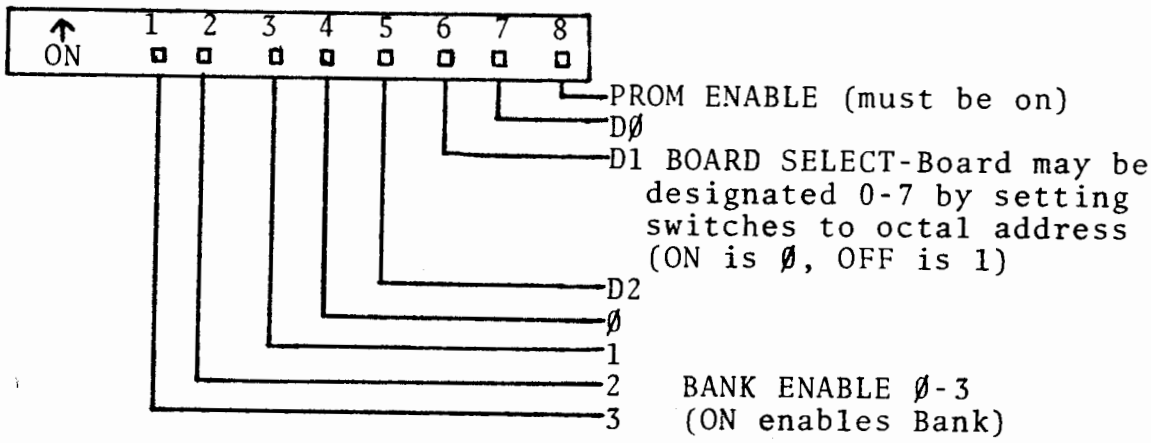


FIGURE 4-1

4-4 USING THE EXPANDORAM II IN NON-SD SYSTEMS ENVIRONMENTS

Some CPU boards supply a different phase of the system clock on pins 24 and 25. If one of these CPU boards are used with the Expandoram II, make the following change. Cut the etch on the back of the board between E22 and E23. Install a jumper between E23 and E24. Also cut the etch between E26 and E25 and install a jumper between E26 and E27. Install the phantom disable jumper between E9 and E10 if the system has other memory in conflict with the Expandoram II board. In addition, if the system is operated at

at 4 MHZ, install the jumper between E14 and E15 to enable M1 Wait States.

APPENDIX A

MEMORY DIAGNOSTIC SOFTWARE LISTING

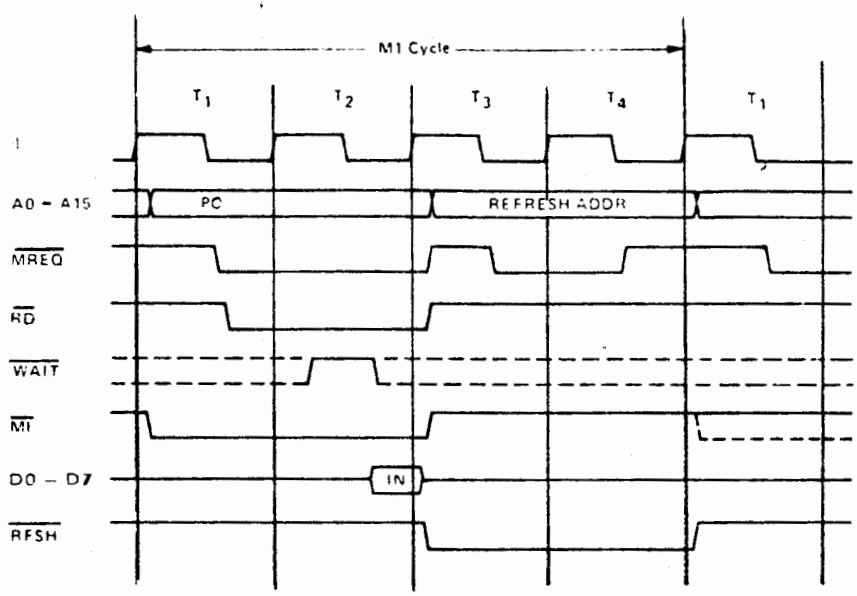
```
ADDR  OBJECT        ST # SOURCE STATEMENT
                    0001 ;TRANSLATED FROM DEC 1976 INTERFACE MAGAZINE
                    0002 ;
                    0003 ;THIS IS A MODIFIED ADDRESS STORAGE TEST WITH
                    0004 ;AN INCREMENTING PATTERN
                    0005 ;
                    0006 ;256 PASSES MUST BE EXECUTED BEFORE THE MEMORY
                    0007 ;IS COMPLETELY TESTED
                    0008 ;
                    0009 ;IF AN ERROR OCCURS, THE PATTERN WILL BE STORED
                    0010 ;AT LOCATION '002C'H AND THE ADDRESS OF THE
                    0011 ;ERROR LOCATION WILL BE STORED AT '002D'H
                    0012 ;AND '002E'H.
                    0013 ;
                    0014 ;THE CONTENTS OF LOCATIONS '000C'H AND'001D'H
                    0015 ;SHOULD BE SELECTED ACCORDING TO THE FOLLOWING
                    0016 ;MEMORY SIZE TESTED
                    0017 ;
                    0018 ;TOP OF MEMORY TO
                    0019 ;BE TESTED                          VALUE OF EPAGE
                    0020 ;
                    0021 ;      4K                                '10'H
                    0022 ;      8K                                '20'H
                    0023 ;     16K                                '40'H
                    0024 ;     32K                                '80'H
                    0025 ;     48K                                'CO'H
                    0026 ;     64K                                'FF'H
                    0027 ;
                    0028 ;THE PROGRAM IS SET UP TO START TESTING AT
                    0029 ;LOCATION '002F'H. THE STARTING ADDRESS FOR THE
                    0030 ;TEST CAN BE MODIFIED BY CHANGING LOCATIONS
                    0031 ;'0003'H-'0004'H AND '0011'H-'0012'H.
                    0032 ;
                    0033 ;TEST TIME FOR A 16K BY 8 MEMORY IS APPROX. 4 MIN
                    0034 ;
                    0035 ;        PSECT   ABS
>0000               0036 ;        ORG     0000H
0000  0600          0037 ;        LD      B,0       ;CLEAR B PATRN MODIFIER
                    0038 ;LOAD UP MEMORY
0002  212F00        0039 LOOP:    LD      HL,START  ;GET STARTING ADDR
0005  7D            0040 FILL:    LD      A,L       ;LOW BYTE TO ACCM
0006  AC            0041          XOR     H         ;XOR WITH HIGH BYTE
0007  A8            0042          XOR     B         ;XOR WITH PATTERN
0008  77            0043          LD      (HL),A    ;STORE IN ADDR
0009  23            0044          INC     HL        ;INCREMENT ADDR
000A  7C            0045          LD      A,H       ;LOAD HIGH BYTE OF ADDR
000B  FE10          0046          CP      EPAGE     ;COMPARE WITH STOP ADDR
000D  C20500        0047          JP      NZ,FILL   ;NOT DONE,GO BACK
                    0048 ;READ AND CHECK TEST DATA
0010  212F00        0049          LD      HL,START  ;GET START ADDR
0013  7D            0050 TEST;    LD      A,L       ;LOAD LOW BYTE
0014  AC            0051          XOR     H         ;XOR WITH HIGH BYTE
0015  AB            0052          XOR     B         :XOR WITH MODIFIER
0016  BE            0053          CP      (HL)      ;COMPARE WITH MEMORY LOC
0017  C225000       0054          JP      NZ,EXIT ;ERROR EXIT
001A  23            0055          INC     HL        ;UPDATE MEMORY ADDR
001B  7C            0056          LD      A,H       ;LOAD HIGH BYTE
001C  FE10          0057          CP      EPAGE     ;COMPARE WITH STOP ADDR
001E  C21300        0058          JP      NZ,TEST   ;LOOP BACK
0021  04            0059          INC     B         ;UPDATE MODIFIER
0022  C30200        0060          JP      LOOP      ;RST WITH NEW MODIFIER
```

```
                        0061 ;ERROR EXIT
0025   222D00           0062 EXIT    LD      (BYTE),HL ;SAVE ERROR ADDRESS
0028   322C00           0063         LD      (PATRN),A ;SAVE BAD PATTERN
002B   76               0064         HALT              ;FLAG OPERATOR
>002C                   0065 PATRN:  DEFS    1
>002D                   0066 BYTE:   DEFS    2
002F    2F00            0067 START:  DEFW    $
0031    3100            0068         DEFW    $         ;PLACE FOR FIRST ADDR
>0010                   0069 EPAGE:  EQU     10H       ;SET UP FOR 4K TEST
                        0070         END
```

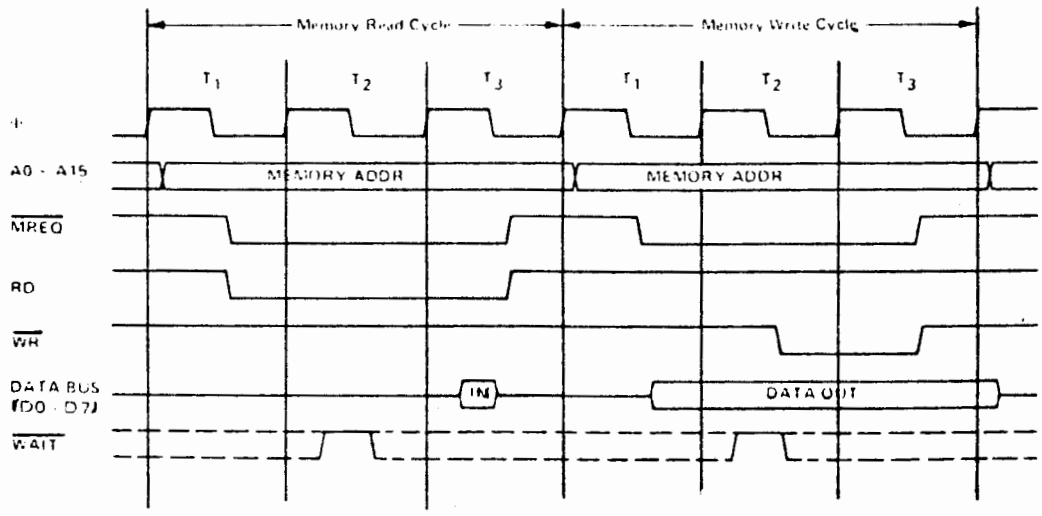
APPENDIX B

EXPANDORAM II TIMING DIAGRAM

INSTRUCTION OP CODE FETCH



MEMORY READ OR WRITE CYCLES

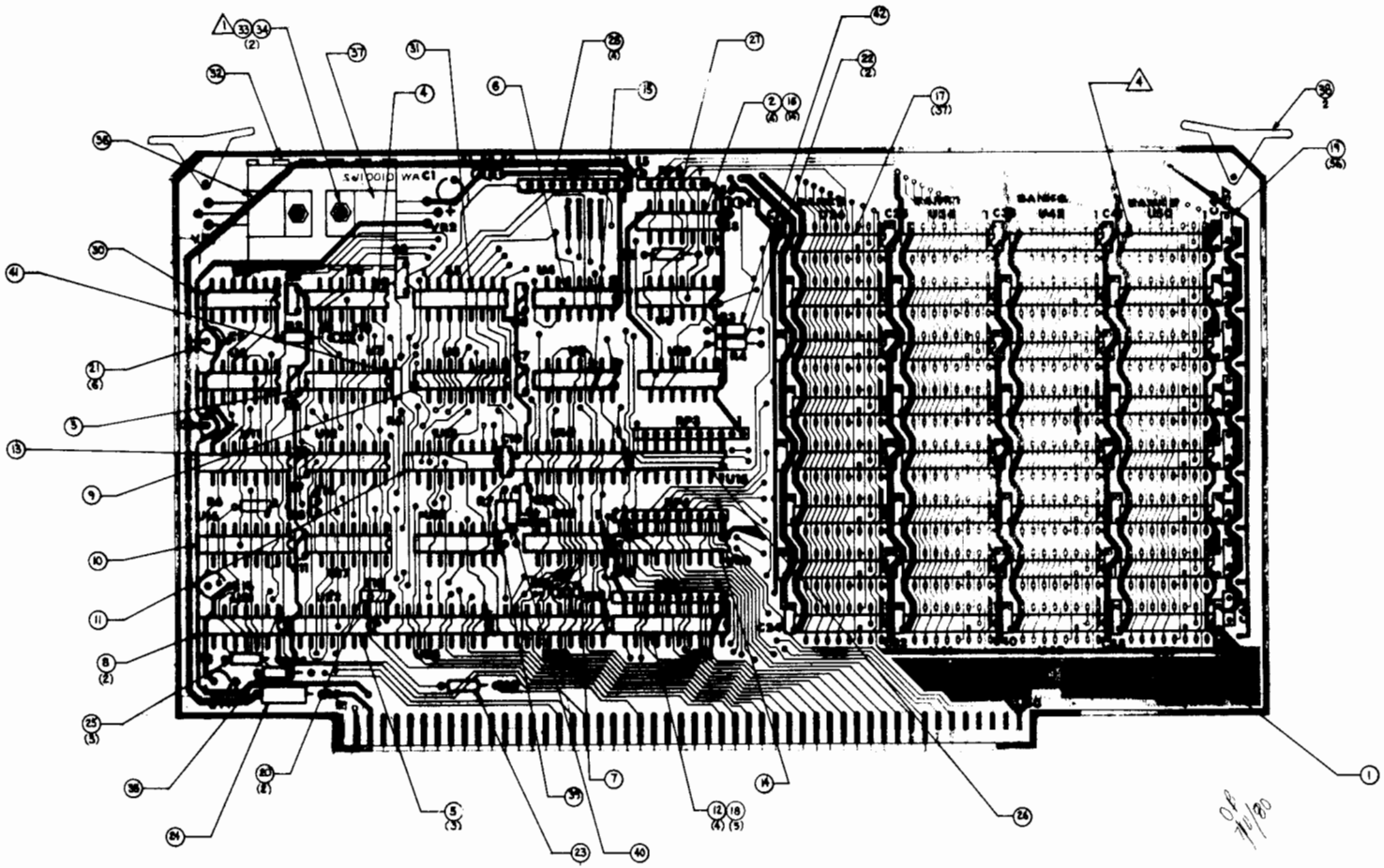


APPENDIX C

EXPANDORAM II

ASSEMBLY DRAWING

REVISIONS			
LTR	DESCRIPTION	DATE	APR
C	INIT PROD RELEASE	1-23-80	
D	PER ECN 0150		JCC



SEE SEPARATE B.O.M. 0100160

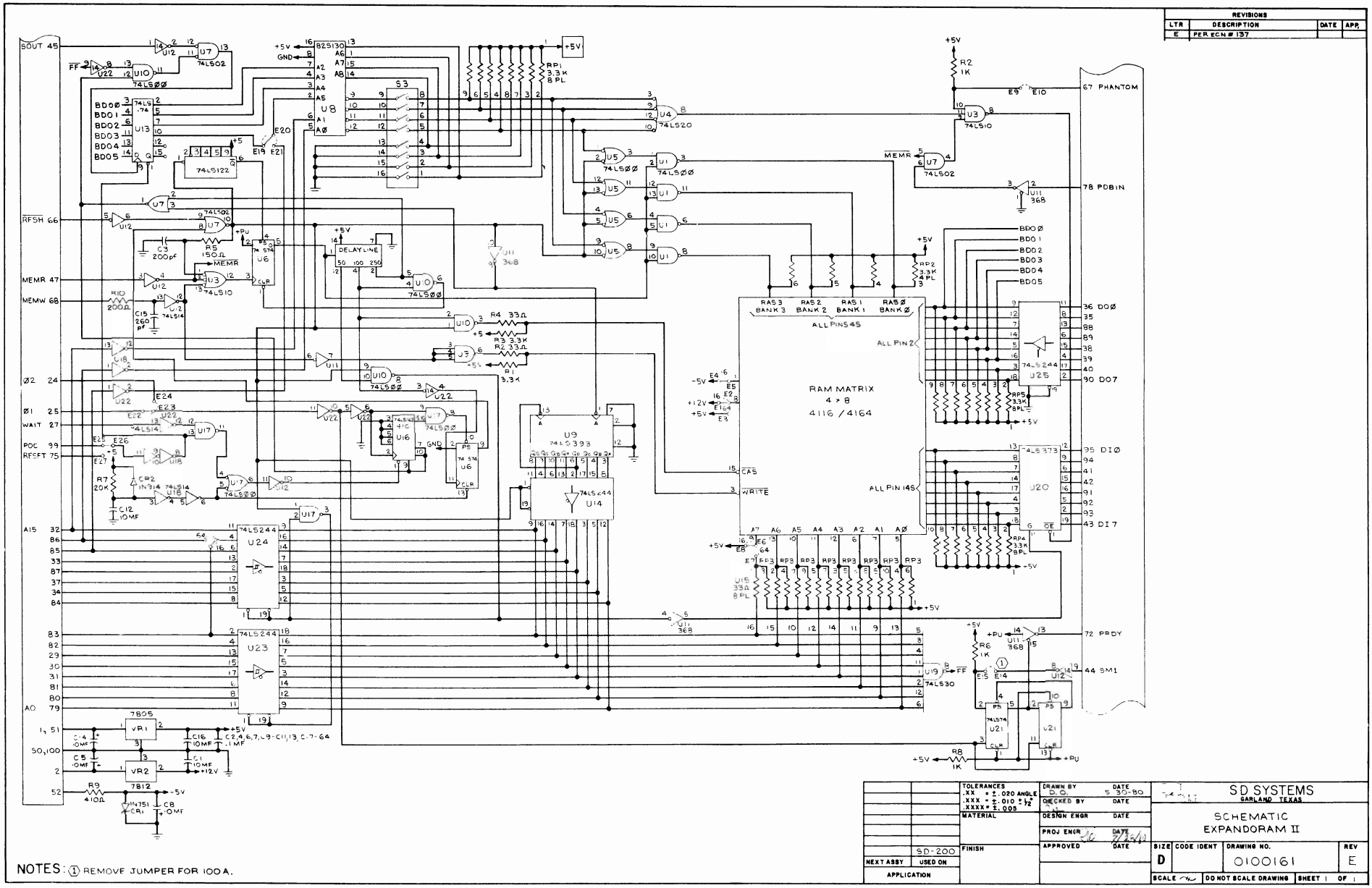
NOTES:

1. ASSEMBLE ALL OTHER PARTS PER PARTS LIST.
2. DEGREASE BOARD.
3. APPLY THERMAL COMPOUND P.N. 120-8 TO YR162.
4. FOR 64K SEE BOM 0100210
   FOR 48K SEE BOM 0100209
   FOR 32K SEE BOM 0100208
   FOR 16K SEE BOM 0100207

		TOLERANCES .XX ± .010 ORD ANGLE .XXX ± .005 ± 1/2° .XXXX ± .003	DRAWN BY [illegible] DATE 10-17-79	SD SYSTEMS GARLAND TEXAS	
		MATERIAL	CHECKED BY DATE	PCB ASSY. EXPANDORAM II	
			DESIGN ENGR DATE		
		FINISH	PROJ ENGR DATE		
	80/109 80/100		APPROVED DATE	SIZE D CODE IDENT	DRAWING NO. 0100160 REV D
NEXT ASSY	USED ON			SCALE	DO NOT SCALE DRAWING SHEET OF
APPLICATION					

APPENDIX D

EXPANDORAM II SCHEMATIC


REVISIONS
LTR | DESCRIPTION | DATE | APP.
E | PER ECN # 137
RAM MATRIX
4 x 8
4116 / 4164
ALL PINS 4S
ALL PIN 2
ALL PIN 14S
RAS3 BANK 3
RAS2 BANK 2
RAS1 BANK 1
RAS0 BANK 0
CAS
WRITE
67 PHANTOM
78 PDBIN
72 PRDY
44 SM1
36 DO0
35
88
89
38
39
40
90 DO7
35 DI0
94
41
42
91
92
93
43 DI7
SOUT 45
RFSH 66
MEMR 47
MEMW 68
Ø2 24
Ø1 25
WAIT 27
POC 99
RESET 75
A15 32
A0 79
I, 51
SO, 100
2
52
NOTES: ① REMOVE JUMPER FOR 100A.
SD SYSTEMS
GARLAND TEXAS
SCHEMATIC
EXPANDORAM II
SIZE D
DRAWING NO. 0100161
REV E
SCALE
DO NOT SCALE DRAWING
SHEET 1 OF 1
DRAWN BY D.O. DATE 5-30-80
CHECKED BY DATE
DESIGN ENGR DATE
PROJ ENGR DATE
APPROVED DATE
TOLERANCES .XX ± ±.020 ANGLE .XXX ± ±.010 ± ½° XXXX ± .005
MATERIAL
FINISH SD-200
NEXT ASSY USED ON
APPLICATION

APPENDIX E

EXPANDORAM II PARTS LIST

SD Systems

P.O. Box 28810 • Dallas, Texas 75228 214-271-4667

BILL OF MATERIALS

Title:	PL No.	Rev.
EXPANDORAM II	0100160	G
Date Released:	**Approved:** QP	**Sheet** 2 **Of** 4

Item no	Qty	SD-P/N	Description	Unit Cost	Extension
1	1	7000012	PRINTED CIRCUIT BOARD 0100162		
2	4	7010160	74LS00 U1, U5, U17 & U10		
3	1	7010162	74LS02 U7		
4	1	7010168	74LS10 U3		
5	3	7010172	74LS14 U12, U18 & U22		
6	1	7010174	74LS20 U4		
7	1	7010180	74LS30 U19		
8	1	7010195	74LS74 U21		
9	1	7010407	82S130 U8 (EX2-48K)		
10	1	7010232	74LS162 U16		
11	1	7010241	74LS174 U13		
12	4	7010264	74LS244 U14, U23, U24 & U25		
13	1	7010303	74LS368 U11		
14	1	7010304	74LS373 U20		
15	1	7010312	74LS393 U9		
16	15	7060002	14 PIN IC SOCKET U1, U3, U4, U5, U6,		
			U7, U9, U10, U12, U17, U18, U19, U21, U22 & U58		
17	37	7060003	16 PIN IC SOCKET U8, U11, U13, U15, U16 &		
			U26 THRU U57		
18	5	7060005	20 PIN IC SOCKET U14, U20, U23, U24 & U25		
19	56	7030045	.1MF CAPACITOR C2, C4, C6, C7, C9,		
			C10, C11, C13 & C17 THRU C64		
20	2	7030043	200 PF CAPACITOR C15 & C3		
21	6	7030009	10 MF CAPACITOR C1, C5, C8, C12, C14 & C16		

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BILL OF MATERIALS

Title: EXPANDORAM II	PL No. 0100160	Rev. G
Date Released:	Approved:	Sheet 3 of 4

Item no	Qty	SD-P/N	Description	Unit Cost	Extension
22	2	7020037	33Ω 5% 1/4 WATT RESISTOR R1 & R4		
23	1	7020056	200Ω 5% 1/4 WATT RESISTOR R10		
24	1	7020065	470Ω 5% 1/4 WATT RESISTOR R9		
25	3	7020073	1KΩ 5% 1/4 WATT RESISTOR R2, R6 & R8		
26	1	7010346	33Ω 16 PIN DIP RESISTOR PACK U15		
27	1	7010344	3.3KΩ 6 PIN SIP RESISTOR PACK RP2		
28	4	7010345	3.3KΩ 10 PIN SIP RESISTOR PACK		
			RP1, RP3, RP4 & RP5		
29	1	7010213	74LS122 U58		
30	1	7010366	DELAY LINE U2		
31	1	7050002	8 POSITION DIP SWITCH (16 PIN DIP) S3		
32	1	7130003	HEAT SINK		
33	2	7130006	6-32 × 3/8 SCREW PHILLIPS HEAD		
34	2	7130007	6-32 HEX NUT		
35	1	7040003	IN751-5V ZENER DIODE CR1		
36	1	7160001	5 VOLT REGULATOR VR1		
37	1	7160003	12 VOLT REGULATOR VR2		
38	2	7130072	PCB EJECTOR		
39	1	7020097	20KΩ 5% 1/4 WATT RESISTOR R7		
40	1	7040001	IN914 DIODE CR2		
41	1	7020053	150Ω 5% 1/4 WATT RESISTOR R5		
42	1	7020085	3.3KΩ 5% 1/4 WATT RESISTOR R3		
43	3	7170004	JUMPER STRAP		
44	2	7170018	BERG HEADER 1X2		

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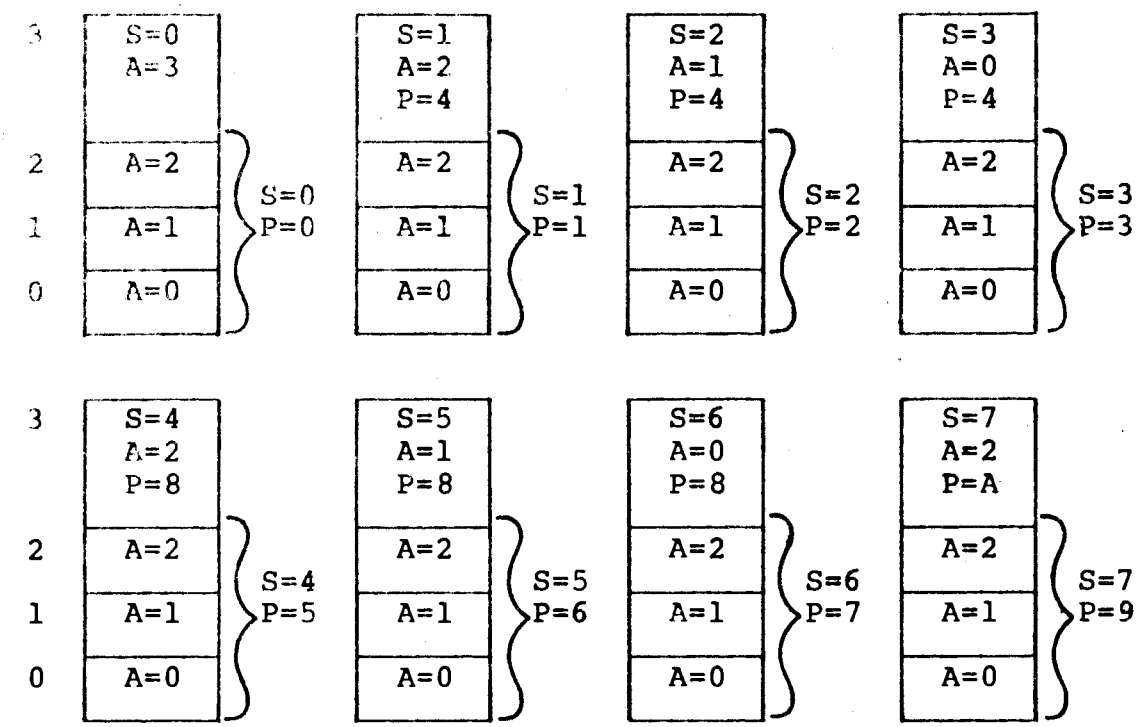
P.O. Box 28810 • Dallas, Texas 75228 214-271-4667

BILL OF MATERIALS

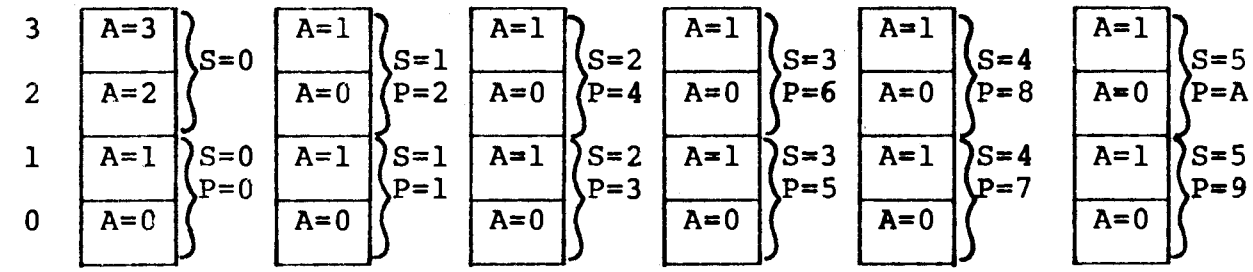
Title: EXPANDORAM II	PL No. 0100160	Rev. G
Date Released:	Approved:	Sheet 4 Of 4

Item no	Qty	SD-P/N	Description	Unit Cost	Extension
45	1	7010402	74S74 U6		
46	1	7170021	BERG HEADER 1x3		

48 BOUNDARY SELECTION



32 BOUNDARY SELECTION

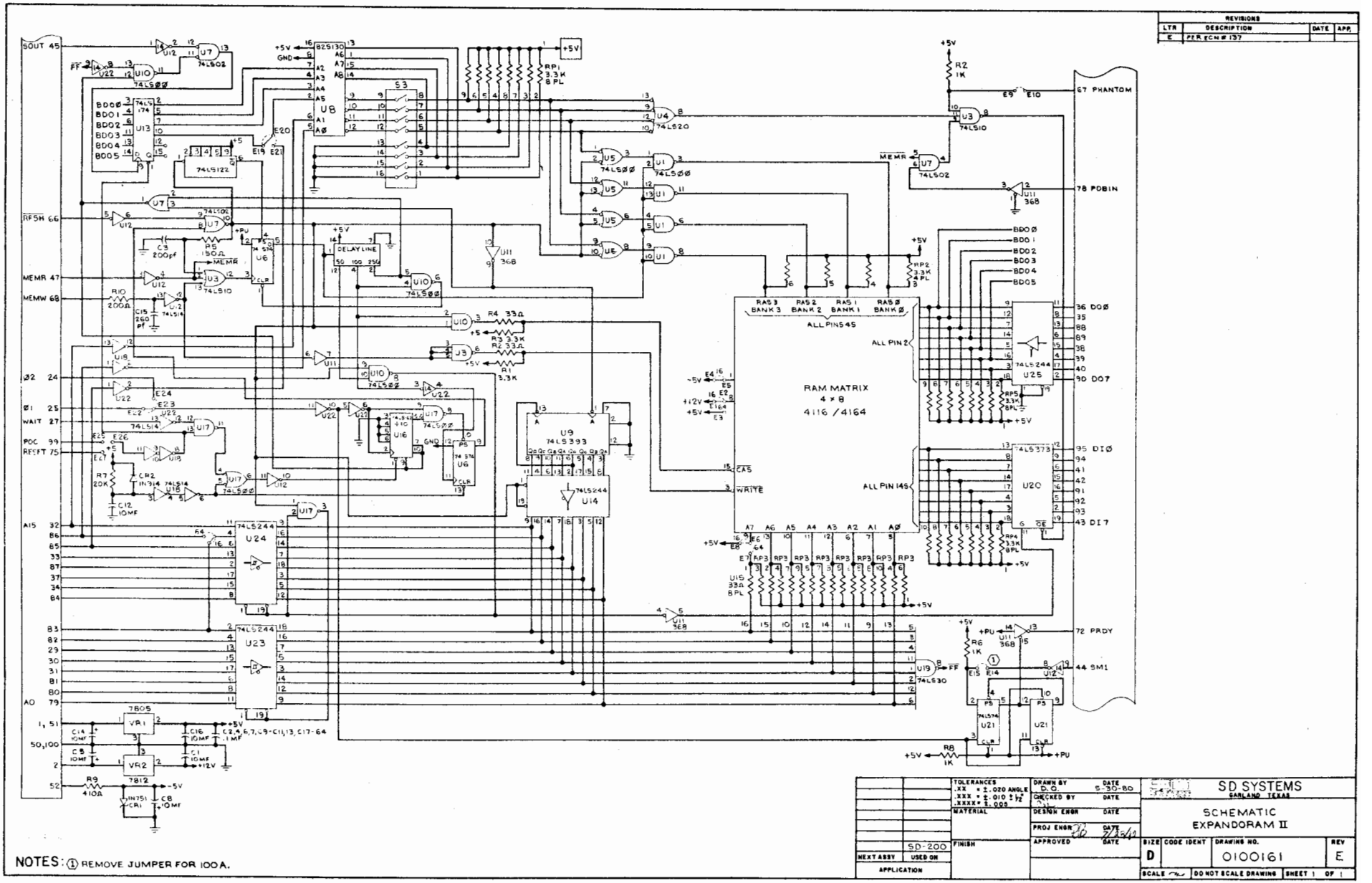


S (BD) (NBR)	A8		
	A7	8	04
	A6	2	
P (USER) (NBR)	A5	S	03
	A4	1	
	A3	3	02
	A2	0	
A (A15,A14)	A1		01
	A0		

BANK SELECTED	PROM OUTPUT
3	7
2	B
1	D
0	E

NOTE: P=B,C,D,E,F IS RESERVED.

Figure 2-4. PROM Program and Page Mapping.



REVISIONS			
LTR	DESCRIPTION	DATE	APP.
E	PER ECN # 137		

TOLERANCES	DRAWN BY D.G.	DATE 5-30-80
.XX ± .020 ANGLE	CHECKED BY	DATE
.XXX ± .010 ± ½°	DESIGN ENGR	DATE
.XXXX ± .005	PROJ ENGR	DATE
MATERIAL	APPROVED	DATE
FINISH		
NEXT ASSY USED ON		
APPLICATION		

SCALE — DO NOT SCALE DRAWING SHEET 1 OF 1