THE LAST MEMORY™

SMS *static memory systems* MB1A

STATIC MEMORY SYSTEMS Inc.

THE LAST MEMORY™

USER AND ASSEMBLY MANUAL

MB1A

Static Memory Systems Inc.
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SECTION 1

General Information and Specifications

1.1 General

THE LAST MEMORY™ is a high performance 64K memory module for 8 bit S100 systems. This board uses TMM 2016, MB8128, of equivalent STATIC RAM's. The use of STATIC RAM eliminates the timing and reliability problems associated with dynamic RAM boards. The 2K by 8 architecture of these RAM's allows high density and low power consumption, a characteristic not found in most static memories.

THE LAST MEMORY™ also accomodates 2716 type EPROM's in place of the RAM IC's with no modifications. As a result, this one board provides total system memory.

1.2 Mixing RAM and EPROM

The 2K by 8 static RAM (see Table 1.1 for compatible RAM) and 2716 EPROM's are pin-for-pin compatible and may be located at any position on this board. However, caution must be exercised when mixing RAMs and 2716s. The RAM's supplied have an access time of 150 nsec, allowing full speed operation with many 6 MHz processors. High speed versions of the 2716 are not available and since wait states are not generated by THE LAST MEMORY™, system speed is limited by the speed of the 2716's used. If high speed operation is required, the Harris semiconductor HM 7617 bipolar PROM may be used in place of the 2716 EPROM. This is a 60 nsec part, but it is not reprogrammable.

Two types of 2716 EPROM's are currently available, one requiring +5 volt only power, and one requiring multiple supplies. Only the +5 volt only type 2716's may be used with this board. Power requirements for 2716 EPROM's are somewhat higher than for 2016 RAM's. No mix of 2016's and 2716's should be used which requires more than 1.0 ampere of supply current.

Due to the higher current requirements of EPROM's, a 7437 has been supplied in place of the 74LS00 (IC2) to support more than 2 EPROM's (see SECTION 5.3). However, if more than 8 EPROM's (16K) are desired, board modifications may be required (consult factory).

1.3 S100 Bus

All bus lines used by this board conform to the proposed IEEE 696.1 Standard. Some "S100" boards, however, have conflicts with this standard. BEFORE INSERTING THIS BOARD INTO THE SYSTEM, check the system bus. SECTION 2 describes bus lines that should be checked as well as the modifications which may be required. This board may not be compatible with front panels which do not act as IEEE 696 temporary masters (generating all status and strobe signals).

THE LAST MEMORY™ has the following levels of compliance as defined by IEEE 696.1 -

SLAVE	
D8	8-data bus only
M24	24-bit memory address path
T150	150 nsec access time
W0	no ability to generate wait states
SH	standard height board (5 inches)

1.4 Addressing

THE LAST MEMORY™, while it may occupy the entire 64K address space of 8-bit microprocessors, maintains compatibility with memory mapped I/O boards which require a part of this space. The location of memory on this board is determined by the particular socket into which a memory IC is inserted. Empty sockets occupy no address space and, therefore, allow for other memory mapped boards. SECTION 2 describes this in detail.

Eight extended address lines, as defined by IEEE 696 have been included. This feature allows the use of multiple memory boards, expanding system memory beyond 64K.

1.5 Specifications

Bus	S100 - IEEE 696.1 Bus Compliance:
	SLAVE D8 M24 T150 WO SH
Storage capacity	2K to 64K in 2K increments
Memory Type	RAM: 2K by 8 static
	EPROM: 2716 (+5 volt only)
Addressing	2K boundaries
Extended addressing	Includes 8 extended address lines
PHANTOM	4 modes
Maximum input load	One LS TTL load
Output buffering	On all data lines
Access time (RAM only)	150 nsec
Wait states generated	None
Power consumption:	
64K RAM	515 mA (typ.) 885 mA (max.)
56K RAM + 8K EPROM	525 mA (typ.) 915 mA (max.)

Compatible RAM

TOSHIBA	TMM2016	NMOS
	TC 5517	CMOS
FUJITSU	MB 8128	NMOS
	MB 8416	CMOS
HITACHI	HM 6116	CMOS
MITSUBISHI	M 58725	NMOS
SYNERTEK	SY2128	NMOS
NATIONAL	NMC2116	NMOS

Table 1.1

SECTION 2

Initial Set Up

2.1 General

READ THIS SECTION COMPLETELY BEFORE INSERTING THE LAST MEMORY™ INTO THE SYSTEM. Described below are checks for proper S100 bus compatibility as well as procedures for setting memory addresses.

2.2 S100 Bus Compatibility

The S100 Bus definition has undergone an evolutionary process since it was originally introduced. Only now is it being standardized via IEEE 696. The bus lines used by THE LAST MEMORY™ are all compatible with IEEE 696. Unless precautions are taken, conflicts with other system boards, using an earlier S100 definition, may result. Table 2.1 lists the bus lines which should be examined. Other bus lines used by this board have not changed definition and should not present a problem. See Appendix D for a complete list of the S100 bus lines.

Potential Conflicting S100 Lines

Number	Early S100	IEEE 696 S100
20	UNPROT	Ground
53	SSW DSB	Ground
70	PROT	Ground
16	Various	A_{16}
17	Various	A_{17}
15	Various	A_{18}
59	Various	A_{19}
61	Various	A_{20}
62	Various	A_{21}
63	Various	A_{22}
64	Various	A_{23}
67	Various	PHANTOM

Table 2.1

Lines 20, 53, and 70 present the most common conflicts. For this reason, they have NOT been connected to ground on THE LAST MEMORY™. Rather solder pads have been provided (see Figure 2.1) so that the user may jumper these pins to ground at his option. These jumpers are not necessary for proper operation.

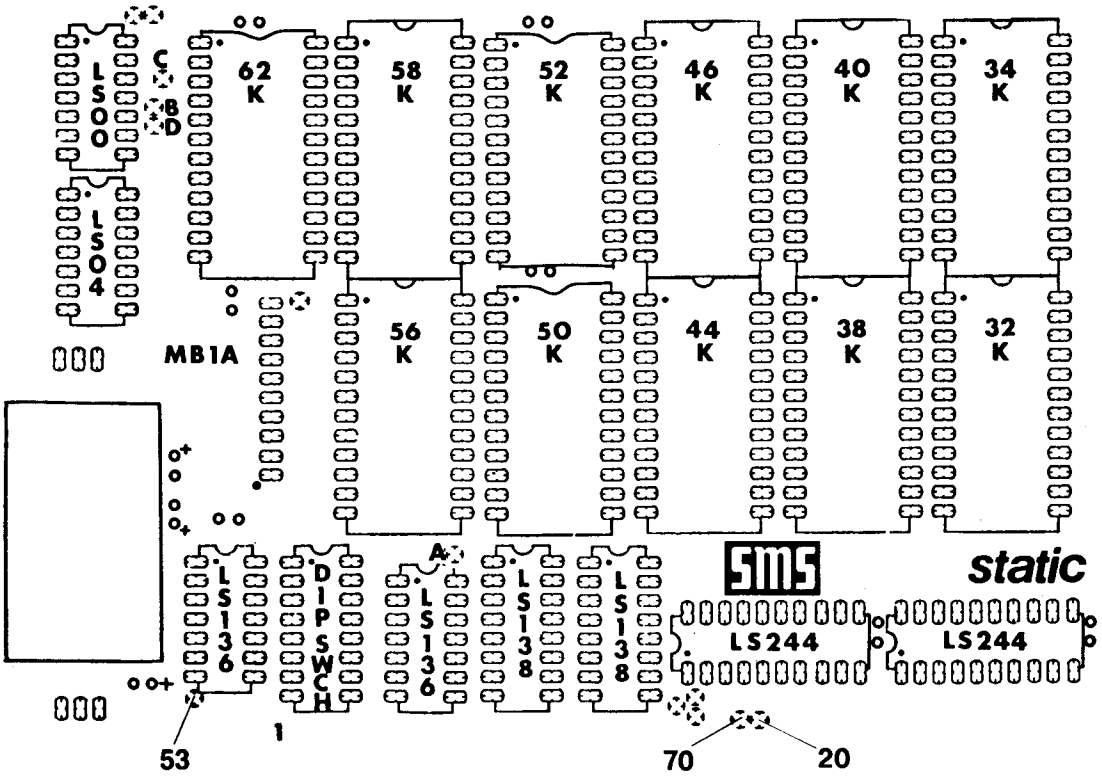


Figure 2.1

If a conflict exists with the extended address pins (A_{16} through A_{23}), then the extended address feature must be disabled. If a conflict exists for only A_{19}, A_{20}, A_{21}, or A_{22} then it is necessary to remove the 74LS136 IC nearest the outside edge of the board (IC4), which will disable only these address lines. If a conflict exists for any of the remaining address lines, then the second 74LS136 (IC5) must be removed as well.

2.3 Memory Addresses

The location of memory is defined by the particular socket into which a memory IC is inserted. Sockets are numbered 2K through 64K (visible in the upper center of the socket). This number corresponds to the cummulative board memory when consecutive sockets are filled. For example, if only the 2K socket is filled, the board will have 2K of memory. If only the 8 sockets, numbered 2K through 16K, are filled, the board will have 16K of memory.

In both of the above examples, memory starts at address zero and is consecutive. In practice, this will not always be the case. Table 2.2 gives the address locations for each socket. Memory IC's may be inserted into any socket, as required. Sockets left empty occupy no memory space and, therefore, the corresponding address may be used by other system boards. Care should be taken to correctly place EPROM's, as they will not generally operate when their address location is incorrect.

Memory Address Locations

Socket	HEX Address	SPLIT-OCTAL Address	Decimal Address
2K	0000 - 07FF	000:000 - 007:377	0 - 2047
4K	0800 - 0FFF	010:000 - 017:377	2048 - 4095
6K	1000 - 17FF	020:000 - 027:377	4096 - 6143
8K	1800 - 1FFF	030:000 - 037:377	6144 - 8191
10K	2000 - 27FF	040:000 - 047:377	8192 - 10239
12K	2800 - 2FFF	050:000 - 057:377	10240 - 12287
14K	3000 - 37FF	060:000 - 067:377	12288 - 14335
16K	3800 - 3FFF	070:000 - 077:377	14336 - 16383
18K	4000 - 47FF	100:000 - 107:377	16384 - 18431
20K	4800 - 4FFF	110:000 - 117:377	18432 - 20479
22K	5000 - 57FF	120:000 - 127:377	20480 - 22527
24K	5800 - 5FFF	130:000 - 137:377	22528 - 24575
26K	6000 - 67FF	140:000 - 147:377	24576 - 26623
28K	6800 - 6FFF	150:000 - 157:377	26624 - 28671
30K	7000 - 77FF	160:000 - 167:377	28672 - 30719
32K	7800 - 7FFF	170:000 - 177:377	30720 - 32767
34K	8000 - 87FF	200:000 - 207:377	32768 - 34815
36K	8800 - 8FFF	210:000 - 217:377	34816 - 36863
38K	9000 - 97FF	220:000 - 227:377	36864 - 38911
40K	9800 - 9FFF	230:000 - 237:377	38912 - 40959
42K	A000 - A7FF	240:000 - 247:377	40960 - 43007
44K	A800 - AFFF	250:000 - 257:377	43008 - 45055
46K	B000 - B7FF	260:000 - 267:377	45056 - 47103
48K	B800 - BFFF	270:000 - 277:377	47104 - 49151
50K	C000 - C7FF	300:000 - 307:377	49152 - 51199
52K	C800 - CFFF	310:000 - 317:377	51200 - 53247
54K	D000 - D7FF	320:000 - 327:377	53248 - 55295
56K	D800 - DFFF	330:000 - 337:377	55296 - 57343
58K	E000 - E7FF	340:000 - 347:377	57344 - 59391
60K	E800 - EFFF	350:000 - 357:377	59392 - 61439
62K	F000 - F7FF	360:000 - 367:377	61440 - 63487
64K	F800 - FFFF	370:000 - 377:377	63488 - 65535

Table 2.2

2.4 Extended Addresses

THE LAST MEMORY™ includes decoding for the 8 IEEE 696.1 extended address lines. These 8 extended address lines are used to extend the address space beyond 64K. THE LAST MEMORY™ is active only when the signal on the 8 extended address lines correspond to the setting of the DIP switch.

For systems which generate the 8 extended address signals, the DIP switch setting is defined in Table 2.3.

Address Line	Switch No. *	Setting For 1	0
A_{16}	SW1	ON	OFF
A_{17}	SW2	ON	OFF
A_{18}	SW3	ON	OFF
A_{19}	SW4	ON	OFF
A_{20}	SW5	ON	OFF
A_{21}	SW6	ON	OFF
A_{22}	SW7	ON	OFF
A_{23}	SW8	ON	OFF

* SW1 is at the top of the DIP switch.

Table 2.3

Systems which do not generate the extended address signals may be handled in one of two ways. Open bus lines (undriven by any system board) appear as 1's to THE LAST MEMORY™ and, therefore, if all switches are set to ON the board will be enabled. A second method is to disable the extended address feature by removing the two 74LS136 IC's (IC4 and IC5) as described in SECTION 2.2. The second method reduces power requirements and prevents problems caused by inadvertent switch position changes. If a bus conflict exists (some of the extended address lines are driven, but not by extended address signals) then IC removal is required.

For systems which generate some of the 8 extended address lines, the DIP switch is set according to Table 2.3 with the unused address lines set to ON.

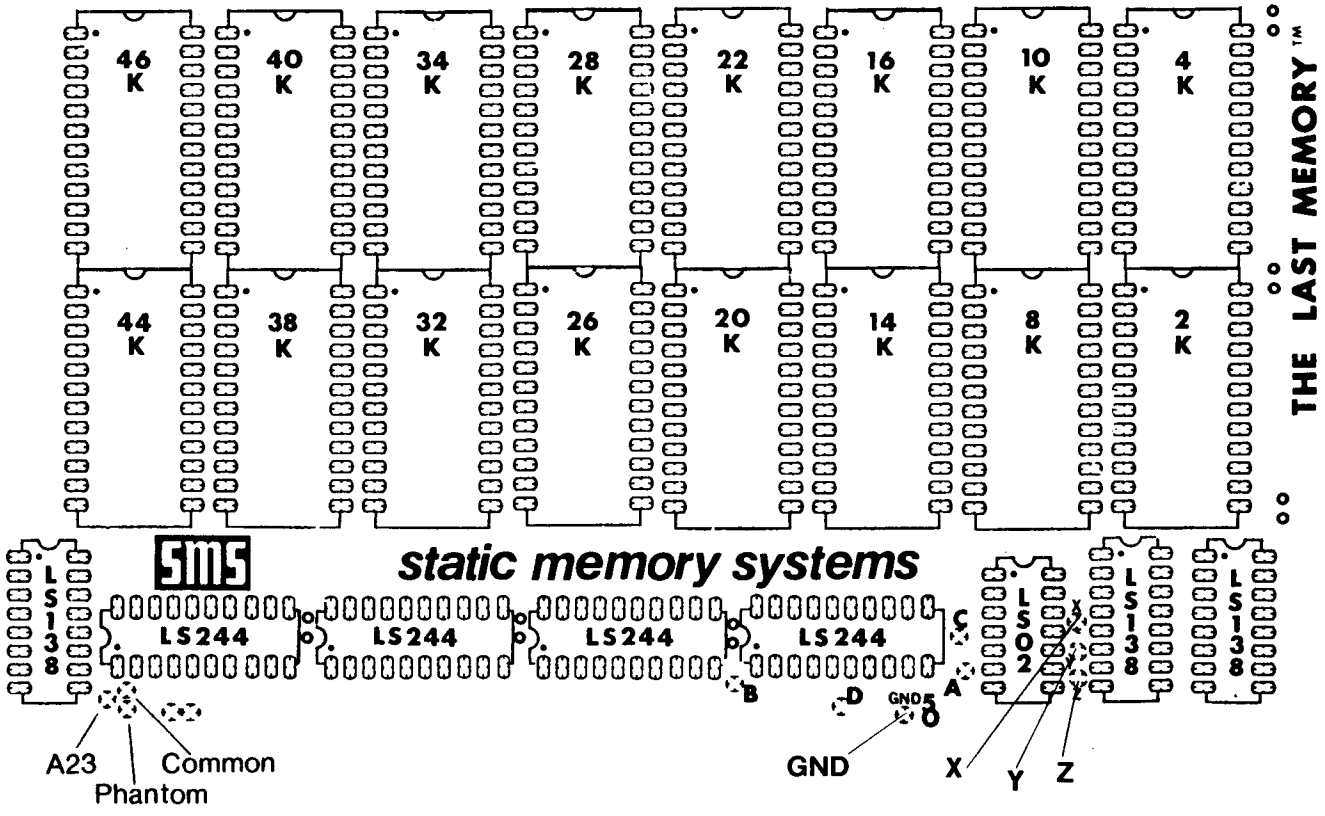


Figure 2.2

2.5 PHANTOM

PHANTOM is jumper selectable in one of four modes: normal bus slave or phantom bus slave (enabling or disabling the entire board when PHANTOM is activated), or phantom write only (enabling or disabling the read function only when PHANTOM is activated).

The first two modes are obtained by disconnecting address line A_{23} and connecting PHANTOM in its place. Referring to Figure 2.2, cut the short copper trace between the point A_{23} and COMMON. Connect a jumper wire between PHANTOM and COMMON. SW8 of the DIP switch will now control the PHANTOM function according to Table 2.4.

Mode	PHANTOM*	SW8 Position
1	LOW - Disables	ON
2	HIGH - Disables	OFF

Table 2.4

The second two modes are obtained by connecting PHANTOM to the read buffer enable circuit. Table 2.5 defines the jumpers required. These modes are most useful for downloading bootstrap programs from read-only-memory which overlaps this memory board. Mode 4 is the most common since it allows downloading only when PHANTOM is active (low).

Mode	PHANTOM*	Jumpers required
3	HIGH - Write Only	PHANTOM to X
4	LOW - Write Only	PHANTOM to Z;X to Y

* Active Low

Table 2.5

If modes 3 or 4 are not used then a jumper from X to ground (GND) is required. Factory assembled and tested boards come with only this jumper installed; none of the PHANTOM modes are connected.

SECTION 3

Board Assembly

3.1 Introduction

Before starting kit assembly, it is strongly recommended that this section be read in its entirety. Although there are many ways to assemble a board, following the instructions below will simplify the procedure.

Care should be taken when handling memory IC's. These are MOS devices and are sensitive to static electricity. They are packaged in conductive plastic or conductive foam which protects them during shipping. Unnecessary handling should be avoided. When inserting them into the board, a grounded insertion tool is recommended. If such a tool is unavailable and the memory IC's must be inserted by hand, a ground strap or wire attached to the fingers or wrist is recommended.

Be sure the tools necessary to build this kit are at hand. Tools required include:

A soldering iron (25 watts maximum)
ROSIN CORE solder (preferably 63/37)
Diagonal cutters
Needle-nose pliers
Screwdriver
A wrench or 1/4" nut driver
Magnifying lens
A small tube of silicone heat sink compound
A piece of cardboard approximately the size of the board

Good soldering practices should be observed. Use a fine soldering iron tip. The tip should make contact with both the component lead and the solder pad. DO NOT OVERHEAT. Do not apply excessive solder - contact is made within the plated-through hole and a large solder cone is not needed.

CAUTION - DO NOT SOLDER OR CLIP COMPONENT LEADS WITHOUT USING SAFETY GLASSES!

If at this point you do not feel completely comfortable with the idea of assembling the kit - STOP NOW! The kit may be returned to Static Memory Systems Inc. for assembly at an additional charge plus shipping and handling. This is a small price to pay as compared to ruining a several hundred dollar kit!

3.2 Assembly

( ) Check the parts received against the parts list (Appendix A). Please report any shortages immediately.

( ) When inserting sockets, be sure to observe the pin 1 notch for proper alignment.

( ) Install all IC sockets before soldering. Install all sockets on the side of the board with the white silk screen. See Parts Layout (Appendix B).

NOTE: No socket is installed in the area marked "DIPSWCH".

( ) Place a piece of cardboard against the component side of the board, hold firmly, and turn over. Press the board down, making sure that all sockets are seated firmly against the board. Inspect to be sure that all pins are sticking through the board. Solder opposite corner pins on each socket - 2 pins only.

( ) Turn the board over and inspect it to determine that all sockets are seated firmly against the board. If any are not flat, melt the solder at the appropriate joint while pressing down. After the socket is reseated, again melt the solder to avoid a cold solder joint.

( ) Solder all IC socket pins.

( ) Install the two single inline (SIP) resistor packs. See Parts Layout for location. Note that a dot marks pin 1, which must be located nearest the bottom of the board (nearest to the gold edge connector). Failure to observe the proper orientation will result in malfunction of the board. Solder.

( ) Install the 13 bypass capacitors (marked .01, 103, or with brown - black - orange dots) at locations shown on the Parts Layout. Solder.

( ) Install the 10µf tantalum capacitor at the location shown. Note that this capacitor is polarized and must be positioned so that the + terminal is inserted in the hole with the + marking. **WARNING!!**

Failure to observe polarity may result in damage to your system. Solder.

( ) Install the two 4.7µf tantalum capacitors at the location shown. Note these capacitors are polarized and must be positioned so that the + terminal is inserted in the hole with the + marking. **Failure to observe polarity may result in damage to your system.** Solder.

( ) Install the DIP switch. Note: switch 1 should be toward the top of the board. Be sure all pins are sticking through the board. Solder.

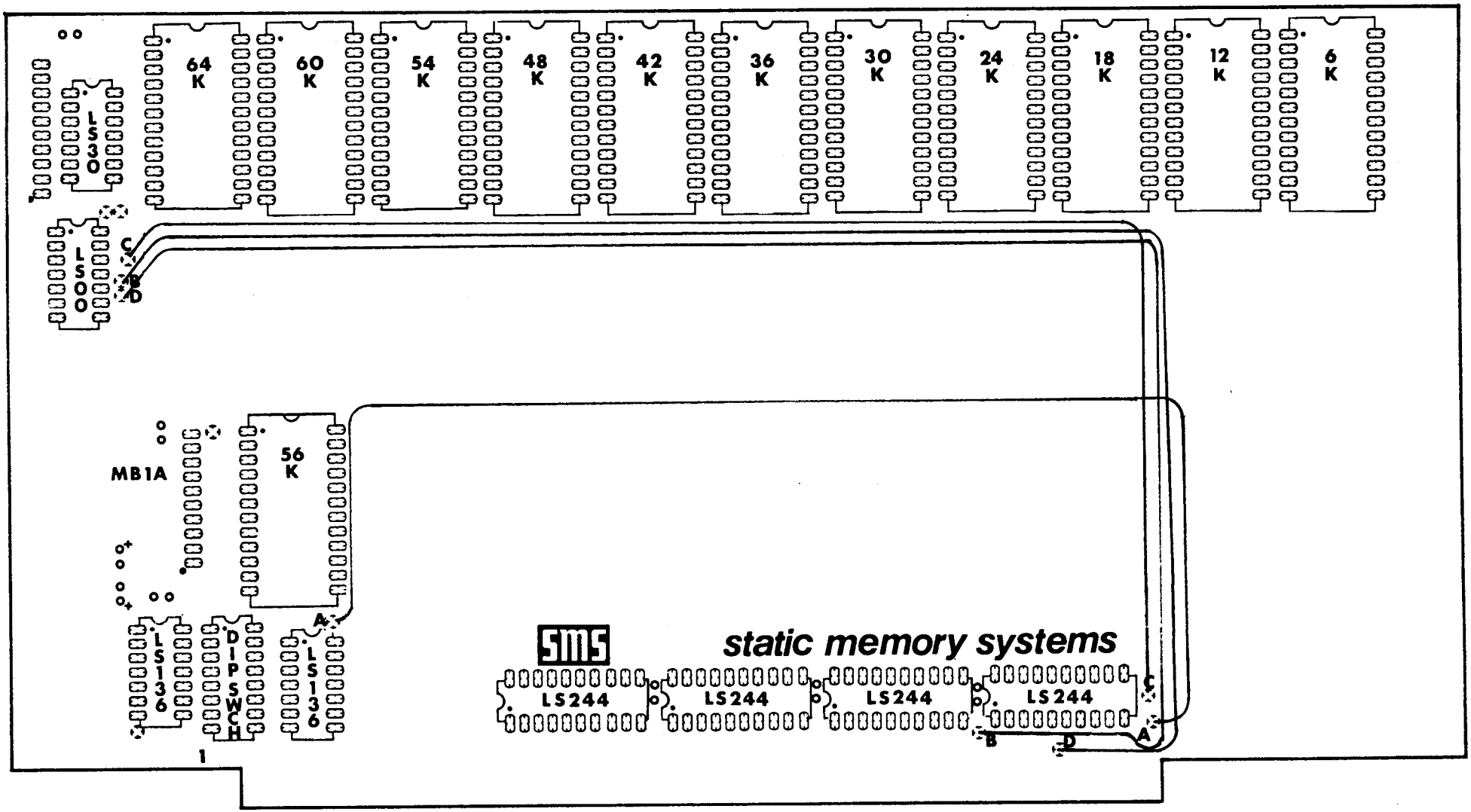
( ) Carefully form the leads of the two 7805 voltage regulators. Apply a thin film of silicone heat sink compound between the board, heat sink, and regulators. Note: too much heat sink compound will do more harm than good. Insert and hand tighten the nuts and screws through the regulators, heat sink, and board. Solder. Tighten the nuts.

( ) Cut and strip the jumper wires according to length shown in Figure 3.1. Install wire 'A' between the two points marked A on the board, routing the wire as shown in Figure 3.2. Solder. Repeat for jumper wires B through D.

JUMPER WIRE	LENGTH (TOTAL)	LENGTH (INSULATION)
A	7 7/8"	7 3/8"
B	12 1/4"	11 3/4"
C	11"	10 1/2"
D	11 7/8"	11 3/8"

Figure 3.1

Figure 3.2

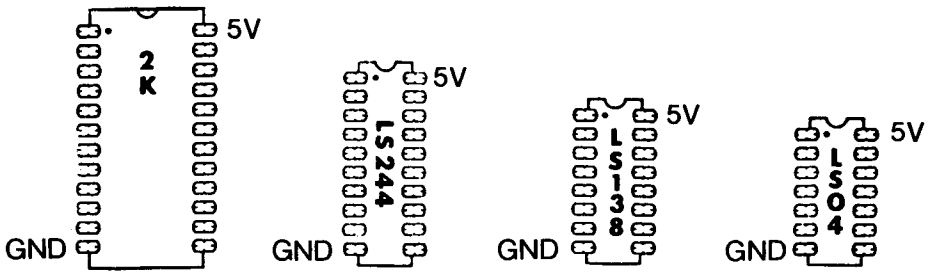

64 K
60 K
54 K
48 K
42 K
36 K
30 K
24 K
18 K
12 K
6 K
LS30
LS00
LS00
C
B
D
MB1A
56 K
LS136
DIPSWCH
LS136
A
SMS
static memory systems
LS244
LS244
LS244
LS244
C
A
B
D
1

( ) After reading SECTION 2.5, decide how PHANTOM is to be used. Jumper wire lengths are shown in Figure 3.3. If mode 3 or 4 are not used, point X must be connected to ground (GND). If point X is left unconnected, the board will not operate properly.

JUMPER WIRE	LENGTH (TOTAL)	LENGTH (INSULATION)
X to GND	1 7/8"	1 3/8"
X to Y	11/16"	3/16"
Y to PHANTOM	6 7/8"	6 3/8"
X to PHANTOM	7 1/8"	6 5/8"

Figure 3.3

( ) Insert the board into an S100 mainframe. Turn on the power switch and check the supply voltage on all IC sockets with a voltmeter. +5 volts should appear between the pin directly across from pin 1 and the last pin on the pin 1 (left) side.



( ) Read SECTION 2. Determine:

( ) S100 Bus Compatibility

( ) Board locations for memory IC's.

( ) Extended address usage

Add jumper wires, as required.

( ) Install all required IC's. Observe pin 1 placement. Inspect to be sure that no pins are folded under an IC; this is the most common problem found in inoperative boards. NOTE: The 7437 should be installed at the location marked 74LS00 (IC2).

( ) Set the DIP switch as described in SECTION 2.

( ) Install the board in a S100 system. If a monitor program is available, deposit and examine at least one byte for every RAM IC used.

( ) The program in SECTION 4 is a more complete test which can also be used for burn in.

SECTION 4

Memory Test Program

4.1 Introduction

The 8080 program which follows, tests memory by writing a bit pattern, reading it back and comparing it with what was written. The bit pattern is generated by incrementing the pattern in the previous address, skipping zero. This program will continue to run until either an error is detected or it is stopped by the user.

FIRST, LAST, and MON must be defined by the user; the values given in the EQU statement are for example only. FIRST is the address of the lowest memory being tested. LAST is the higher order byte (H register) of the address of the last consecutive memory location plus one. MON is the address of the system monitor or a routine capable of displaying the error conditions stored in HIA, LOWA, DWR, and DRD.

This program can only be used to test consecutive memory. If memory is broken by empty sockets, then each group must be tested separately.

```
8080 Macro Assembler, Ver 2.4          Errors = 0

                ************************************************
                      TEST PROGRAM FOR THE LAST MEMORY™
                        STATIC MEMORY SYSTEMS - 06/10/81
                ************************************************

0000                    ORG     0000H
0100                    FIRST   EQU     0100H           ;FIRST ADDRESS
0080                    LAST    EQU     080H            ;HIGH BYTE LAST ADDRESS
F800                    MON     EQU     0F800H          ;MONITOR ADDRESS
0000    AF              START:  XRA     A               ;CLEAR A
0001    47                      MOV     B,A             ;CLEAR B
0002    210001          LOOP:   LXI     H,FIRST         ;START ADDRESS
0005    48                      MOV     C,B
0006    71              STORE:  MOV     M,C             ;STORE DATA
0007    23                      INX     H               ;NEXT ADDRESS
0008    0C                      INR     C               ;NEXT DATA
0009    C20D00                  JNZ     SKIP
000C    0C                      INR     C               ;SKIP ZERO
000D    7C              SKIP:   MOV     A,H
000E    FE80                    CPI     LAST
0010    C20600                  JNZ     STORE           ;CONTINUE BIT PATTERN
0013    78                      MOV     A,B
0014    210001                  LXI     H,FIRST
0017    5E              READ:   MOV     E,M             ;READ BACK
0018    BB                      CMP     E               ;COMPARE
0019    C22E00                  JNZ     ERROR
001C    23                      INX     H               ;NEXT ADDRESS
001D    3C                      INR     A               ;NEXT DATA AS STORED
001E    C22200                  JNZ     ZIP
0021    3C                      INR     A               ;SKIP ZERO
0022    4F              ZIP:    MOV     C,A
0023    7C                      MOV     A,H
0024    FE80                    CPI     LAST            ;TEST FOR LOOP COMPLETE
0026    79                      MOV     A,C
0027    C21700                  JNZ     READ
002A    04                      INR     B
002B    C30200                  JMP     LOOP
002E    223B00          ERROR:  SHLD    LOWA            ;SAVE ADDRESS OF ERROR
0031    323D00                  STA     DWR             ;SAVE DATA AS STORED
0034    7B                      MOV     A,E
0035    323E00                  STA     DRD             ;SAVE DATA READBACK
0038    C300F8                  JMP     MON             ;JUMP BACK TO MONITOR
003B                    LOWA:   DS      1
003C                    HIA:    DS      1
003D                    DWR:    DS      1
003E                    DRD:    DS      1
                        END

NO PROGRAM ERRORS
```

SECTION 5

Theory of Operation

5.1 Introduction

The operation of THE LAST MEMORY™ is straightforward. The memory IC's are static and require no complex on-board timing. This board selects the appropriate memory IC and controls the flow of data to or from this IC.

5.2 Address Decoding

Address lines A_0 through A_{10} are decoded directly by the individual memory IC's. The address lines select one of 2048 bytes of memory internal to the IC. These are buffered by 74LS244 three state gates which are always active.

The balance of the address lines must determine which of the 32 sockets contain the memory location being addressed by the bus. Address lines A_{14} and A_{15} feed the enable pins of four 74LS138 (one of eight decoders). They are connected so that only one of the four decoders is enabled at any one time. Address lines A_{11}, A_{12}, and A_{13} feed the select inputs of the 74LS138's resulting in a single output from the enabled decoder. This decoder output is connected to pin 18 of the memory socket being addressed.

The extended address decode circuitry is connected to a third enable pin on the 74LS138 decoders. Address lines A_{16} through A_{23} are compared with the switch settings on the DIP switch via 8 exclusive-or gates (2-74LS136's). These open collector gates are WIRED-OR to give a signal which can disable all four 74LS138 decoders, thus disabling the entire board.

Note that, unless disabled by the extended address or PHANTOM, one of the 32 sockets is always enabled.

5.3 Write Data Cycle

The write data cycle consists of activating the write data buffer, selecting the appropriate memory IC, and generating a write strobe. The write data buffer (74LS244) allows data to flow from the input data bus onto the board. This buffer is activated when the SW0 signal (Bus Pin 97) is low. The appropriate memory IC is selected by the address decode circuitry as described above. The write data strobe is generated from PWR (Bus Pin 77) and SOUT (Bus Pin 45). When both of these signals are low, pin 21 of the memory socket will be low. For RAM's, pin 21 is the write enable and a low signal allows data to be written. For 2716 EPROM's, pin 21 is the programming pin and the write strobe will disable the EPROM and, as a result, have no effect. However, the EPROM's programming pin will source current which must be sinked by the NAND gate (IC2) which generates the write data strobe. If more than 2 EPROM's are used it may be necessary to substitute a 7437 for the 74LS00. These two IC's are functionally identical, but the 7437 provides approximately six times the current

capability.

	74LS00	74LS37	7437
I_L(ma)	8	24	48

Table 5.1

5.4 Read Data Cycle

The read data cycle consists of selecting a memory IC, generating a read enable, and activating the read data buffer if the memory socket is not empty. The appropriate memory IC is selected by the address decode circuitry as described in SECTION 5.2. The read data enable is generated from SMEMR (Bus Pin 47) and PDBIN (Bus Pin 78). When both of these signals are high, pin 20 of the memory socket will be low, which enables the output of TMM 2016's and 2716's.

The read data enable signal could be used to activate the read data buffer (74LS244) as well. However, if other memory mapped boards (using a part of the 64K memory space) are present, a bus conflict would result, even though the socket corresponding to the conflicting address has been left empty. While the other board was attempting to put actual data on the system data bus, this board would attempt to put FFH (all 1's) on the system data bus.

This potential problem is overcome by using a 74LS30 to determine when an FFH is on the board's internal data bus. The output of the 74LS30 is gated with the read data enable so as to activate the read data buffer only when FFH is not present on the internal data bus. Thus, empty memory sockets will not create bus conflicts and other system boards may occupy the

address locations of the empty sockets.

If the data being read from a memory IC would happen to be an FFH, the read data buffer again would not be activated. However, since other system boards may not occupy this address location, data will appear as an FFH.

If the system contains no other memory mapped devices, the FFH detector can be defeated by removing the 74LS30 IC and placing a jumper across pin 12 and 13 of the adjacent 74LS00 (two pads at top-left of IC2). Remember to reverse this process if memory mapped boards are added to the system at a later date.

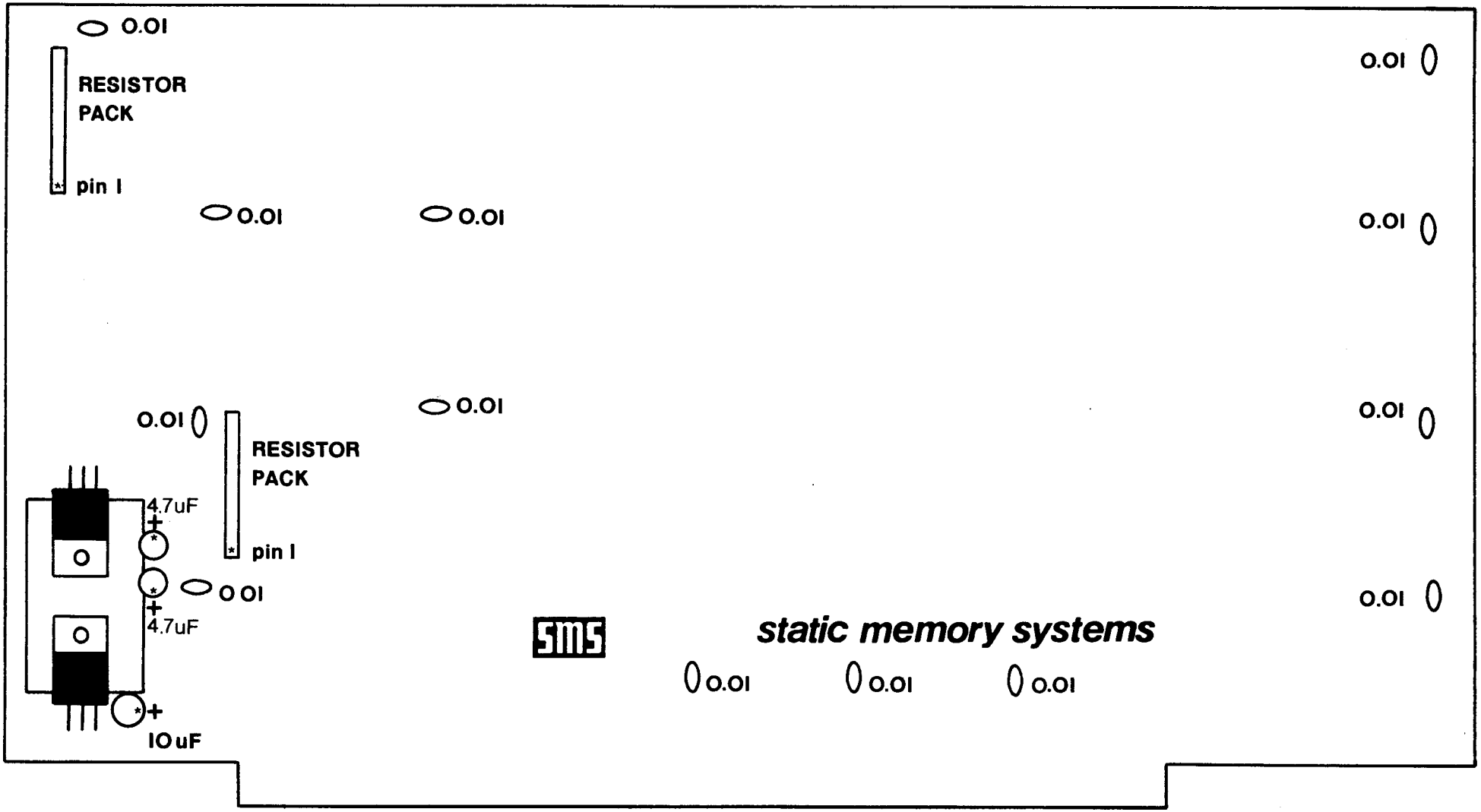
A third signal with input at point X is also gated with the read data enable to activate the read data buffer. If this signal is not used, point X must be connected to ground. It may, however, be used in conjunction with PHANTOM to inhibit reading from this board while allowing writing. If the PHANTOM signal is connected directly to point X, then reading is possible only when PHANTOM is active (low). If the PHANTOM signal is first connected to an inverter (input = Z; output = Y), then reading is inhibited when PHANTOM is active (low). These two connections of PHANTOM correspond to modes 3 and 4 respectively, as described in SECTION 2.5.

APPENDIX A

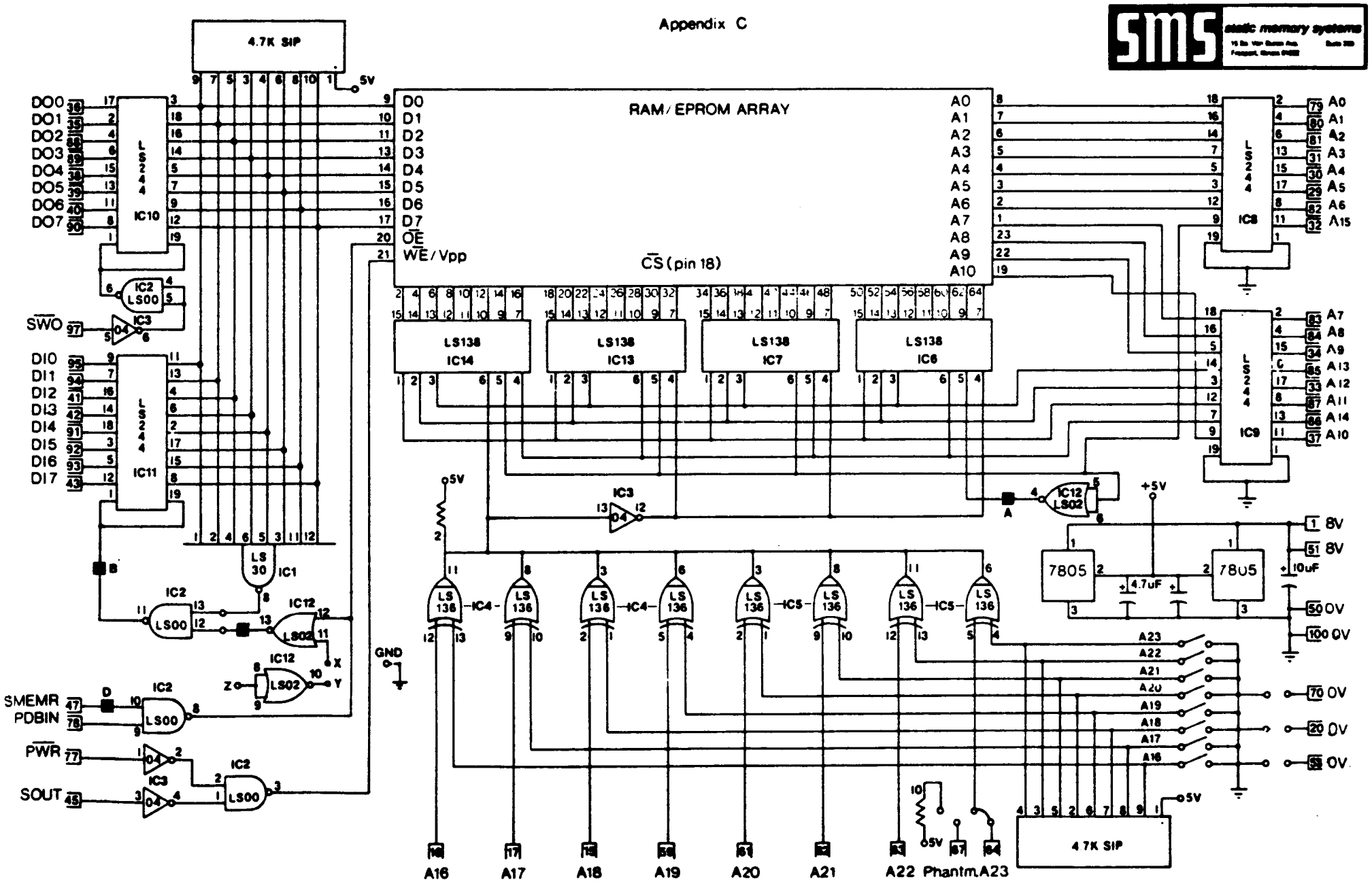
PARTS LIST

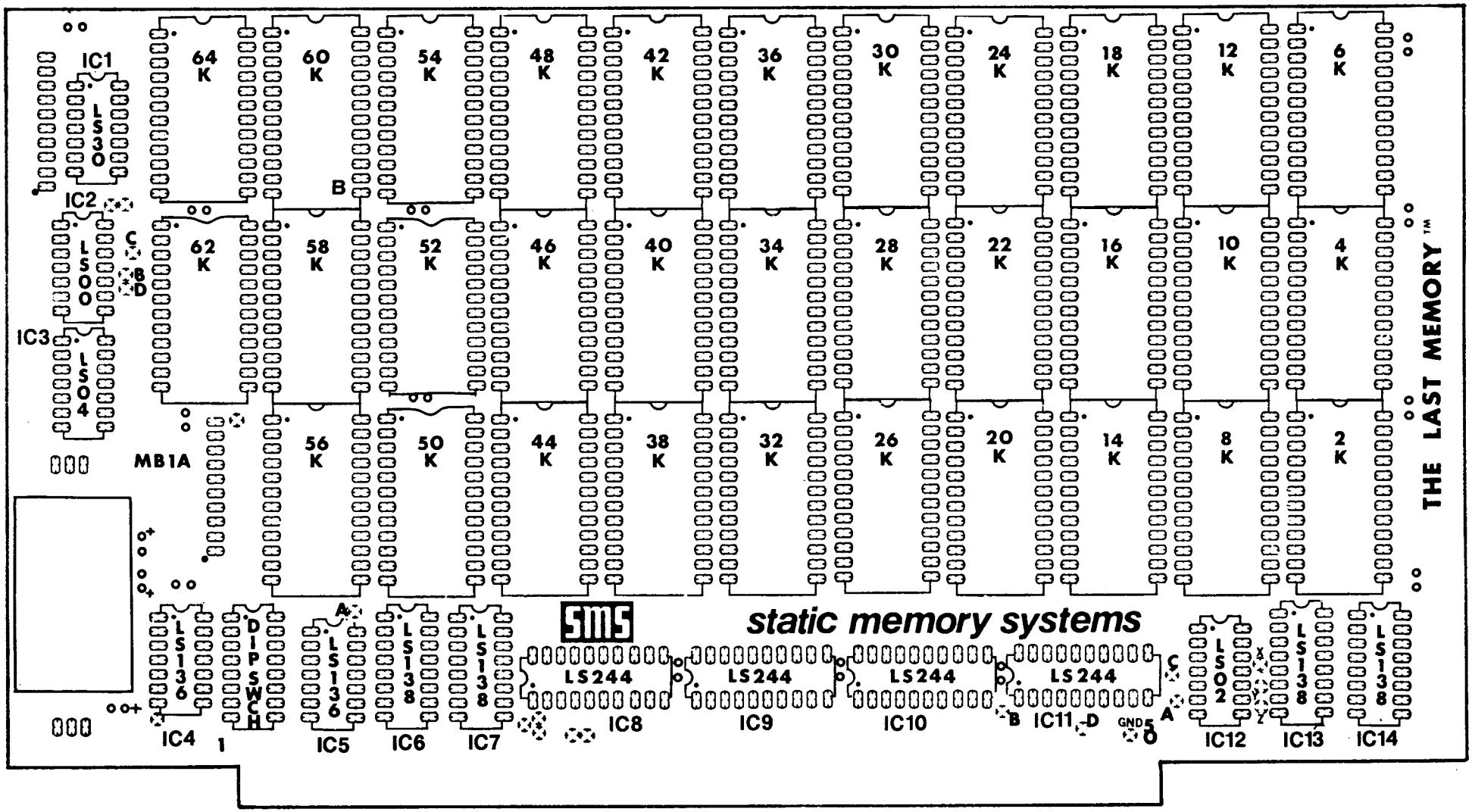
	Quantity	Part
( )	1	74LS00 or 7437
( )	1	74LS02
( )	1	74LS04
( )	1	74LS30
( )	2	74LS136
( )	4	74LS138
( )	4	74LS244
( )	2	7805 +5 volt regulator
( )	1	10µf, 25 volt tantalum capacitor
( )	2	4.7µf, 16 volt tantalum capacitor
( )	13	0.01µf, 50 v capacitor
( )	2	4.7K ohm x 9 SIP resistor pack
( )	32	24 pin socket
( )	4	20 pin socket
( )	4	16 pin socket
( )	6	14 pin socket
( )	1	8 position DIP switch
( )	2	6-32 3/8" screw
( )	2	6-32 nut
( )	1	Heatsink (#367)
( )	--	Jumper wire
( )	--	Memory IC's
( )	1	Printed Circuit Board
( )	1	Manual

Part Placement - Appendix B



Appendix C


4.7K SIP
5V
RAM/EPROM ARRAY
D0
D1
D2
D3
D4
D5
D6
D7
OE
WE/Vpp
CS (pin 18)
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
LS244 IC10
LS244 IC11
LS244 IC8
LS244 IC9
LS138 IC14
LS138 IC13
LS138 IC7
LS138 IC6
DO0
DO1
DO2
DO3
DO4
DO5
DO6
DO7
DI0
DI1
DI2
DI3
DI4
DI5
DI6
DI7
SWO
IC2 LS00
IC3
IC12 LS02
LS 30 IC1
LS 136
IC4
IC5
7805
+5V
8V
10uF
4.7uF
GND
SMEMR
PDBIN
PWR
SOUT
A23
A22
A21
A20
A19
A18
A17
A16
4.7K SIP
A16
A17
A18
A19
A20
A21
A22 Phantm.A23


IC1
LS30
IC2
LS00
IC3
LS04
64 K
60 K
54 K
48 K
42 K
36 K
30 K
24 K
18 K
12 K
6 K
62 K
58 K
52 K
46 K
40 K
34 K
28 K
22 K
16 K
10 K
4 K
56 K
50 K
44 K
38 K
32 K
26 K
20 K
14 K
8 K
2 K
B
C
8
D
MB1A
A
THE LAST MEMORY™
SMS
static memory systems
LS136
DIPSWCH
LS138
LS244
IC4
IC5
IC6
IC7
IC8
IC9
IC10
IC11
IC12
IC13
IC14
GND
5
1

APPENDIX D
S100 BUS DEFINITION

pin 1	*	+8 Volts		pin 51	*	+8 Volts	
pin 2		+16 Volts		pin 52		-16 Volts	
pin 3		XRDY	H	pin 53	**	GND	
pin 4		VIO	L	pin 54		SLAVE CLR	L
pin 5		VI1	L	pin 55		DMA0	L
pin 6		VI2	L	pin 56		DMA1	L
pin 7		VI3	L	pin 57		DMA2	L
pin 8		VI4	L	pin 58		sXTRQ	L
pin 9		VI5	L	pin 59	**	A19	H
pin 10		VI6	L	pin 60		SIXTN	L
pin 11		VI7	L	pin 61	**	A20	H
pin 12		NMI	L	pin 62	**	A21	H
pin 13		PWRFAIL	L	pin 63	**	A22	H
pin 14		DMA3	L	pin 64	**	A23	H
pin 15	**	A18	H	pin 65		NDEF	
pin 16	**	A16	H	pin 66		NDEF	
pin 17	**	A17	H	pin 67	**	PHANTOM	L
pin 18		SDSB	L	pin 68		MWRT	H
pin 19		CDSB	L	pin 69		RFU	
pin 20	**	GND		pin 70	**	GND	
pin 21		RFU		pin 71		NDEF	
pin 22		ADSB	L	pin 72		RDY	H
pin 23		DODSB	L	pin 73		INT	L
pin 24		Ø	H	pin 74		HOLD	L
pin 25		pSTVAL	L	pin 75		RESET	L
pin 26		pHLDA	H	pin 76		pSYNC	H
pin 27		RFU		pin 77	*	pWR	L
pin 28		RFU		pin 78	*	pDBIN	H
pin 29	*	A5	H	pin 79	*	A0	H
pin 30	*	A4	H	pin 80	*	A1	H
pin 31	*	A3	H	pin 81	*	A2	H
pin 32	*	A15	H	pin 82	*	A6	H
pin 33	*	A12	H	pin 83	*	A7	H
pin 34	*	A9	H	pin 84	*	A8	H
pin 35	*	DO1/DATA1	H	pin 85	*	A13	H
pin 36	*	DO0/DATA0	H	pin 86	*	A14	H
pin 37	*	A10	H	pin 87	*	A11	H
pin 38	*	DO4/DATA4	H	pin 88	*	DO2/DATA2	H
pin 39	*	DO5/DATA5	H	pin 89	*	DO3/DATA3	H
pin 40	*	DO6/DATA6	H	pin 90	*	DO7/DATA7	H
pin 41	*	DI2/DATA10	H	pin 91	*	DI4/DATA12	H
pin 42	*	DI3/DATA11	H	pin 92	*	DI5/DATA13	H
pin 43	*	DI7/DATA15	H	pin 93	*	DI6/DATA14	H
pin 44		sM1	H	pin 94	*	DI1/DATA9	H
pin 45	*	sOUT	H	pin 95	*	DI0/DATA8	H
pin 46		sINP	H	pin 96		sINTA	H
pin 47	*	sMEMR	H	pin 97	*	sWO	L
pin 48		sHLTA	H	pin 98		ERROR	L
pin 49		CLOCK		pin 99		POC	L
pin 50	*	GND		pin 100	*	GND	

* Pins used by THE LAST MEMORY™

** Pins used by THE LAST MEMORY™ and discussed in SECTION 2.

H Active high signal. L Active low signal.

APPENDIX E

LIMITED WARRANTY

Static Memory Systems, Inc. (SMS) warrants, to the original purchaser, its products to be free from defects in materials and/or workmanship for a period of one (1) year. In the event of malfunction or other indication of failure attributable directly to faulty workmanship and/or material within 90 days, upon return of the product (postage paid), SMS will, at its option, repair or replace the defective part or parts to restore said product to proper operating condition. All such repairs and/or replacements shall be rendered by SMS without charge for parts or labor when the product is returned within 90 days of the date of purchase. After 90 days, any defective part(s) may be exchanged, during the one year warranty period, but labor will be at the expense of the purchaser. This warranty does not cover malfunction or failure attributable to improper kit building or the use of parts not purchased from SMS.

This warranty will not cover the failure of SMS products which at the discretion of SMS, shall have resulted from accident, abuse, negligence, alteration, shipping damage, or misapplication of the product. While every effort has been made to provide clear and accurate technical information on the application of SMS products, SMS assumes no liability in any events which may arise from the use of said technical information.

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