VECTOR

64K DYNAMIC RAM

User's Manual

64K DYNAMIC MEMORY BOARD

Revision 3

USER'S MANUAL

Revision A
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FOREWORD

Audience This manual is intended for computer distributors, or others with at least a moderate technical knowledge of small computers.

Scope It will describe what the Vector Graphic 64K Dynamic RAM board does in the context of a computer system, how to use the board both in Vector Graphic and in other S-100 systems, and how the board circuitry works.

Organization Each section is written at a uniform level of technical depth. "Perspective" describes WHAT the board does and requires only a moderate knowledge of computer design. "User's Guide" describes HOW to make it do things and assumes the same level of knowledge, plus the ability to solder jumpers and flip switches. "Theory of Operation" discusses WHY the board works and assumes a knowledge of digital electronics.

REPAIR AGREEMENT

The 64K Dynamic Memory Board sold hereunder is sold "as is", with all faults and without any warranty, either expressed or implied, including any implied warranty of fitness for intended use or merchantability. However, the above notwithstanding, VECTOR GRAPHIC, INC., will, for a period of ninety (90) days following delivery to customer, repair or replace any 64K Dynamic Memory Board that is found to contain defects in materials or workmanship, provided:

1. Such defect in material or workmanship existed at the time the 64K Dynamic Memory Board left the VECTOR GRAPHIC, INC., factory;

2. VECTOR GRAPHIC, INC., is given notice of the precise defect claimed within ten (10) days after its discovery;

3. The 64K Dynamic Memory Board is promptly returned to VECTOR GRAPHIC, INC., at customer's expense, for examination by VECTOR GRAPHIC, INC., to confirm the alleged defect, and for subsequent repair or replacement if found to be in order.

Repair, replacement or correction of any defects in material or workmanship which are discovered after expiration of the period set forth above will be performed by VECTOR GRAPHIC, INC., at Buyer's expense, provided the 64K Dynamic Memory Board is returned, also at Buyer's expense, to VECTOR GRAPHIC, INC., for such repair, replacement or correction. In performing any repair, replacement or correction after expiration of the period set forth above, Buyer will be charged in addition to the cost of parts the then-current VECTOR GRAPHIC, INC., repair rate. At the present time the applicable rate is $35.00 for the first hour, and $18.00 per hour for every hour of work required thereafter. Prior to commencing any repair, replacement or correction of defects in material or workmanship discovered after expiration of the period for no-cost-to-Buyer repairs, VECTOR GRAPHIC, INC., will submit to Buyer a written estimate of the expected charges, and VECTOR GRAPHIC, INC., will not commence repair until such time as the written estimate of charges has been returned by Buyer to VECTOR GRAPHIC, INC., signed by duly authorized representative authorizing VECTOR GRAPHIC, INC., to commence with the repair work involved. VECTOR GRAPHIC, INC., shall have no obligation to repair, replace or correct any 64K Dynamic Memory Board until the written estimate has been returned with approval to proceed, and VECTOR GRAPHIC, INC., may at its option also require prepayment of the estimated repair charges prior to commencing work.

Repair Agreement void if the enclosed card is not returned to VECTOR GRAPHIC, INC. within ten (10) days of end consumer purchase.

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SPECIFICATIONS

Capacity:	65,536 8-bit bytes.
Compatibility:	Most Z-80 systems. (Systems not originally shipped with the 64K board usually require modification to use it. See Section II.)
Buffering:	Buffered data input and output.
Access Time:	Compatible with Z-80 at 4 MHz without wait states.
Power Consumption:	0.35A of +8V and 0.30A of +16V, 0.30A of -16V typical.
Phantom:	Output buffer disable compatible with Vector Graphic ZCB Board, which generates phantom in response to Power-on-clear (POC), and Fast Reset.
DMA:	Must not interrupt CPU for longer than $2X10^{-3}$ seconds without generating the necessary refresh signals.
Board Addressing	Jumper to disable either one or both of the two top 8K portions (C000H to DFFFH and E000H to FFFFH.)
Standard Addressing	Manufactured with E000H to FFFFH disabled; thus 0000H to DFFFH enabled.
Bank Select	Switch selectable bank number assigned to each 64K board in a system. System selects a board by outputting a byte via port 40H.
Standard Bank Number	As shipped the board responds to bank number 0. In that state, it is automatically selected when computer is first turned on or RESET key is depressed. If this does not work then make sure bank select switch on board is set to number 0.

I. PERSPECTIVE

1.1 CAPACITY AND COMPATIBILITY

The Vector Graphic 64K Dynamic Memory Board provides up to 65,536 (64K) 8-bit bytes of random access memory.

It can be used in most S-100 bus computer using a Z-80 CPU board. (Minor modifications may be necessary if system was not shipped with this board. See Part II, "User's Guide".) It cannot be used in an 8080 based S-100 system.

1.2 BOARD ADDRESSING

The board can occupy the full 64K of memory, i.e. beginning at 0000H. All systems, however, must reserve some part of the memory space for use by Read-Only-Memory (ROM), and other special functions located on other boards. Usually these functions make use of the top part of the memory space, beginning at E000H.

For this reason, the board includes an option (selectable by jumper) for disabling one or both of the top two 8K portions of the board address space. In other words, you can disable either or both C000H to DFFFH and E000H to FFFFH. Once disabled, the board will not respond to memory reads and writes for the addresses that have been disabled. Therefore, you can make the board respond to one of the following four address spaces:

option	addresses enabled
64K	0000H to FFFFH
56K	0000H to DFFFH
48K + 8K at E000H	0000H to BFFFH and E0000H to FFFFH
48K	0000H to BFFFH

1.3 MULTIPLE 64K BOARDS IN ONE SYSTEM

Up to 8 Vector Graphic 64K Dynamic Memory Boards can be used in a system at one time. Only one of the boards actually responds at any given time, but memory is retained in all boards all the time. This enables creation of a system with up to 512K of memory.

This is accomplished by assigning each such board in the system a bank number from 0 to 7. The desired number is set on a small switch on the board. Software selects the board it wants to address by outputting a byte of data through port address 40H. Thus this port address must not be used in the system for any other purpose.

The 64K board with bank number 0 is always enabled when the system is turned on or the RESET switch (or other source of Power-On-Clear) is depressed.

For this reason, if only one 64K board is in the system, you do not have to output anything through port address 40H if the board is set for bank number 0.

The Vector Graphic 16K Static RAM Board has exactly the same bank selecting capability. Therefore, you can mix Vector Graphic 16K and 64K boards in the same system so long as each board has a different bank number and is selected as described above.

1.4 OPTIONAL RESET

Circuitry has been provided on-board to establish a fast reset circuit. To enable this circuitry requires the addition of three common integrated circuits and a small handful of discrete passive devices. Instructions for installing these are given in section 2.1.1.

1.5 RELIABILITY AND COST-EFFECTIVENESS OF THE BOARD

The Vector Graphic 64K Dynamic Memory Board is clearly a breakthrough in cost effectiveness. This is accomplished by combining compact inexpensive DYNAMIC memory chips with the use of the refresh provisions of the Z-80 CPU. The most recent STATIC RAM boards cost considerably more, take up more space, and require more power. Other dynamic memory boards use complex support logic on the board, rather than the built in features of the Z-80.

In addition to the above features, the Vector Graphic Dynamic Memory Board has proven to be remarkably reliable. Considerable attention was given during design of the board to the elimination of noise. It features a gridded ground plane designed to reduce noise. Accepted design practice was observed in structuring grounds, power supply, and bypass.

II. USER'S GUIDE

In order to understand the User's Guide, you must understand that the 64K DYNAMIC Memory Board (like the Vector Graphic 48K Dynamic Memory Board) has a special requirement not true for a STATIC memory board. In order for dynamic memory to work, the Z-80 CPU must refresh every memory cell on the board every 2 milliseconds. Refresh is simply a process of recalling the contents of the cell and then writing it back out again. If not done, the contents of the cell are lost. This is the price we pay for such low cost, low power, compact memory. The Z-80 will take care of this automatically, so long as certain precautions are taken as discussed below.

2.1 MODIFICATIONS TO THE 64K BOARD AND Z-80 BOARD

This section is concerned with making modifications to the jumpers on the 64K board and CPU board in order to use the 64K board in existing systems. If you are going to use the board in an existing system THIS SECTION IS VERY IMPORTANT.

However, if the 64K board was shipped as a part of a complete Vector Graphic computer, or if it is replacing a Vector Graphic 48K Dynamic Memory Board in a system, then skip this section. Such a system is obviously already set up for use of dynamic memory.

1. REFRESH SIGNAL - This modification is only needed for certain non-Vector Graphic Z-80 CPU boards. It involves installing jumpers to provide the proper RFSH signal, making use of the signal presently coming from your CPU. This is to ensure that a refresh cycle is generated during every instruction fetch cycle. Without this signal, operation is not possible.

2. MWRITE - This modification is not necessary in Vector Graphic systems, but is necessary in any system which has no other source of MWRITE. This would be the case if there is no front panel, and neither the CPU board nor any other memory board can generate MWRITE. If the system has some other memory such as a PROM board, and it works fine without the 64K board, then you do not have to worry about MWRITE on the 64K board. However, if you remove the memory board being replace by the 64K board, and the system then does not work at all even though there is some other memory, then you may have to generate MWRITE on the 64K board.

3. RESET CIRCUITRY (OPTIONAL) - This modification is not required on standard Vector Graphic Systems because the RESET function is handled on the ZCB board. Circuitry has been provided on the board, however, in case the 64K board is used in other than a standard system. If your Vector Graphic system is being modified from static to dynamic for the first time, you will also have to make this modification on the CPU board. The only exceptions are those computers that don't use the PRESET line (pin 75 of the bus) to reset the CPU.

   The modification involves changing the reset circuit of the CPU board so that it responds to the short reset pulse generated by the 64K RAM board on pin 55 rather than responding directly to the $\overline{\text{PRESET}}$ signal on pin 75 generated by the RESET switch. This modification prevents the CPU from being held in a reset state for longer than 2 milliseconds when RESET is depressed. This would result in loss of memory data, since memory is not being refreshed while the CPU is in a reset state.

The above three modifications are discussed in detail below:

2.1.1 Refresh signal (jumper areas A and C)

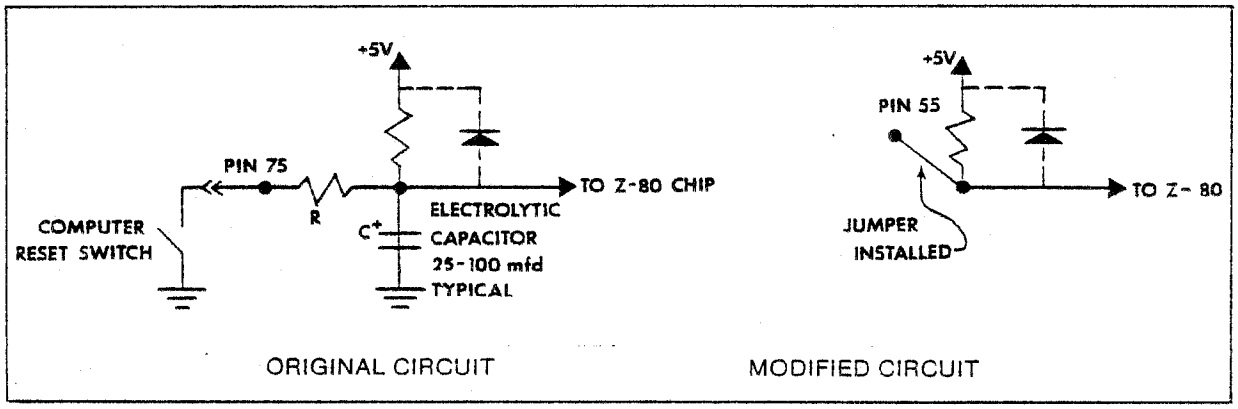
If you are using the 64K board with a non-Vector Graphic CPU board, refer to the manual for your CPU board to determine if the polarity and pin connection of the $\overline{\text{RFSH}}$ signal are correct. This signal is generated by pin 28 of the Z-80 CPU chip and should be buffered onto pin 66 of the bus using a non-inverting buffer of the 8097 or 74367 type.

If this is not the case, it is necessary to modify the jumper arrangement on the 64K board. Area C on the board allows for inverting the polarity of the $\overline{\text{RFSH}}$ signal if it is inverted on the CPU board. Cut the trace between pad 2 and pad 1 and connect a jumper between pad 3 and pad 1. If the $\overline{\text{RFSH}}$ signal is brought to pin 98 on the bus instead of pin 66, a pad is provided on the 64K board. Cut the trace in area A to pin 66 and install a jumper to pin 98.

2.1.2 Reset circuitry

The purpose of this modification is to allow the short (about 200 microseconds) pulse generated by the 64K board on pin 55 (previously unused) to reset the CPU, rather than using the $\overline{\text{PRESET}}$ signal generated on pin 75 by the RESET switch. The short signal on pin 55 is generated by the 64K board in response to the $\overline{\text{PRESET}}$ signal.

The modification is done to the Z-80 CPU boards, NOT the 64K board. A typical reset circuit on a Z-80 CPU board and the necessary modifications are shown below.



Modification to reset circuitry on the system Z-80 board

Remove the Resistor R and Capacitor C from the board. Then connect a jumper from pin 55 to the pad previously connected to the + end of the capacitor.

The above gives the general idea. The specific modifications for each of four particular Z-80 boards are given below. If your Z-80 board is not one of these, then you will have to use the general description and drawing given above to determine how to modify it.

Vector Graphic ZCB boards

The ZCB single board computer handles the reset function. The 64K reset circuitry is not needed. It is shipped disabled for this reason.

To enable the optional reset circuitry on the 64K dynamic memory board, the following components must be soldered to the points indicated. It is suggested that all integrated circuits be socketed. Be sure to observe polarity on the electrolytic capacitors. Use a low wattage (25W) soldering iron. Orient the IC's so that the notch on one end matches the notch silk screened on the IC outline on the board. If you are unfamiliar with this kind of work, we recommend you contact your dealer.

Component #	Type	Value	Comment
U17	I.C.	74LS74	
U18	I.C.	74121	
U32	I.C.	7406	
R20	Resistor	4.7K Ohms	5% -1/4W
R21	Resistor	27 Ohms	5% -1/4W
R19	Resistor	6.8K Ohms	5% -1/4W
R1	Resistor	2.7K Ohms	5% -1/4W
C13	Capacitor	100 uF	25V Electrolytic
C12	Capacitor	100 uF	25V Electrolytic
C10	Capacitor	.01 uF	50V Ceramic Disk

Vector Graphic Revision 1 Z-80 boards

On the Z-80 board, install a jumper between pin 55 and the junction of the 220 ohm and 180 ohm resistor connected to the emitter of the 2N3643 transistor. This junction will be found near the upper right-hand corner of the Z-80 board schematic. Then, remove the 100 ohm resistor and the capacitor which are connected to pin 75.

Vector Graphic Revision 2 and later Z-80 boards

The relevent circuitry is the same as Revision 1, but jumper pads are provided for this modification. Simply cut the trace in area D and tie pad E to pad F. These pads are all found at the bottom edge of the board.

North Star Z-80 Board

1. Remove capacitor C21
2. Remove resistor R17
3. Connect a jumper from IC "7G" pin 5 to pin 55 of the S-100 edge connector.

   No modifications for the $\overline{\text{RFSH}}$ signal are needed for the North Star Z-80 board.

Cromemco "ZPU" Board

1. Bend pin 11 of U11 out of the way, and then return U11 to its socket.
2. Cut the foil going to pin 75 on the S-100 edge connector.
3. Install a jumper from U11 pin 10 to pin 55 of the S-100 edge connector.

For Cromemco "ZPU" boards used in non-Cromemco systems that use Power-on-clear ($\overline{POC}$) for RESET (e.g. Vector Graphic systems, North Star systems, etc.) perform the following steps in addition to the above.

4. Bend pin 9 of U23 out of the way, and then return U23 to its socket.
5. Install a jumper from U11 pin 9 to pin 99 of the S-100 edge connector.

No modifications for the $\overline{RFSH}$ signal are needed for the Cromemco ZPU.

2.1.3 MWRITE - jumper area B

To generate MWRITE on the 64K board, install a jumper between pads 1 and 2 in area B.

2.2 OTHER SPECIAL SITUATIONS WHICH COULD CAUSE LOSS OF MEMORY

If the CPU is held in a wait state for 2 mS or longer, the normal refresh sequence will be interrupted which could result in the loss of memory data. Since computers with a front panel use the $\overline{WAIT}$ line to halt program operation, if your computer has a front panel, you may NOT use the front panel when the 64K Board is being used. If you attempt to use the front panel, the system will lose the data in memory.

Caution should also be exercised with PROM programming boards, which typically hold the CPU in a wait state of 600 microseconds during a programming pulse. After every byte programmed, a software loop should execute 128 instructions to ensure refresh. A typical loop is as follows:

```
        PUSH B
        MVI B,80H
LOOP    DJNZ LOOP
        POP B
```

Other common uses of the $\overline{WAIT}$ line are to synchronize disk transfers and to prevent video display glitching. These last two are usually not a problem due to the relatively short wait period, on the order of a few microseconds.

2.3 USING DMA

If you are using DMA along with the 64K board, the DMA must not interrupt the CPU for longer than 2 mS without g the necessary refresh signals.

2.4 ADDRESS OF THE BOARD — JUMPER AREA D

The board can occupy the full 64K of memory, i.e. beginning at 0000H. All systems, however, must reserve some part of the memory space for use by Read-Only-Memory (ROM), and other special functions located on other boards. Usually these functions make use of the top part of the memory space, beginning at E000H.

For this reason, the board includes an option (selectable by jumper) for disabling one or both of the top two 8K portions of the board address space. In other words, you can disable either or both C000H to DFFFH and E000H to FFFFH. Once disabled, the board will not respond to memory reads and writes for the addresses that have been disabled. Therefore, you can make the board occupy one of the following four address spaces:

option	addresses enabled	jumper in area D
64K	0000H to FFFFH	1 to 3
56K	0000H to DFFFH	5 to 3
48K + 8K at E000H	0000H to BFFFH and E000H to FFFFH	4 to 3
48K	0000H to BFFFH	2 to 3

As shown in the above table, a jumper in area D determines the address space occupied by the board. The standard jumpering is listed in the specifications at the beginning of this manual.

2.5 UPGRADING FROM VECTOR GRAPHIC 48K BOARD TO 64K BOARD

If the 64K board is jumpered for the 48K option as described above, it is interchangeable with a Vector Graphic 48K Dynamic Memory Board (assuming the 64K board is set to bank number 0, as is standard.)

More often, you will want to use the board in its 56K option in an existing Vector Graphic system. This requires that all other boards having memory on them be rejumpered or reset for different addressing in that system. This includes the disk controller board, ZCB board, and video (Flashwriter) board (if any).

Further, all operating system level software must be modified to work in the rearranged system. First, you must obtain a copy of the Extended Systems Monitor addressed at E000H. At this writing, this is version 4.1. Second, your operating system diskette or diskettes (CP/M, Word Management System, Word Management Demo, and MZOS) must be modified by Vector Graphic to work in the new system. Last, any other software in PROM on the ZCB board must be modified and put either on disk or reprogrammed on PROM to run at the new locations. Specifically, if your system had word processing in PROM located at E000H or above (such as in MEMORITE systems), this software must be converted to a disk version.

If you order an "update to a 56K system," Vector Graphic will supply you a 64K board (unless you already have one), will furnish complete instructions for readdressing all boards as required, will supply the new Extended Systems Monitor, will modify all system diskettes sent in by the user, and will supply a disk version of MEMORITE to replace the PROM version in existing systems. There is an extra charge for a PROM to disk version of Memorite. Please do not send in system diskettes that you have no intention of using once modified.

2.6 USING MULTIPLE 64K BOARDS IN ONE SYSTEM - "BANK SELECTING"

Up to 8 Vector Graphic 64K Dynamic Memory Boards can be used in a system at one time. Only one of the boards actually responds at any given time, but memory is retained (dynamically refreshed) in all boards all the time. This enables creation of a system with up to 512K of memory.

This is accomplished by assigning each such board in the system a bank number from 0 to 7.

Set the desired number on the dip-switch near the right side of the board (switch S1.) Ignore the white numbers printed on the switch itself and use the numbers printed on the board. First, make sure all the rockers are in the OPEN position (pressed DOWN toward the OPEN label.) Then find the rocker corresponding to the desired bank number, and press it down on the side AWAY from the OPEN label.

Software selects the board it wants to address by outputting a byte of data through port address 40H. Thus PORT ADDRESS 40H MUST NOT BE USED IN THE SYSTEM FOR ANY OTHER PURPOSE when the 64K board is used.

The byte of data corresponding to each bank number is as follows:

bank number	output to port 40H
0	01
1	02
2	04
3	08
4	10
5	20
6	40
7	80

For example, to select the 64K board with bank number 5, execute the following 8080 (or Vector Z-80) assembly language codes:

```
MVI A,20H
OUT 40H
```

The 64K board with bank number 0 is always enabled when the system is turned on or the RESET switch (or other source of Power-On-Clear) is depressed.

For this reason, if only one 64K board is in the system, you do not have to output anything through port address 40H if the board is set for bank number 0.

The Vector Graphic 16K Static RAM Board has exactly the same bank selecting capability. Therefore, you can mix Vector Graphic 16K and 64K boards in the same system so long as each board has a different bank number and is selected as described above.

Before installing a 64K board in your system, make sure you check the setting of the bank select switch. Again, if it is the only main memory board in the system, the top rocker should be pressed away from the OPEN label, and all the other rockers pressed toward the OPEN label.

2.7 MEMORY TEST

This section is relevent if you are using a Vector Graphic computer, or at least the Vector Graphic Extended Systems Monitor in PROM, in addition to the 64K board.

The 64K board can be tested using the Vector Graphic Extended Monitor T command. Install the board in your system and turn the system on. Now look at the table in Section 2.4, above. Figure out what the lowest DISABLED address is. For example, if you are using the 56K option, the lowest disabled address is E000H. Then, type T 0000 XXXX, where XXXX is the lowest disabled address. Using E000H, for example, type T 0000 E000. The T command now prints " ..... " as memory is tested between any two locations you wish to test.

If you are using the 48K option with 8K at E000H, the command is slightly different. Type T E000 C000. C000H is the lowest disabled address in this option. This works because the T test will wrap around back to address 0000H and continue on from there.

After a few seconds XXXX YY ZZ should appear on the terminal indicating that location XXXX could not be written to. XXXX refers to the lowest disabled address. (YY and ZZ can be anything; it does not matter.) The test will automatically repeat, and no addresses other than XXXX should be printed out. If any other address prints, then the board requires service.

Depress the RESET key on the front panel to terminate the test.

III. THEORY OF OPERATION

3.1 THE MEMORY CIRCUITRY

The Vector Graphic 64K Dynamic Memory Board uses the refresh provisions of the Z-80 CPU board, which greatly simplifies the support logic circuitry on the board.

A memory reference cycle begins with the CPU board sending the address over A0-A15. Each of the memory chips contains 16K bits, so 14 address bits must be supplied to the chips. This is done by time multiplexing 7 address inputs. Initially the low order 7 addresses are applied to the chip address inputs by U30. After the address lines have had time to settle, the CPU board issues a memory read signal on SMEMR or a write signal in MWRITE ($\overline{PWR}$ AND SOUT). This signal propagates down a chain of inverters in U13 to initiate a timing sequence which does the following things in order:

1. Generates a low going $\overline{RAS}$ (row address strobe) for the appropriate memory block which is selected by U19 and gates U3, U4, and U20, from the two highest order address lines. This strobe latches the address bits internally in the memory chips.
2. Disables U30, a tri-state driver.
3. Enables U29, applying the second 7 address lines to the chips.
4. Generates a low going $\overline{CAS}$ (column address strobe) which latches the addresses in the memory chips and initiates a timing sequence in the chip to enable the output drivers if it is a read cycle, or to write the data into the selected memory location if it is a write cycle.

If the cycle is a read cycle or M1 cycle, the logic associated with U16 enables the bus driver U53 to place the memory data on the DI bus to be read by the CPU. If the cycle is a write cycle, data on the DO bus is buffered by U54 and made available at the data input pin of the chips. The 74LS244 chips have Schmitt trigger inputs to discriminate against noise.

3.2 THE REFRESH FEATURE

The principal difference between static and dynamic memory is the need to refresh the data stored in a dynamic memory. This is necessary because each bit of data is represented by an electric charge stored on a capacitor in each memory "cell". This charge will gradually leak away due to the finite insulation resistance of the dielectric. In order to restore the amplitude of the charge, it must be periodically read out, amplified, and written back in the same location. This is accomplished, thanks to the ingenuity of the chip designers, by executing a $\overline{RAS}$ only memory cycle for each of the 128 row addresses within a 2 millisecond interval. In other dynamic memory boards, this is done using counters, multiplexers and complicated priority resolving circuitry to interleave refresh cycles with CPU access cycles.

Fortunately, the designers of the Z-80 provided for this requirement by including a 7 bit refresh counter in the chip which is incremented every M1 cycle and by designing the chip to output the count on the address bus during every M1 cycle at a point in time when the address bus is idle. The Vector Graphic Z-80 board outputs a $\overline{RFSH}$ signal on pin 66 of the bus to indicate that a refresh cycle must be initiated. The timing of this signal is modified by U1 and reclocked by the system clock to satisfy the timing requirements of the memory chips. The output of U2-8 is combined at U2-11 with MWRITE NOR SMEMR to generate a $\overline{RAS}$ strobe which is applied to all chips during the refresh cycle.

There are several conditions under which the normal refresh sequence will be interrupted which could result in loss of memory data.

1. if the CPU is held in a wait state for 2 mS or longer.
2. if a DMA device takes control of the bus for more than 2 mS without generating the necessary refresh signals.

Condition 1 would not occur in a Vector Graphic computer, but can occur in a system with a front panel where the $\overline{\text{WAIT}}$ line is used to halt program execution. There are other ways in which this can occur since the $\overline{\text{WAIT}}$ line is a popular way of suspending CPU operation. Caution should be exercised with PROM programming boards, which typically hold the CPU in a wait state of 600 microseconds during a programming pulse. See Section II, "User's Guide," for information on handling this problem with PROM programmers. Other common uses of the $\overline{\text{WAIT}}$ line are to synchronize disk transfers and to prevent video display glitching. These last two are usually not a problem due to the relatively short wait period, on the order of a few microseconds.

Condition 2 does not occur in a Vector Graphic computer since none of the boards use DMA. If you are using DMA along with the 64K board, the DMA must not interrupt the CPU for longer than 2 mS without generating the necessary refresh signals.

3.3 BANK SELECT

The addressing of port 40H by the CPU is detected by gates U31 and U16, producing the $\overline{\text{OUT STROBE}}$ at U16-8. This causes the byte on the data-out lines to be latched into quad latches U42 and U43. The board will be enabled if there is a high at U41-8. This will happen if any of the inputs to it are low. All the open rockers of the bank select switch will be detected as highs by U41. Thus a high on the one closed switch will enable the board, because it is inverted before entering U41.

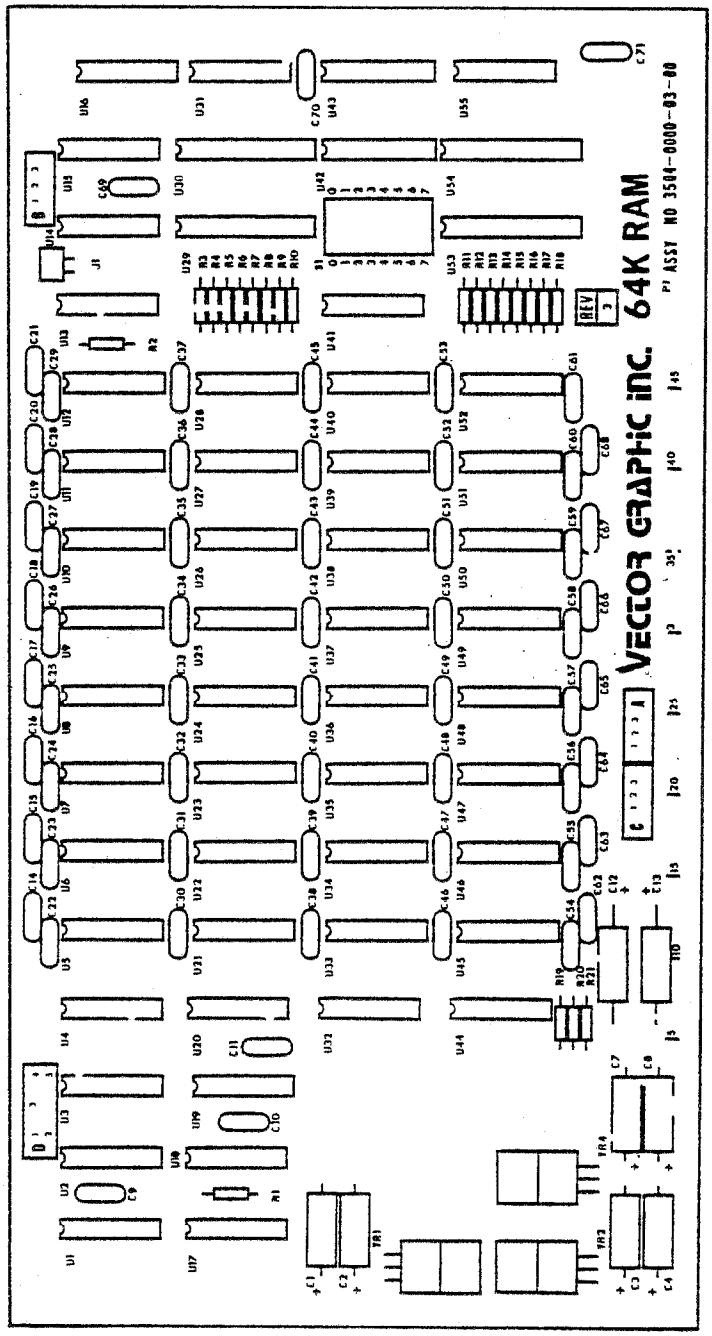
Line DO0 is inverted before U43 so that the non-inverted output at U43-2 can be sent to U41. This enables POC to enable bank 0 by simulating a 1 on line DO0, because $\overline{\text{POC}}$ is connected to the $\overline{\text{CLEAR}}$ pins of U42 and U43.

Bank select signal is inverted by U15 and goes to connector J1. This signal can be used to bank select the Flashwriter II board for Time-Share.

3.4 BOARD ADDRESSING

The board is disabled whenever U20-3, -4, and -5 are all high. U20-3 and U20-4 are both high when the top 16K of memory is addressed. U20-5 is connected to address line A13, A13, VCC, or ground through the jumper in area D. Thus U20-5 is high when one of the top 8K blocks is addressed IF the appropriate jumper is in place.

IV. SCHEMATICS



Layout