into the command register during the RESTORE, in which case the remainder of the steps will occur at the new selected rate until Track 00 is sensed. The minimum pulse width of $\overline{MR}$ is 50 μs.

DATA REQUEST

The Data Request line (pin 38) and the Data Request bit of the status register indicate valid data transfers. When performing any read command, it indicates that valid data is contained in the data register and the host processor may read this byte. In any write command, it indicates that the data register is empty and may be loaded by the host processor with a new data byte. If it is desired to have separate DRQ's to indicate "read" and "write" mode, the circuit of figure 2 may be used. Whenever RG is true, DRQ will be caused by a read operation. When false, DRQ must have been caused by a write operation.

DRQ is always reset when the Data Register is read or written to. DRQ is also reset when the Command Register is loaded with a new command, providing the FD179X is IDLE (Busy = 0).

HEAD LOAD TIMING

The Head Load Output (HLD) controls the movement of the R/W head against the media. When HLD = 1, the head is to be loaded against the disk. An internal 15 ms. delay allows for the head to fully engage. If the drive used requires more head load time, an external circuit must be used to increase this time delay. Figure 3 illustrates the use of a one-shot to perform this function. When the E flag of any Type II or III command is reset (E = 0), the internal 15 ms. delay is disabled and the HLT line is sampled immediately. The duration of the one-shot pulse width set by the Resistor/Capacitor combination selected will prevent a Logic "1" from appearing on HLT until the preset time has expired. The "AND" function of HLT and HLD appears in the status register as BIT 5 and may be used to avoid another time delay by informing the host processor that the R/W head is already engaged. This will speed up access when doing 2 consecutive READ SECTOR commands, for example. Regardless of the head load configuration used, HLT is always sampled for a Logic "1" before the current command is continued.

$\overline{TEST}$ INPUT

The $\overline{TEST}$ input of the FD179X is used when interfacing to voice-coil activated motors. In most applications, it may be tied high or simply left open by the user. When $\overline{TEST}$ = 0, the internal stepping rates are decreased to about 400 microseconds, the HLT internal 15 ms. delay is disabled, and acts as if the E flag was reset. Figure 4 shows a typical implementation of $\overline{TEST}$ when used with a voice-coil activated drive.

$\overline{DDEN}$ INPUT (1791 and 1793 only)

The Double Density Enable ($\overline{DDEN}$) pin is used to select single and double density operation. When $\overline{DDEN}$ = 1, single density is selected; when $\overline{DDEN}$ = 0, double density is selected. This line can be switched from 0 to 1 or from 1 to 0 at any time except when WRITE GATE (WG) is activated. IBM double density diskettes have TRACK 00 side 0 recorded in single density instead of double density. The "ANDING" of the $\overline{TR00}$ and a side 0 signal can be used to force $\overline{DDEN}$ to a Logic "1" when on TRACK 00. The $\overline{DDEN}$ (pin 37) of the 1792 and 1794 must be left open for proper operation.

COMMAND USAGE

Whenever a command is successfully or unsuccessfully completed, the busy bit of the status register is reset and the INTRQ line is forced high. Command termination may be detected either way. The INTRQ can be tied to the host processor's interrupt line, causing a system interrupt with an appropriate service routine to terminate commands. The busy bit may be monitored with a user program and will achieve the same results through software. Performing both an INTRQ and a busy bit check is not recommended because a read of the status register to determine the condition of the busy bit will reset the INTRQ line. This can cause an INTRQ from not occurring.

RESTORE COMMAND

On some disk drives, it is possible to position the R/W head outward past Track 00 and prevent the $\overline{TR00}$ line from going low unless a STEP IN is first performed. If this condition exists in the drive used, the RESTORE command will never detect a $\overline{TR00}$. Issuing several STEP IN pulses before a RESTORE command will remedy this situation. The RESTORE and all other Type 1 commands will execute even though the READY bit indicates the drive in not ready (NOT READY = 1).

READ TRACK COMMAND

The READ TRACK command can be used to manually inspect data on a hard copy printout. Gaps, address marks, and all data are brought in to the data register during this command. The READ TRACK command may be used to inspect diskettes for valid formatting and data fields as well as address marks. Since the 179X does not synchronize clock and data until the Index Address Mark is detected, data previous to this ID mark will not be valid. READ GATE (RG) is not actuated during this command.

READ ADDRESS COMMAND

In systems that use either multiple drives or sides, the read address command can be used to tell the

host processor which drive or side is selected. The current position of the R/W head is also denoted in the six bytes of data that are sent to the computer.

Track	Side	Sector	CRC Length	CRC 1	CRC 2

The READ ADDRESS command as well as all other Type II and Type III commands will not execute if the READY line is inactive (READY = 0). Instead, an interrupt will be generated and the NOT READY status bit will be set to a 1.

FORCED INTERRUPT COMMAND

The Forced Interrupt command is generally used to terminate a multiple sector command or to insure Type I status in the status register. The lower four bits of the command determine the conditional interrupt as follows:

I_0 = NOT-READY TO READY TRANSITION
I_1 = READY TO NOT-READY TRANSITION
I_2 = EVERY INDEX PULSE
I_3 = IMMEDIATE INTERRUPT

Regardless of the conditional interrupt set, any command that is currently being executed when the Forced Interrupt command is loaded will immediately be terminated and the busy bit will be reset indicating an idle condition. Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred.

The conditional interrupt is enabled when the corresponding bit positions of the command (I_3 -I_0) are set to a 1. If I_3 -I_0 are all set to zero, no interrupt will occur, but any command presently under execution will be immediately terminated upon receipt of the Force Interrupt command (HEX D0).

As usual, to clear the interrupt a read of the status register or a write to the command register is required. The exception is when using the immediate interrupt condition (I_3= 1). If this command is loaded into the command register, an interrupt will be immediately generated and the current command terminated. Reading the status or writing to the command register will not automatically clear the interrupt; another forced interrupt command with I_3 -I_0 = 0 must be loaded into the command register in order to reset the INTRQ from this condition.

More than one condition may be set at a time. If for example, the READY TO NOT-READY condition (I_1 = 1) and the Every Index Pulse (I_2 = 1) are both set, the resultant command would be HEX "DA". The "OR" function is performed so that either a READY TO NOT-READY or the next Index Pulse will cause an interrupt condition.

FLOPPY DISK INTERFACE

READ GATE

The Read Gate output from the FD179X is used to inform the external data separator circuitry that a field of ones or zeros has been read off the disk. In FM mode, the RG signal will go high only after the following conditions are met:

1. The Head is loaded
2. HLT is at a Logic "1"
3. Settling time, if programmed, has elapsed
4. A field of zeros has been read off the disk

RG will be reset back to a zero upon a Master Reset ($\overline{MR}$) or upon receipt of any command including the Force Interrupt command when BUSY = 0, or upon a Force Interrupt command when terminating a multiple sector Read/Write command. For double density operation (MFM), the RG characteristics are as follows: Assume the FD1791/3 is searching for an ID field. When 4 consecutive bytes of zeros are detected, RG will be made active. RG will be reset upon any one of the following conditions:

1. 3 A1's with missing clocks not found within 16 bytes
2. HEX "FE" not found within the next byte
3. One byte after CRC
4. Invalid TRACK/SECTOR Address (only during a READ/WRITE sector command)

If the ID search was unsuccessful, the FD1791/3 will then continue the search for the specified ID field. When the correct ID field is encountered and if the current command was a WRITE SECTOR, RG will remain at a Logic "0". If the current command was a READ SECTOR, the FD1791/3 will then look for 4 consecutive bytes of zeros. If 4 bytes of zeros were not found, the FD1791/3 will do an internal retry. If 4 bytes are found within the next 33 bytes, RG will then be set to a Logic "1".

RG is now deactivated (RG = 0) upon one of the following conditions:

1. 3 A1's with missing clocks found within 16 bytes
2. HEX "FB" or "F8" not found within the next byte
3. After the CRC is read (successful completion)

Items 1 and 2 will result in an internal retry. RG is not activated during the Read Track command.

$\overline{VFOE}$/$\overline{WF}$

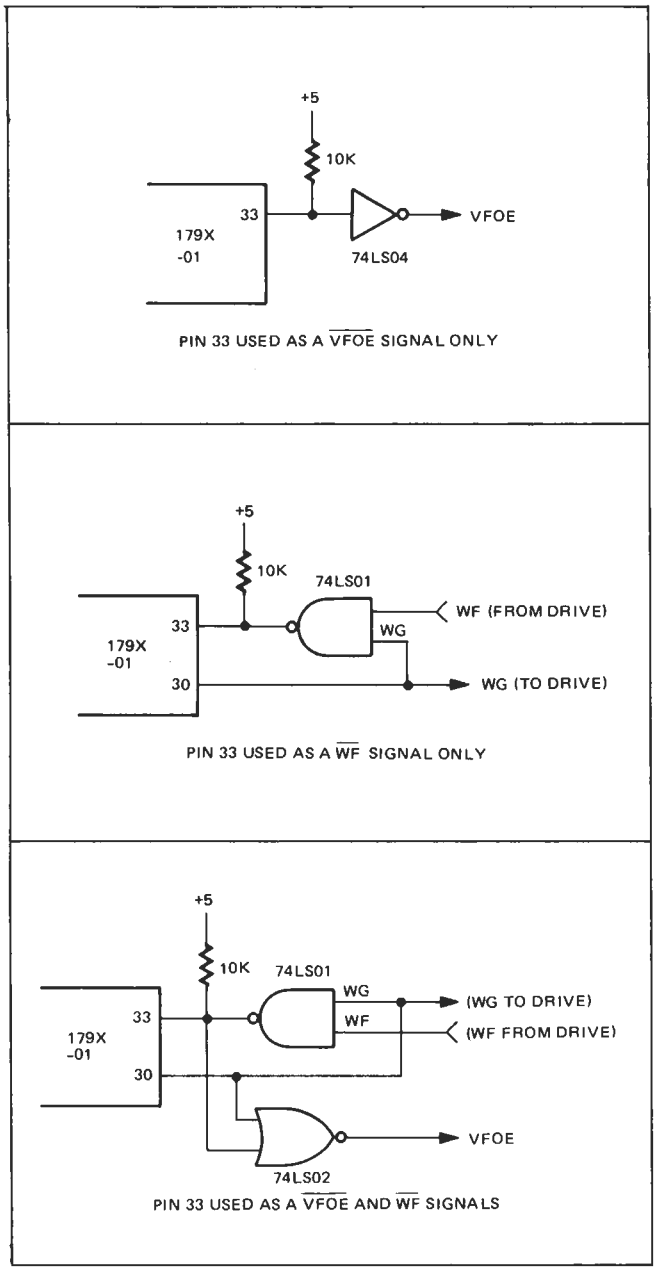
The 179X provides an additional signal that can be used to control the external data separator, $\overline{VFOE}$/$\overline{WF}$ (pin 33) is an input/output pin that functions as a VFO enable and a write fault signal.

When Write Gate (WG) = 1, pin 33 functions as an input to detect write fault conditions at the drive. If pin 33 is brought low when WG = 1, the current Write command is terminated and the INTRQ is activated. The write fault status bit is then set indicating a failure in drive electronics.

When WG = 0, pin 33 functions as an output, pin 33 will go active (Logic "0") when the following conditions are met:

1. Head is loaded
2. Settling time, if programmed, has elapsed
3. Data is being inspected off the disk

The VFOE signal can be used to control RCLK. When VFOE = 0, RCLK should be allowed to free run; when VFOE = 1, RCLK should be forced low. The following circuits can be used to separate $\overline{VFOE}$/$\overline{WF}$ signals.



$\overline{\text{RAW READ}}$

The $\overline{\text{RAW READ}}$ input should be supplied a negative going pulse for every clock or data bit recorded on the media. The normal pulse width is 100 to 200 ns. but may be any pulse width providing the pulse occurs entirely in the read clock window.

When flux reversals are totally non-existant (i.e., head is disengaged), the external separator should ensure that the $\overline{\text{RAW READ}}$ is held at a Logic "1".

RCLK

The READ CLOCK signal must be supplied from an external data separator and is used to "frame" each $\overline{\text{RAW READ}}$ transition. The FD179X will determine whether the $\overline{\text{RAW READ}}$ pulse is clock or data, so the active state of RCLK is unimportant (i.e., high or low during $\overline{\text{RAW READ}}$). RCLK transitions must be phased with $\overline{\text{RAW READ}}$ either by a counter/separator, or phase lock loop configuration.

For proper operation, RCLK must be a minimum of 800 ns. high and 800 ns. low. For 8" MFM, this requires a 50-50 RCLK window. VFO's that operate in the 8-16 MHz range are recommended. When switching RCLK from one source to another, great care must be exercised to ensure this 800 ns. margin. Figure 5 shows the $\overline{\text{RAW READ}}$ and RCLK timing relationships. When $\overline{VFOE}$ = 1 RCLK should be forced low, and free-running when $\overline{VFOE}$ = 0.

WRITE PRECOMPENSATION

Write precompensation is a technique where the WRITE DATA (both clock and data) is written in a direction opposite of the anticipated bit shift. It is generally required for 8" MFM recording and is usually not used for FM single density. Write precompensation may be obtained by the use of external circuitry in conjunction with WD, EARLY and LATE. The algorithm for write precompensation is shown in figure 6. The external logic required is in the form of delay circuits or one shots. As a general rule, write precompensation is done only on Tracks 44-77, but may be required on all tracks if specified by the drive manufacturer.

Figure 8 illustrates a precomp circuit using the Western Digital 2143 4-phase clock generator. The timing relationships are shown in figure 9. The early, late or nominal condition is latched into the 74LS175 on the rising edge of WD. This fires the 2143 via its OSC in (pin 11) line and starts the 4-phase generation. Depending upon the condition, the resultant WD is generated by Ø2 on nominal, Ø1 on early, or Ø3 on late. The Ø4 output resets the latch in anticipation of the next WD pulse. The 7438 is an open collector device and requires a pull-up resistor if not supplied at the drive. A 5K potentiometer is used to adjust the desired pulse width.

DATA SEPARATION

The FD179X requires an external data separator. Data separators range from the counter/one-shot

technique to phase lock loops. The choice of separator design is dependent upon data reliability and system cost.

The FD179X requires a $\overline{\text{RAW READ}}$ signal which is a negative going pulse for every flux reversal, and a Read Clock (RCLK) signal to indicate flux reversal spacing. $\overline{\text{RAW READ}}$ must be a minimum of 100 ns. and RCLK (high or low) at 800 ns. Because of high flux reversal rates, Write Precompensation with a Phase Lock Loop separator is recommended for 8" MFM applications.

Figure 10 illustrates a counter separator. This circuit uses a crystal clock and Read Gate (RG) is not used. Figure 11 shows the timing of the circuit. Any negative $\overline{\text{RAW READ}}$ transition loads the counter with a "5". When the counter counts down to zero, the RCLK flip-flop (74LS74) toggles, producing a RCLK. If the next data bit is zero (no $\overline{\text{RAW READ}}$ pulse), the counter continually counts down until another $\overline{\text{RAW READ}}$ pulse occurs. Then it is loaded again and the process repeats. Many users are using this circuit and are achieving error rates better than 10^{-8}, even for 8" MFM with write precompensation. This circuit may also be used for the 5" mini-floppy.

Figure 12 illustrates a phase lock loop method of data separation. The advantage of this scheme over counter/separators is its excellent data recovery and high reliability. The RCLK "tracks" the $\overline{\text{RAW READ}}$ transitions, allowing for greater flexibility in bit shifts and overall system margins. Although the PPL arrangement is preferred, its added component count generally limits its use to 8" MFM and FM applications.

DATA RECOVERY

Occasionally, the R/W head of the disk drive may get "off track", and dust or dirt may get trapped on the media. Both of these conditions will cause a RECORD NOT FOUND and/or a CRC error to occur. This "soft error" can usually be recovered by the following procedure:

1. Issue the command again
2. Unload and load the head and repeat step
3. Issue a restore, seek the track, and repeat step 1

If RNF or CRC errors are still occurring after trying these methods, a "hard error" may exist. This is usually caused by improper disk handling, exposure to high magnetic fields, etc. and generally results in destroying portions or tracks of the diskette.

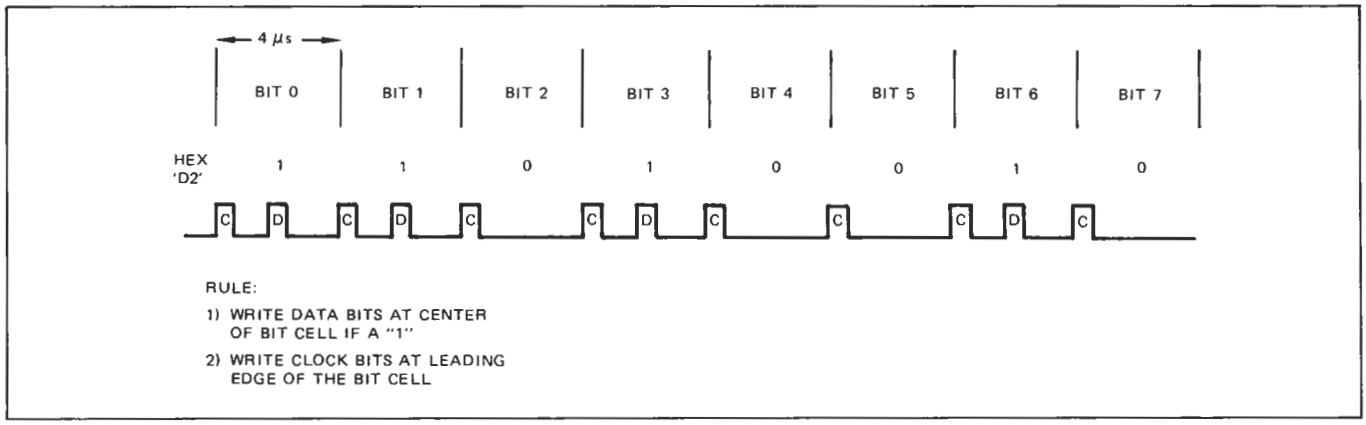


FIGURE 1A. FM RECORDING

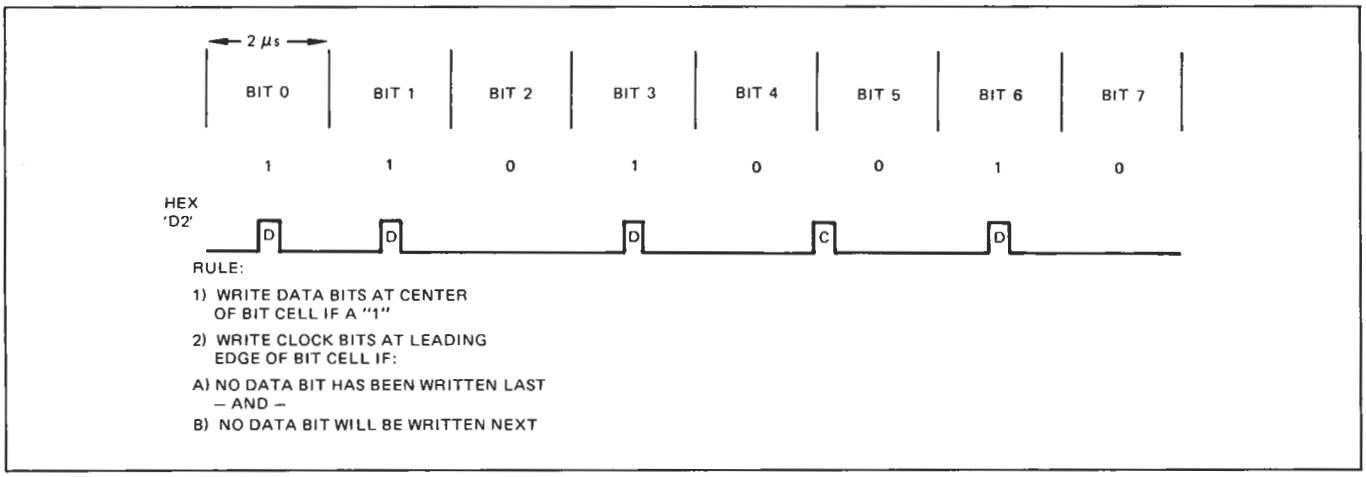


FIGURE 1B. MFM RECORDING

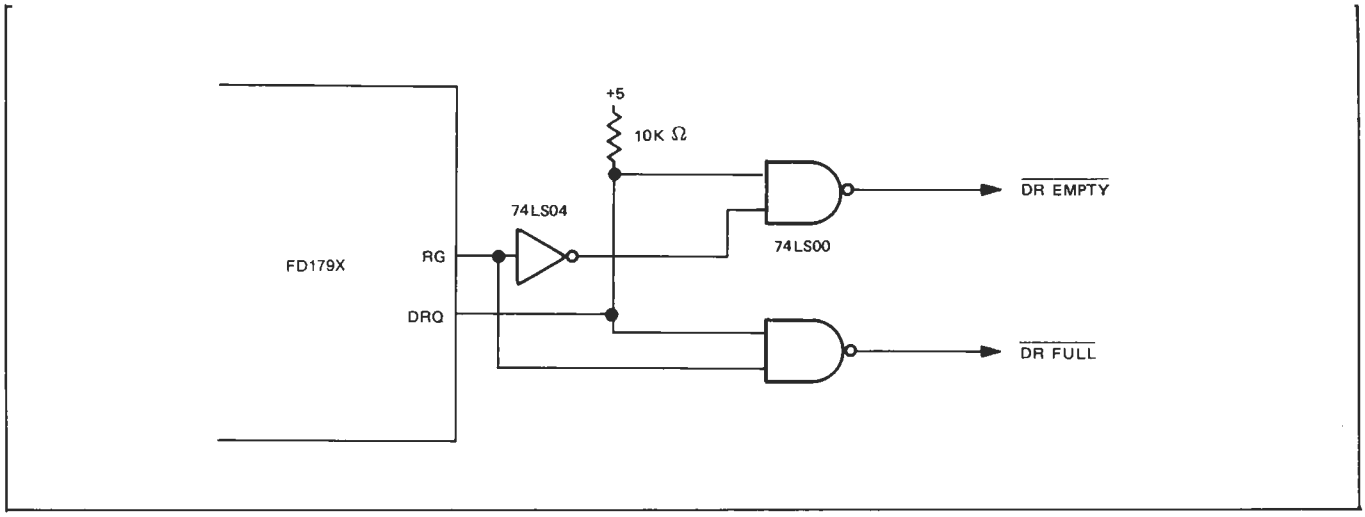


FIGURE 2. FORMING SEPARATE READ AND WRITE MODE SIGNALS FROM DRQ

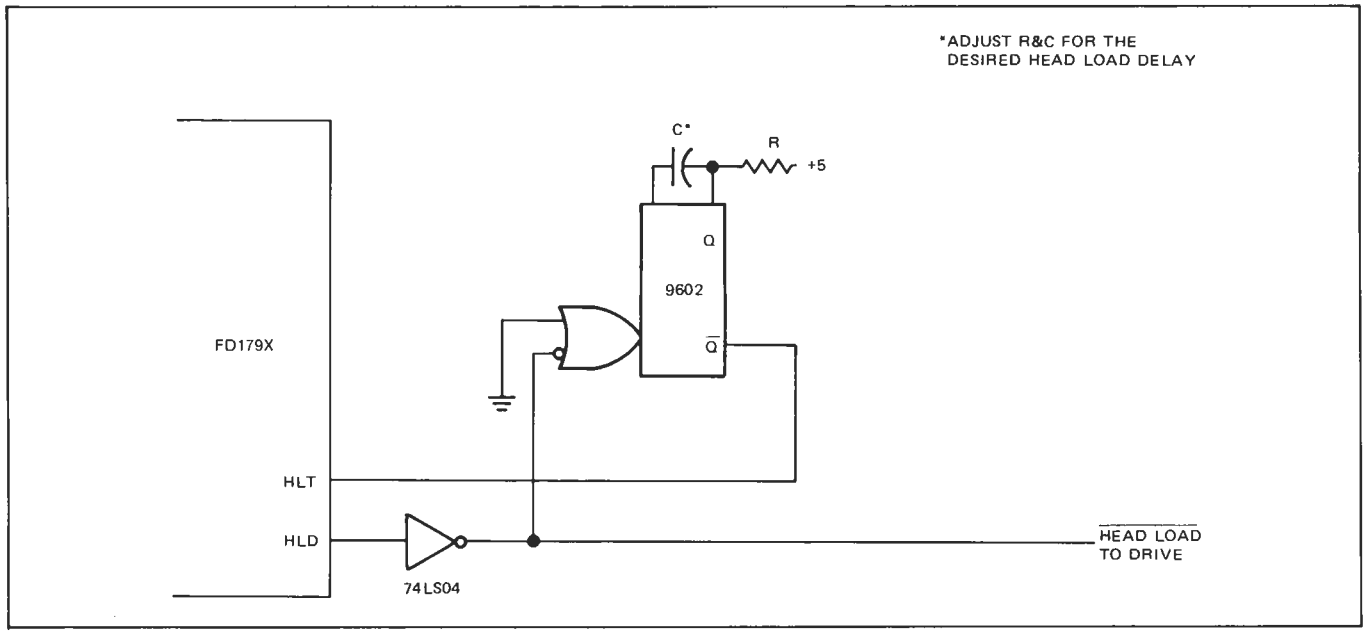


FIGURE 3. CONTROLLING HEAD LOAD TIMING

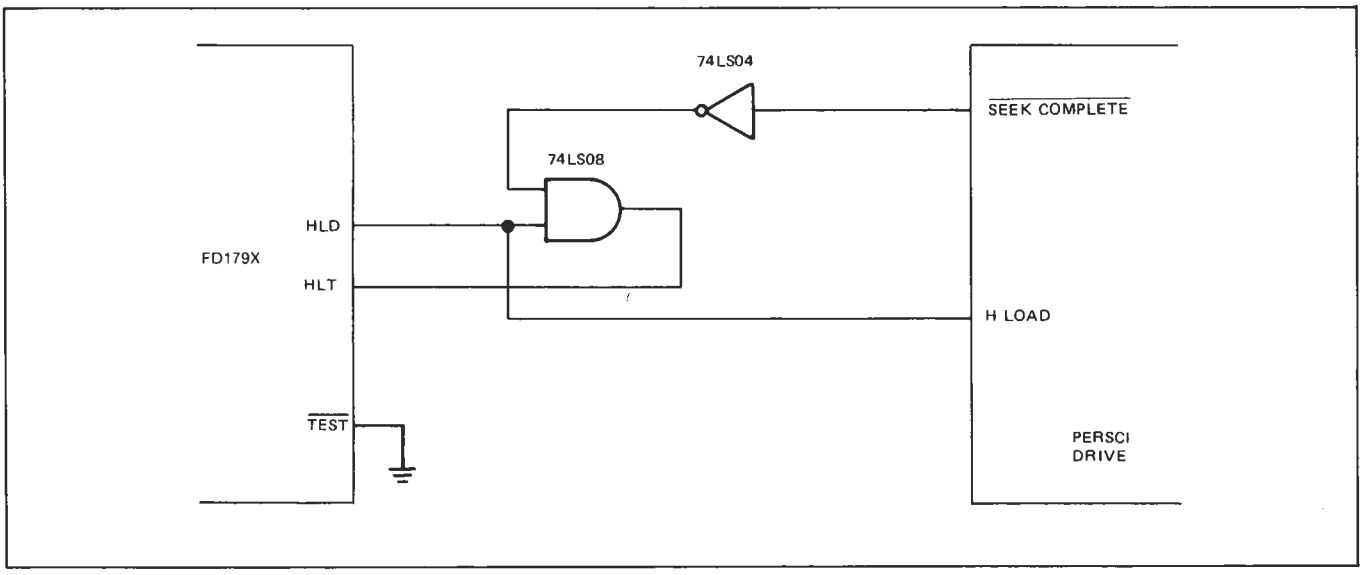
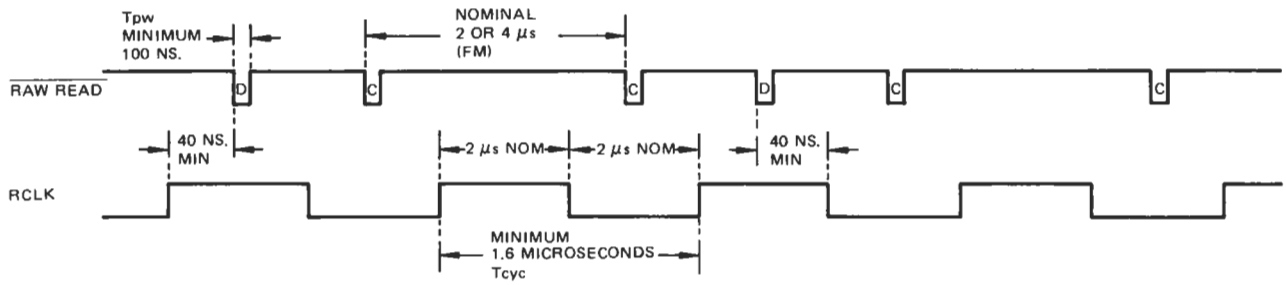


FIGURE 4. INTERFACING TO VOICE-COIL ACTIVATED DRIVES



NOTES:

1) Tcyc SHOULD NEVER FALL BELOW 1.6 MICROSECONDS (50-50 DUTY CYCLE)

2) RCLK MUST BE FREE RUNNING WHEN $\overline{VFOE}$ = 0

3) Tpw MAY OVERLAP IN BOTH WINDOWS IF Tpw < 300 NS. (MFM) OR Tpw < 600 NS. (FM)

FIGURE 5. READ DATA TIMING

Already Sent		Sending	To Be Sent	MFM	FM
X	1	1	0	Precomp Early	Precomp Early [1]
X	0	1	1	Precomp Late	Precomp Late [1]
0	0	0	1	Precomp Early (Inhibit During A1 & C2) [2]	N/A
1	0	0	0	Precomp Late (Inhibit During A1 & C2) [2]	N/A

X = Don't Care
N/A = Not Applicable
1 = Inhibited during missing clocks
2 = With missing clock transitions (Address marks)

FIGURE 6A. INTERNAL WRITE PRE-COMP ALGORITHM

Early	Late	Precomp Required
1	0	Do not Delay WD
0	0	Delay WD By Δ
0	1	Delay WD by 2 Δ

Notes:
All other Early/Late conditions are illegal. Δ = 100 — 150 ns. depending upon drive manufacturer. See figure 7 for timing with Early/Late.

FIGURE 6B. PRE-COMP CIRCUIT REQUIREMENTS

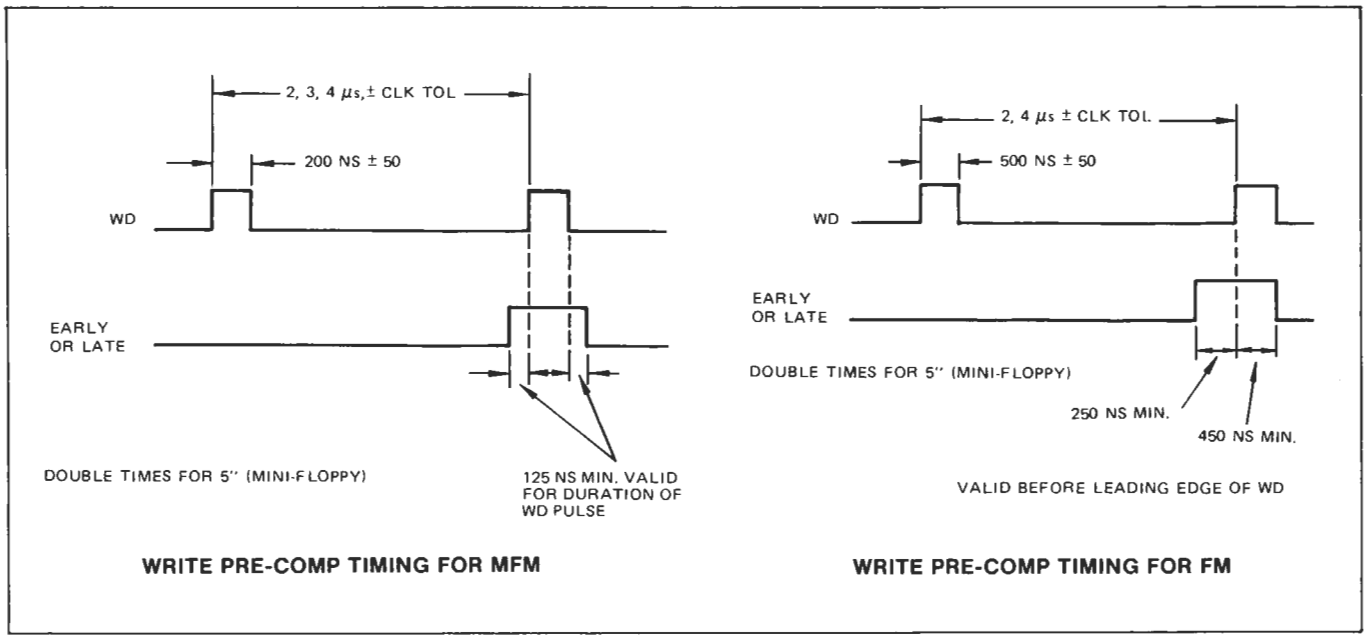


FIGURE 7. WRITE PRE-COMP TIMING

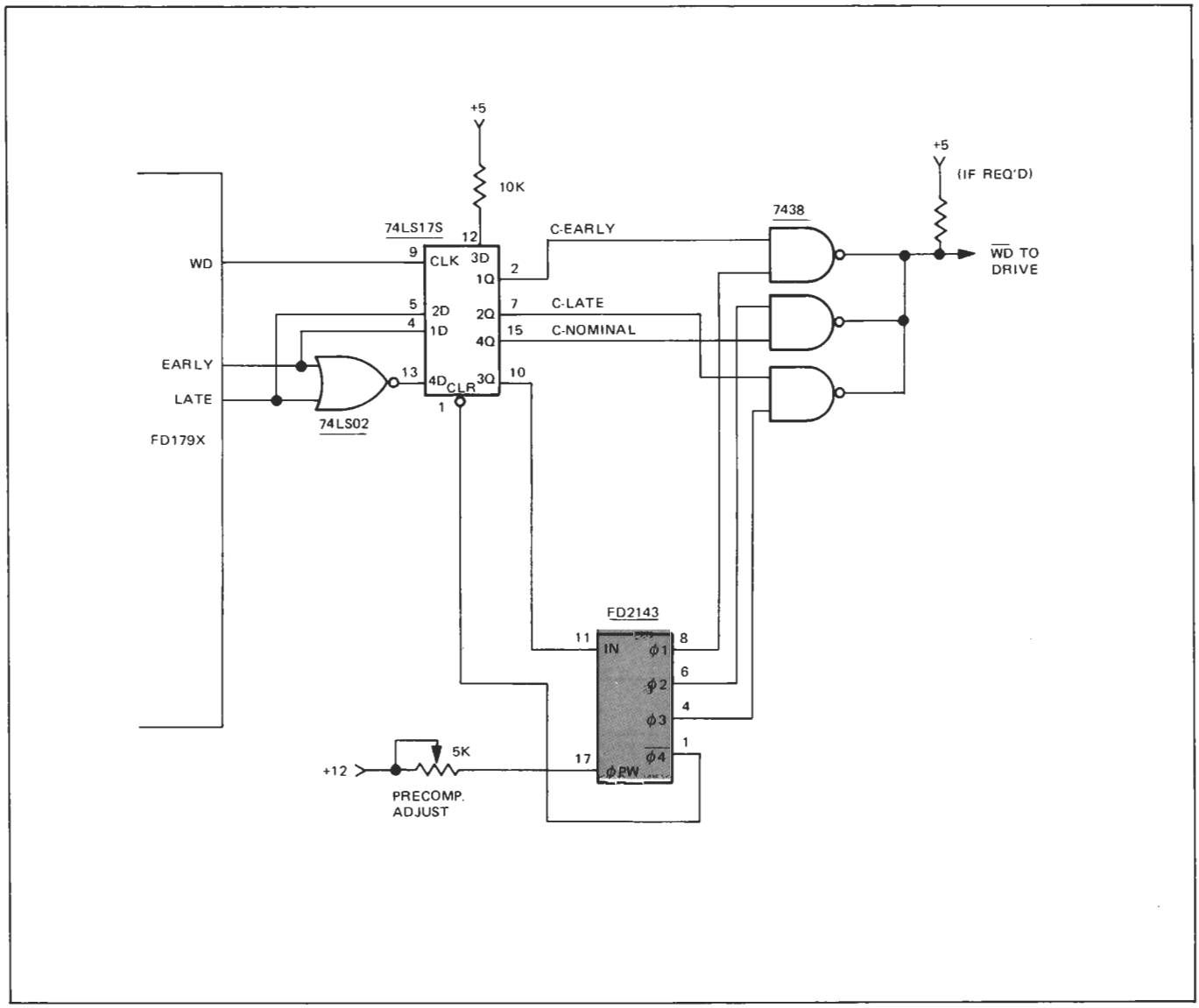


FIGURE 8. 179X WRITE PRE-COMP

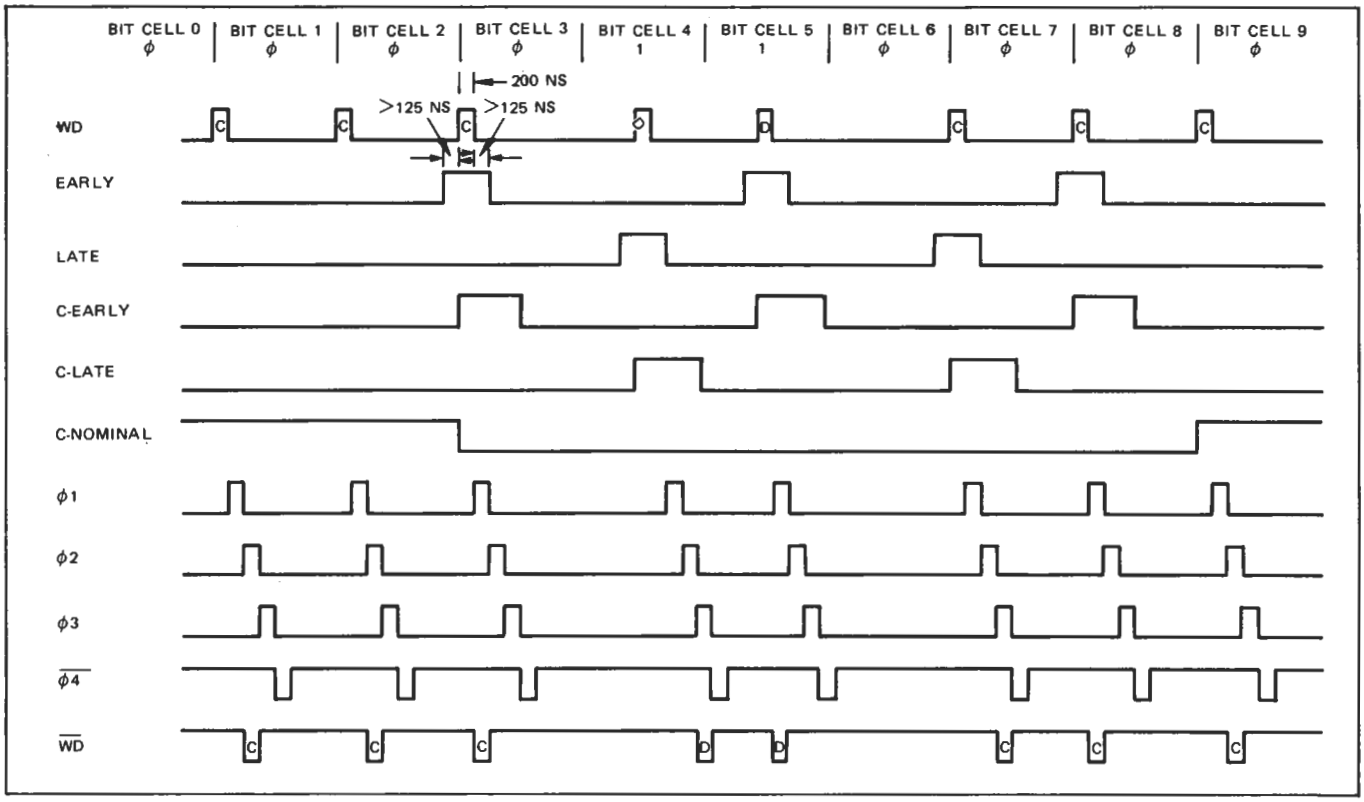
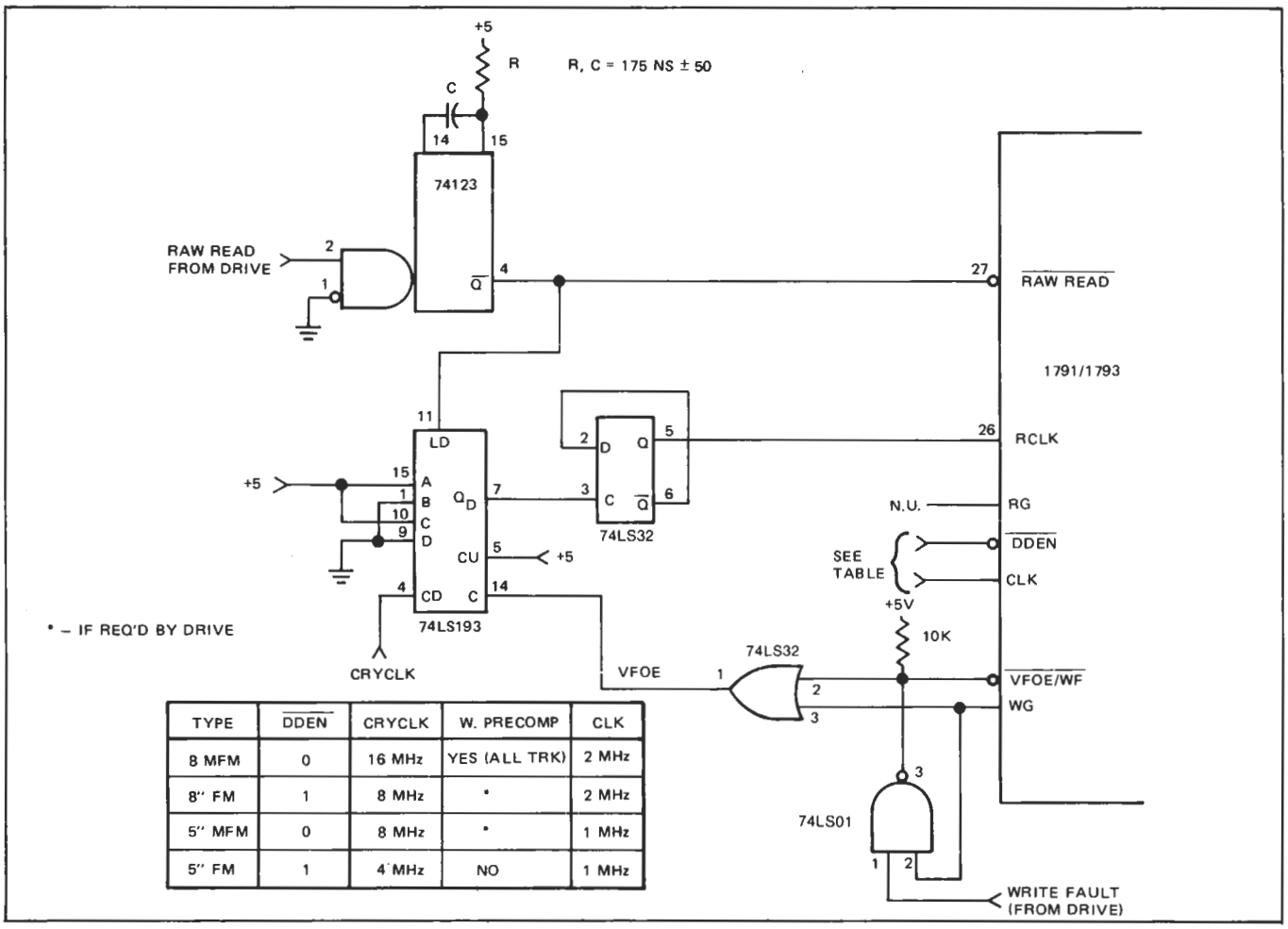


FIGURE 9. WRITE PRE-COMP TIMING



TYPE	$\overline{\text{DDEN}}$	CRYCLK	W. PRECOMP	CLK
8 MFM	0	16 MHz	YES (ALL TRK)	2 MHz
8" FM	1	8 MHz	*	2 MHz
5" MFM	0	8 MHz	*	1 MHz
5" FM	1	4 MHz	NO	1 MHz

FIGURE 10. COUNTER/SEPARATOR

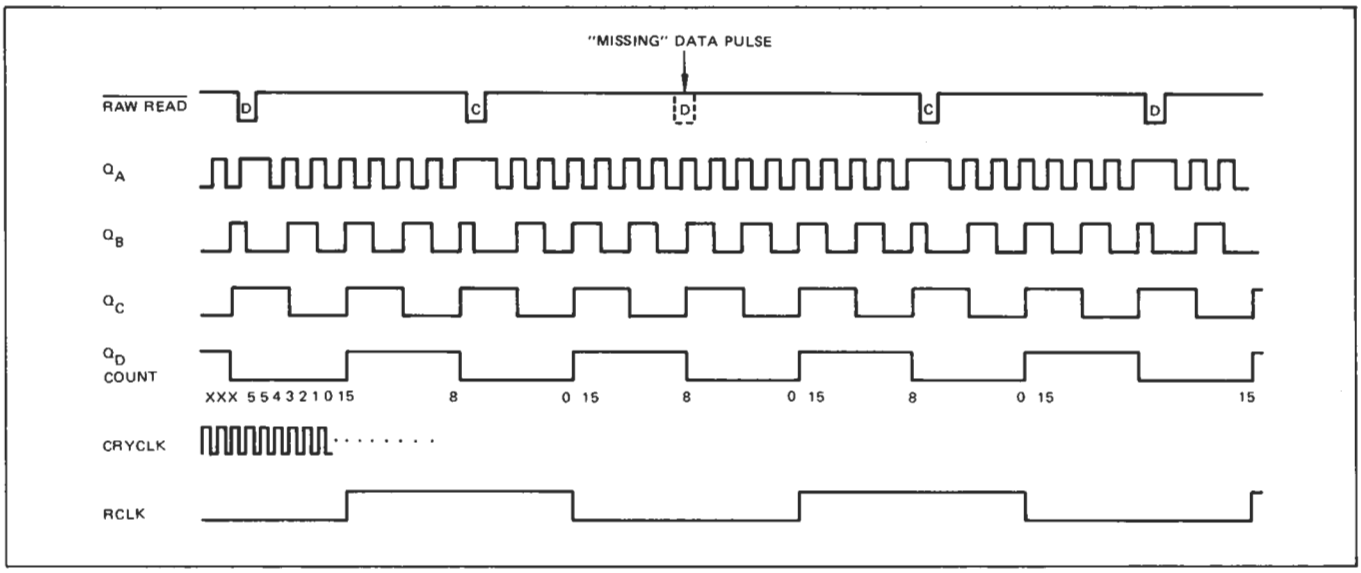


FIGURE 11. COUNTER/SEPARATOR TIMING (8" FM SHOWN)

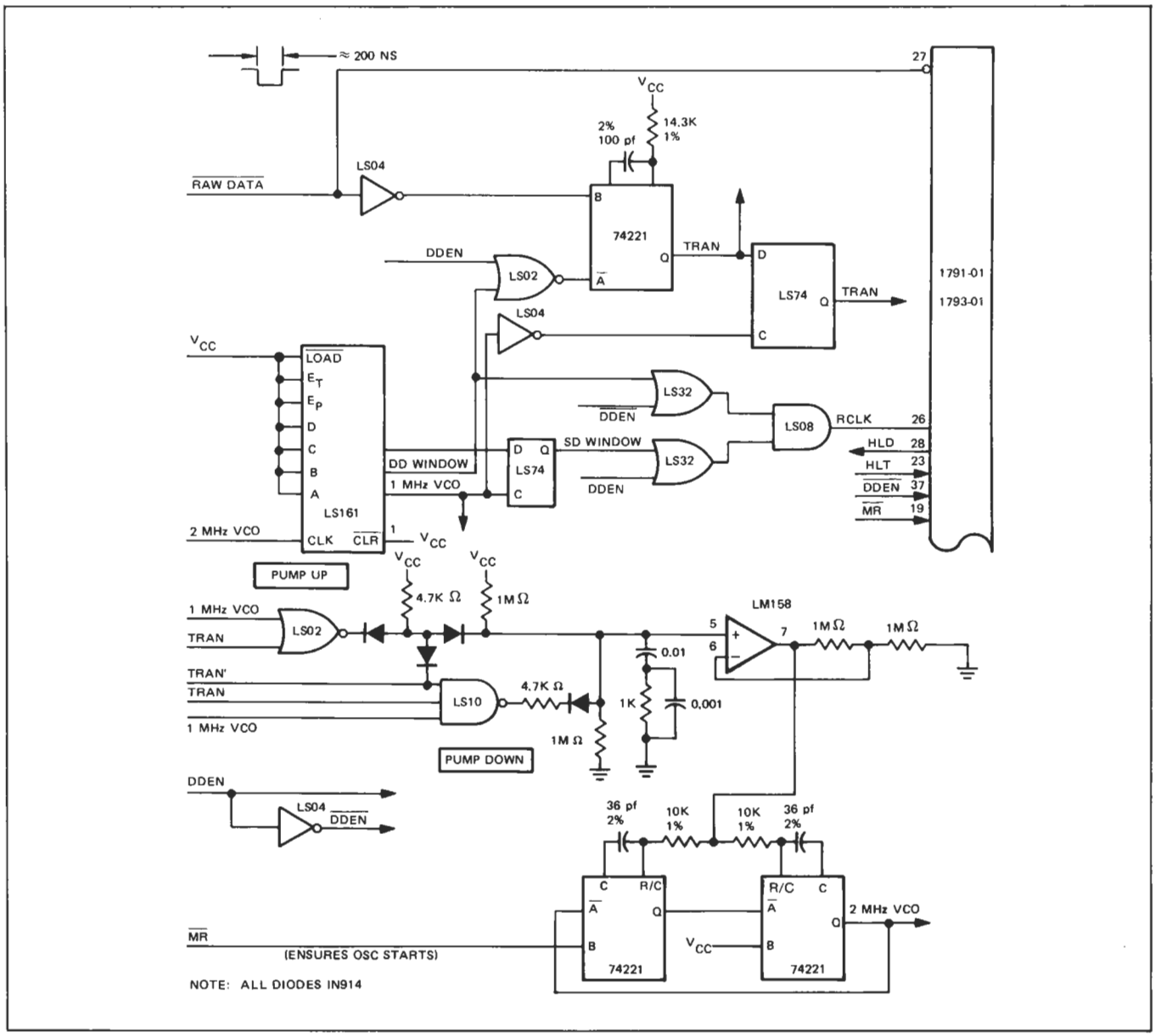


FIGURE 12. ANALOG PLL (FM & MFM) FOR 1791-01 OR 1793-01

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

WESTERN DIGITAL
CORPORATION

3128 REDHILL AVENUE, BOX 2180
NEWPORT BEACH, CA 92663 (714) 557-3550,TWX 910-595-1139

Printed in USA
Document No. A0105

WESTERN DIGITAL
CORPORATION

179X-01 Application Notes

INTRODUCTION

The FD179X Floppy Disk Formatter/Controller performs all the functions necessary to read or write data to any type of floppy disk drive. Both 8" and 5" (mini-floppy) drives with single or double density storage capabilities are supported. These MOS/LSI devices will replace a large amount of discrete logic required for interfacing a host processor to a floppy disk. The FD179X is ideally suited for microprocessor interfacing, either in a stand-alone computer system, or as a slave processor for mini-computer applications. The chip has been designed to be compatible with the IBM 3740 (FM) data format, or IBM System 34 (MFM). Provisions for non-standard variable length sectors have been included to provide more data storage capability per track. Programmable stepping rates via a 2-bit setting in the Command Register allows for interfacing to disk drives with different track-to-track access times. Requiring standard +5V, +12V power supplies, the FD179X is available in a standard 40-pin dual-in-line package.

When $\overline{DDEN}$=1, the FD1791/3 reads and writes data in a frequency-modulated format. Both clock and data are recorded serially on each track of the disk. A data pulse or flux transition recorded between two clock pulses indicates a Logic "1"; the absence of a pulse between clocks indicates a Logic "0". Recorded on each track are unique combinations of data and clock bits called Address Marks. These address marks do not appear elsewhere on the disk and are used for synchronization. Four distinct address marks used are:

Description	Data	Clock
Index Address Mark	FC	D7
ID Address Mark	FE	C7
Data Address Mark	FB	C7
Deleted Address Mark	F8	C7

Figure 1A illustrates a typical recording in FM format. Note that a clock bit is always written before the data bit, regardless if the data written is a 1 or 0. The 1792 and 1794 have been designed for single density applications. Pin 37 must be left open by the user for proper operation.

When the Double Density Enable ($\overline{DDEN}$) pin of the 1791/3 is brought low, MFM recording is enabled. This modified-frequency-modulated technique uses a self-clocking feature to allow for recording at higher densities. Figure 1B illustrates this format. A clock pulse is written to the disk only if the preceding and present data bit written is zero. Without the use of this encoding scheme, recording densities at this higher speed would not be possible.

PROCESSOR INTERFACE

The FD179X contains five internal registers that can read or be written to. These registers are used to write commands, read status, and read and write data to and from the floppy disk. They are selected by a proper binary code on the A0, A1 lines in conjunction with the RE and WE lines when the device is selected. The registers and their addresses are:

$\overline{CS}$	A_1	A_0	$\overline{RE}$ = 0	$\overline{WE}$ = 0
0	0	0	STATUS REG	COMMAND REG
0	0	1	TRACK REG	TRACK REG
0	1	0	SECTOR REG	SECTOR REG
0	1	1	DATA REG	DATA REG
1	X	X	Deselected	Deselected

X = don't care

REGISTER ACCESS

Because of internal clock synchronization, certain delays are required when accessing registers in read and write conditions. These time delays are:

OPERATION	NEXT OPERATION	TIME DELAY REQ'D
Write to Command Register	Read from Status Register	MFM = 4 µs FM = 8 µs Before Status is Valid
Write to Command Register	Read Busy Bit in Status Register	MFM = 6 µs FM = 12 µs
Write to any Register	Read from a Different Register	No Delay Req'd.

Note: All time delays double for mini-floppy (CLK = 1MHz) operation.

MASTER RESET

The $\overline{MR}$ line of the FD179X is used during a power-up condition when processor initialization is to take place. During the trailing edge of $\overline{MR}$, a RESTORE command (HEX 03) is jammed into the command register and executed at the slowest stepping rate. If a faster stepping rate is desired, this can be loaded