

TANDY®

Service Manual

25-3530

Tandy® 1100 FD LAPTOP COMPUTER

Catalog Number: 25-3530

SPECIFICATIONS

Microprocessor	μPD70108-8 (V20), (8088 equivalent)
Clock Speed	8 MHz
Operating System	Includes MS-DOS V3.30
Memory	640 K RAM 8 K ROM for Character Font 32 K ROM for BIOS 512 K ROM for DESKMATE/DOS V3.30
Keyboard	Membrane, XT 101 Emulation, 84 keys
LED Indicator	CHARGE/LOW BATTERY
Display	Reflective type LCD, Green, 640x200 pixels, 80 Charactersx25 lines, Aspect ratio 1:1.6
Disk Drive	One Internal 720 KB (formatted), 3.5 inch Double-sided, 80 tracks
MODEM	Optional 2400-bps, Hayes-compatible mode
External Connections	DC IN 9.5 V Jack DB-25 Parallel Port DB-9 Serial Port
AC Adapter	9.5 Vdc, 2.1 A, UL listed
Battery Type & Life	Lead-acid rechargeable (6 V, 1.8 Ah) 3.0 hours with 10% FDD duty, 4.5 hours without using FDD
Other Features	Battery-Powered Clock/Calendar, Standby Mode and Beeper
Dimensions	12-5/32 (W)x2-7/16 (H)x9-13/16 (D) inches
Weight	6.41 lbs. (2.9 kg)
Temperature	Operating: 41°F~95°F (5°C~35°C) Storage: -40°F~-150°F (-40°C~66°C)
Humidity	Operating: Max. 80% (86°F, 30°C) Storage: Max. 90% (104°F, 40°C)

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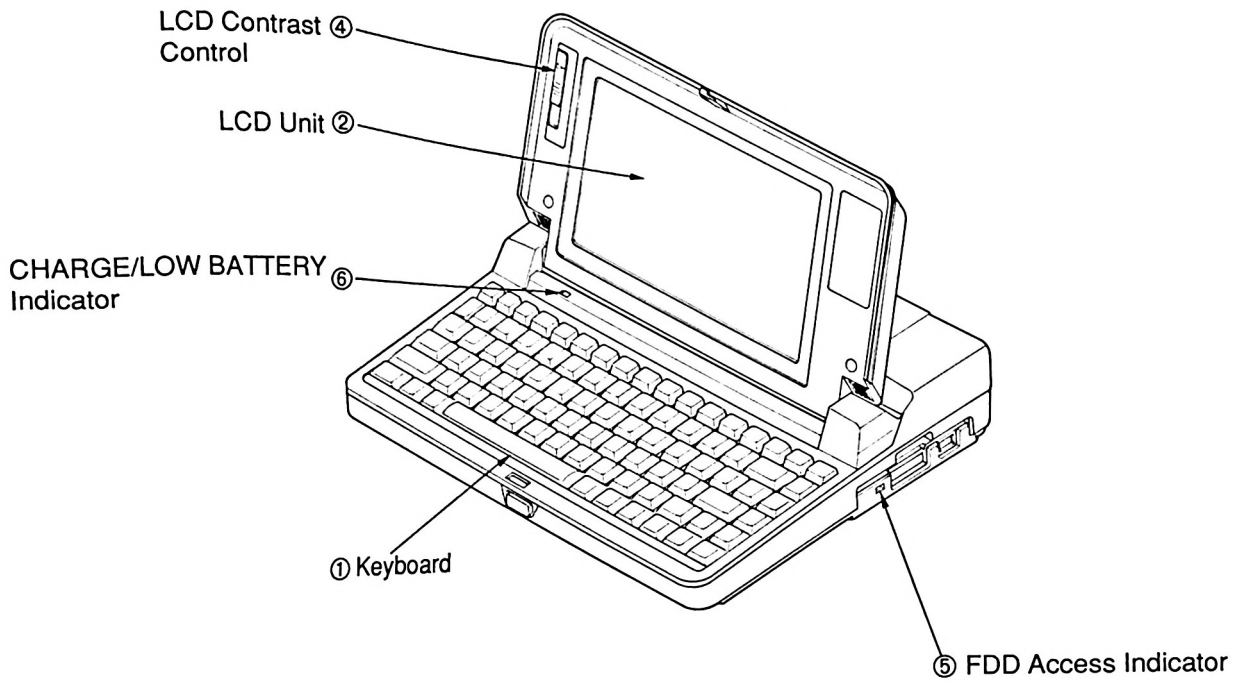


Figure 1-1 Front View

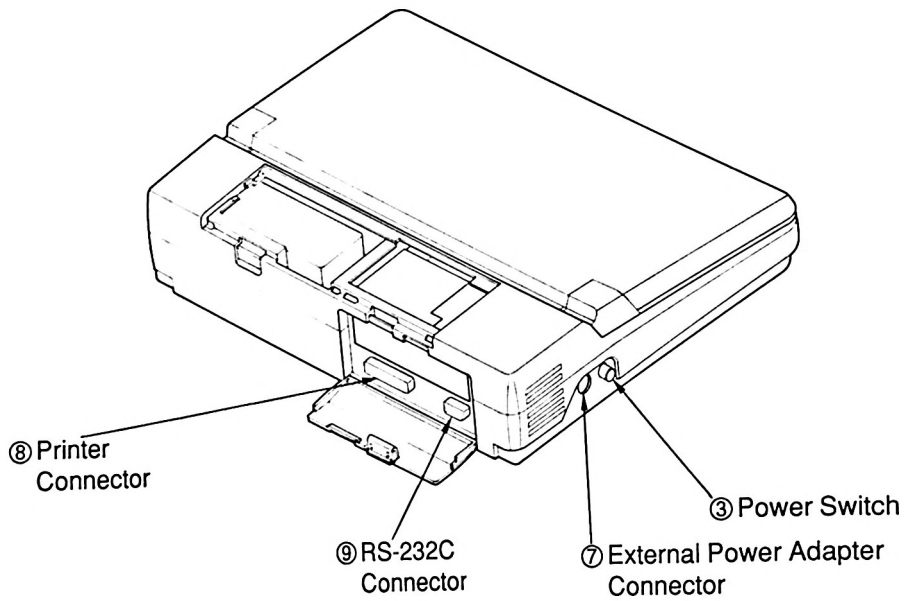


Figure 1-2 Rear View

Internal View

The Tandy 1100FD consists of five printed circuit boards:

- LCD PCB
- Keyboard PCB
- Main PCB
- LED PCB
- FDD PCB

(Main electrical components are shown in this figure.)

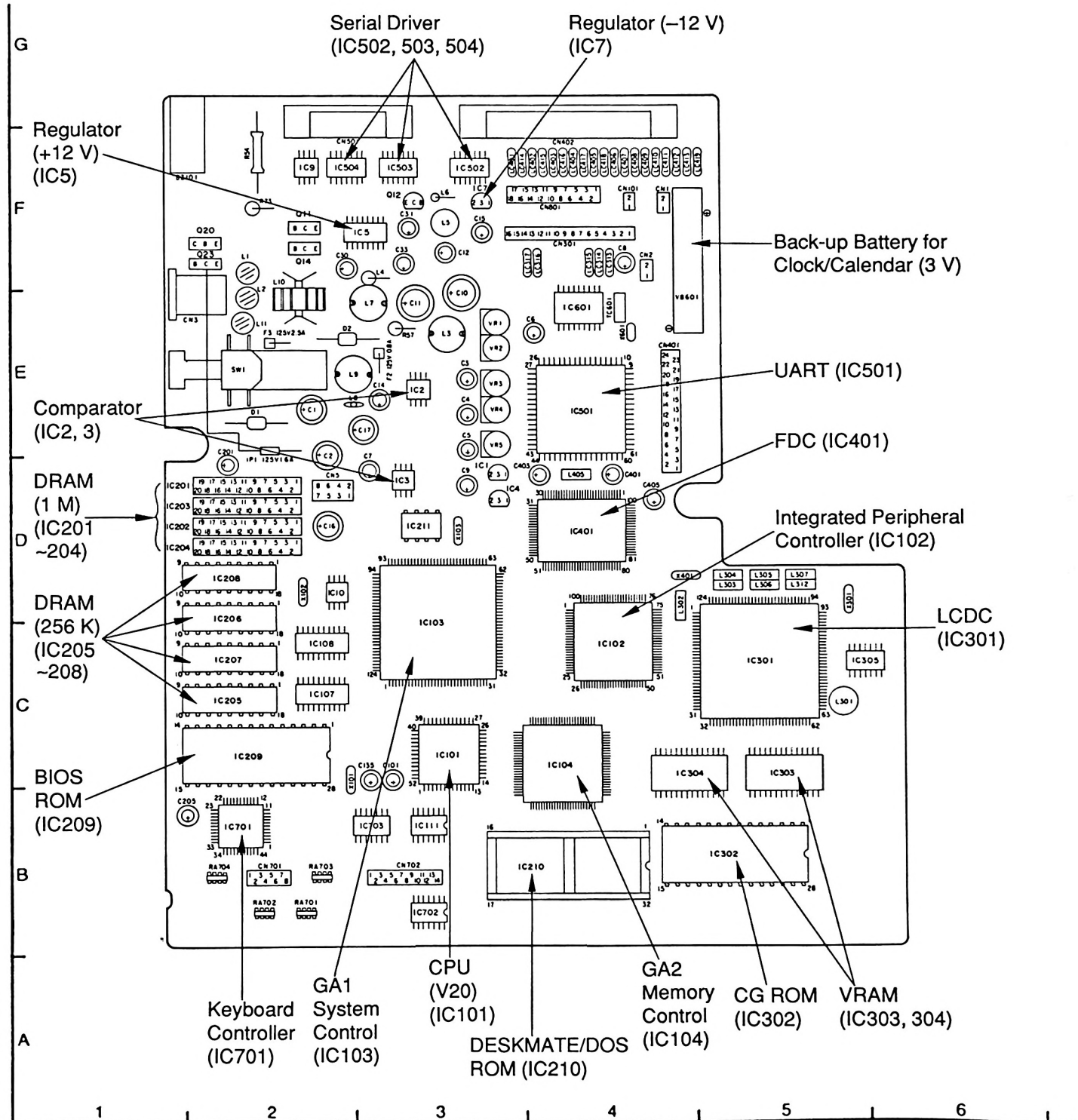


Figure 1-3 Main PCB

Hardware Specifications

- CPU
NEC V20 (μ PD70108-8)
- CPU Clock
8 MHz (0 Wait)
- RAM
Capacity Device
640 K bytes
00000H–7FFFFH 1 M bit type DRAM (256 K bit by 4)
80000H–9FFFFH 256 K bit type DRAM (64 K bit by 4)
All memory data will be lost when the main power is turned off.
- ROM
512 K for DESKMATE/DOS V3.30
32 K for BIOS
8 K for character font
- DISPLAY
Control Device
Graphic Resolution
Character Display
Display Device
Display Control
Video RAM
Character Generator
Base System Display Device
Effective Display Area
MN5502 LCD Controller
640x200 dots
80 charactersx25 lines (or 40 charactersx25 lines)
Reflective type dot matrix LCD
Basically conforms to IBM-CGA
16 K byte (64 K bit type SRAMx2)
Character ROM is used for the character display mode.
Consists of dot matrix LCD panel (640x200 dots)
The time sharing gradation system enables 4 gradation displays.
7.56x4.64 inches (191.97x117.97 mm)
Dot size—0.27x0.56 mm
Dot pitch—0.30x0.59 mm
Aspect—1:1.6
- KEYBOARD
Number of Keys
84 Keys (8x12 Key matrix)
- FDD
Floppy Disk Drive
Number of Tracks
Dimensions
Weight
Operating Voltage
Power Consumption
Rotating Speed
Encoding Method
Capacity
Floppy Disk Controller
Standby Control
Data Transmission
Transfer Rate
EME-213AMC (Matsushita)
Double-sided 3.5-inch FDD
80
4x5.75x1 inches (101.6x146x25.4 mm)
0.7 lb. (315 g)
4.5~5.5 Vdc
Read (Write): 1.5 W Typical
Standby: 50 mW Typical
Seek: 3.1 W Typical
300 rpm
MFM
Unformatted: 1000 K-byte
Formatted per disk: 737 K-byte (9-sector/track)
SPC 2050F CMOS type of 765
Standby control is controlled by software
DMA transmit
250 K bits/sec

●RS-232C INTERFACE

Standard Conform to EIA Standard
 Device VL16C452
 DS14C88 and DS14C89AN
 Word Length 5, 6, 7 or 8 bits
 Parity Even, Odd or None
 Stop Bit Length 1, 1.5 or 2 bits
 Baud Rate 50, 75, 110, 150, 300, 600, 1200, 2400, 4800 and 9600 bps
 Output Signal Level Output Signal based on +12 V and -12 V
 Input Signal Voltage SPACE: +3 V ~ +15 V
 MARK: -3 V ~ -15 V

●PRINTER INTERFACE

Device VL16C452
 Control The printer is controlled by the STROBE and BUSY signals. When the printer is not busy, the CPU receives an interrupt signal, IRQ7.
 Output Normal commercial printers can be used, if they have input.

●RTC (REAL TIME CLOCK)

Device RICOH RF5C15
 Crystal Oscillation 32.768 kHz
 Battery Backup Time counting is maintained by the backup battery even when the system power is turned off.
 Accuracy ±30 sec./month

●POWER SOURCE

Main Battery 6 V, 1800 mAh, Sealed Lead-acid battery
 Back up Battery Lithium battery of 3 V, 1000 mAh to hold the time data of RTC.
 Battery voltage warning The first warning is a one-second flashing of the Low Battery LED. The user is instructed to charge the battery voltage to 5.9 V~6.0 V. After the first warning, the system can be used for about 30 minutes with FDD 10% duty. The second warning is a 250 msec flashing of the Low Battery LED. The user is instructed to shut down the system at a battery voltage of 5.1 V~5.6 V. User should close current task file. About 5 minutes after the second warning, the system shuts down and loses all RAM data.

●POWER SAVE MODE

When nothing is input for pre-set time (software selectable), the system automatically turns to STANDBY MODE. Pressing any key brings the computer out of STANDBY MODE. The program being used when STANDBY MODE is engaged is maintained intact.

Note 1: The time of auto STANDBY MODE can be set from 0 to 255 minutes with the "POWER11.COM" program.

Note 2: In STANDBY MODE, memory contents will be maintained by main battery for 5 hours, at the condition of full charge. When main battery is discharged, memory contents will be lost. The Low Battery warning is displayed in STANDBY MODE as well.

Note 3: Input power rating (AC adapter) Voltage 8.55~10.45 V

Note 4: Current consumption (Typical Data)

Mode	AC Operation	Battery Operation
NORMAL USE MODE	250 mA	330 mA
FDD SEEK	600 mA	830 mA
FDD MOTOR ON	730 mA	1000 mA
STANDBY MODE	210 mA	285 mA

PART II. DISASSEMBLY INSTRUCTIONS

Note: Before disassembling, be sure to perform the following procedures first:

1. Turn the power switch off.
2. Disconnect the AC adapter.
3. Remove the battery cover and disconnect the battery.
4. Remove the floppy diskette.

Caution: Please follow directions carefully.
Do not interchange screws in any part of the system.

Top Case

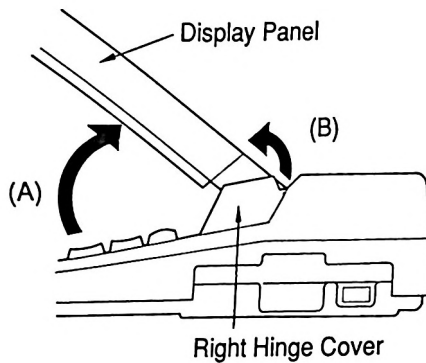


Figure 1

- (1) Open the display panel and adjust its angle in the direction of arrow (A) as shown in Figure 1. Then, gently lift up the rear end of the right hinge cover in the direction of arrow (B).

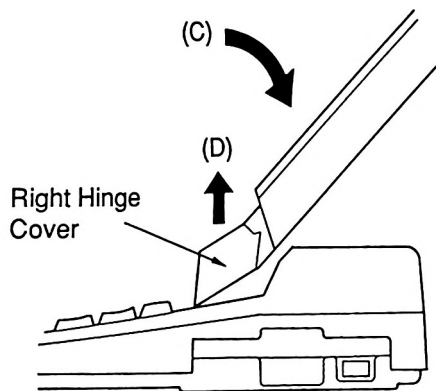


Figure 2

- (2) Set the angle of the display panel in the direction of arrow (C) as shown in Figure 2. Then, lift up the right hinge cover in the direction of arrow (D).
- (3) Repeat the same procedures mentioned above to remove the left hinge cover.
- (4) Close display panel.

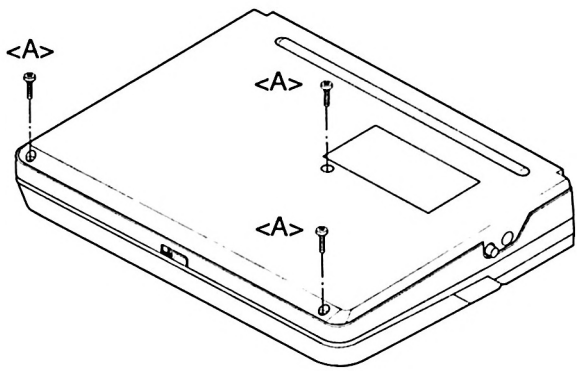


Figure 3

(5) Turn over the computer and remove three screws <A> ($3\text{Ø}\times 10$) on the bottom panel as shown in Figure 3.

(6) Place the back of unit to your side.

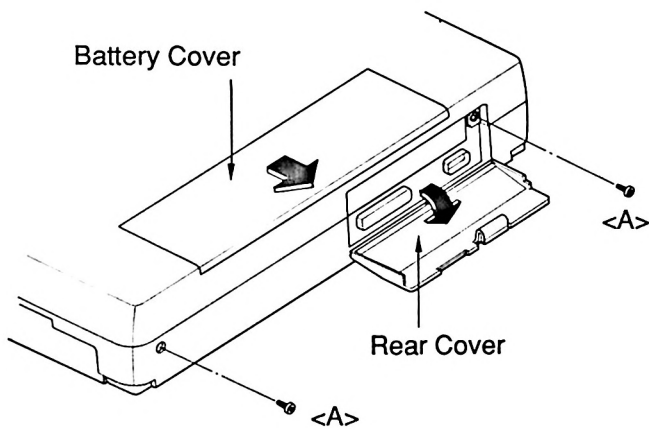


Figure 4

(7) Open the rear cover and remove two screws <A> ($3\text{Ø}\times 8$) as shown in Figure 4.

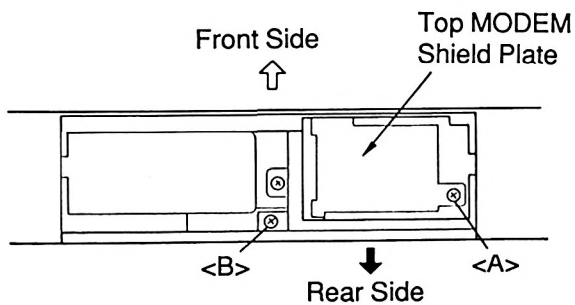


Figure 5

(8) Open the battery cover and remove one screw <A> ($3\text{Ø}\times 6$) fixing the top MODEM shield plate and one screw ($3\text{Ø}\times 10$) as shown in Figure 5.

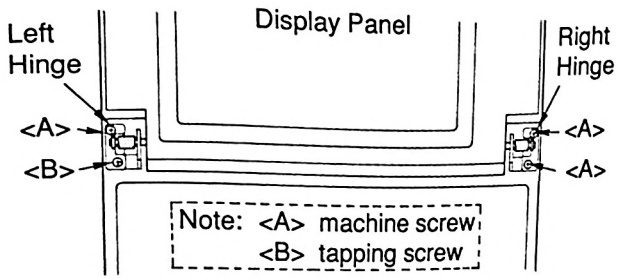


Figure 6

- (9) Remove three screws <A> (machine screw, 3Ø×8) on the right and left hinges, and remove one screw (tapping screw, 3Ø×10) on the left hinge as shown in Figure 6.

***Note:** When reassembling, please make sure the tapping screw is in the correct location.

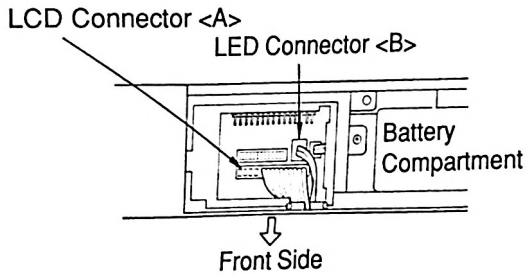


Figure 7

- (10) Disconnect the LCD connector <A> and the LED connector as shown in Figure 7.

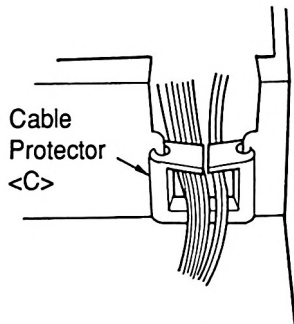


Figure 8

- (11) Remove the cable protector <C> from the top shield plate while lifting up the rear end of the top case slightly as shown in Figure 8.

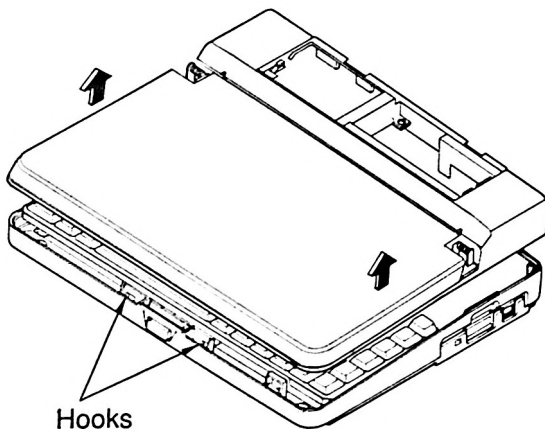


Figure 9

- (12) Gently lift up the top case as shown in Figure 9.

Note: There are two retaining hooks that must be carefully unlatched.

Keyboard

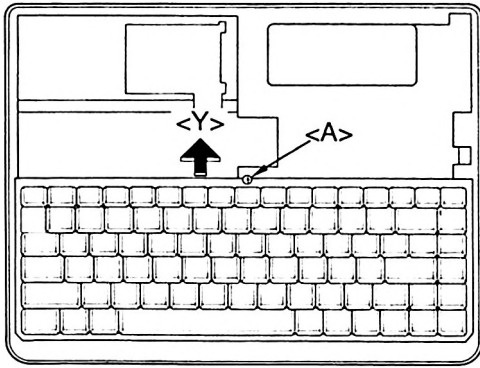
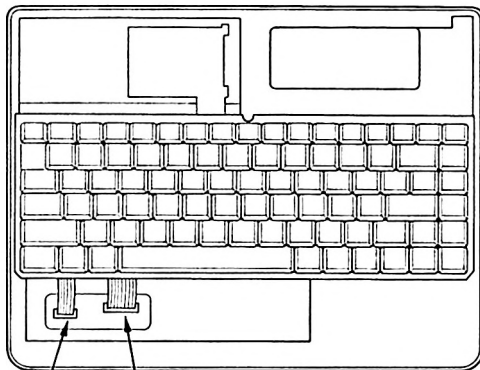


Figure 10

- (1) After removing the top case, remove one screw <A> (3Ø×8) from the keyboard as shown in Figure 10.
- (2) While lifting up the rear end of keyboard slightly, slide it in the direction of <Y> as shown in Figure 10.

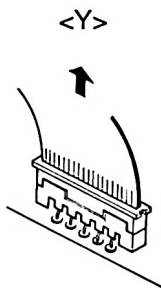


Keyboard Flat Cables

Figure 11

- (3) Remove the keyboard flat cables <A> and from their connectors as shown in Figure 11.

Note: These flat cables can be removed by sliding their connectors in the direction of <Y> as shown in Figure 12.



Keyboard Connector

Figure 12

Main PCB

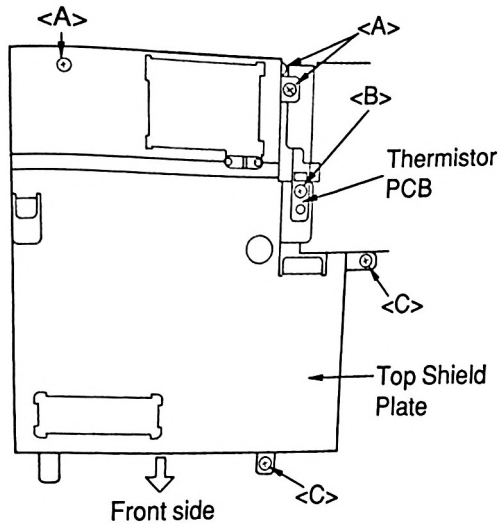


Figure 13

(1) After removing the keyboard, remove three screws <A> (machine screw, 3Ø×6) on the top shield plate, one screw (machine screw, 3Ø×6) on the thermistor PCB and two screws <C> (tapping screw, 3Ø×8) on the top shield plate as shown in Figure 13.

(2) Lift up the top shield plate.

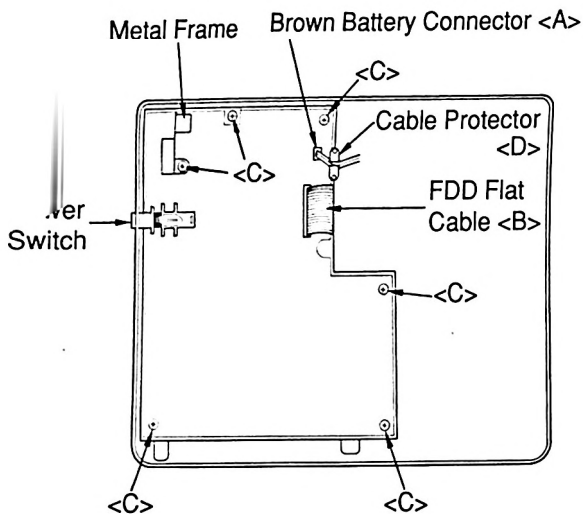


Figure 14

(3) Detach the brown battery connector <A> as shown in Figure 14.

(4) Detach the FDD flat cable by gently pulling it up as shown in Figure 14.

(5) Remove six screws <C> (3Ø×8) fixing the main PCB as shown in Figure 14.

(6) Remove the cable protector <D> from the bottom shield plate and take out the brown battery connector from the cable protector as shown in Figure 14.

(7) Gently push the power switch inward as shown in Figure 14.

(8) Lift up the main PCB from the right end by holding the metal frame fixing serial & parallel connectors.

(9) Detach the power switch knob <A> and remove the metal frame from the main PCB by loosening 4 screws <C> as shown in Figure 15.

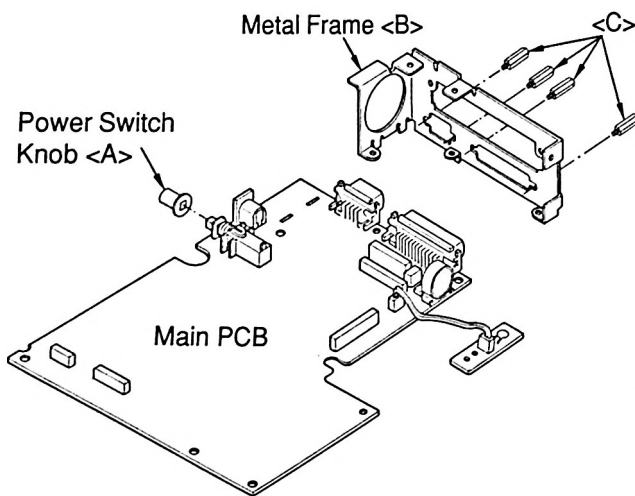


Figure 15

Floppy Disk Drive

Note: Before disassembling the FDD, remove the main PCB as mentioned on the page 2-5.

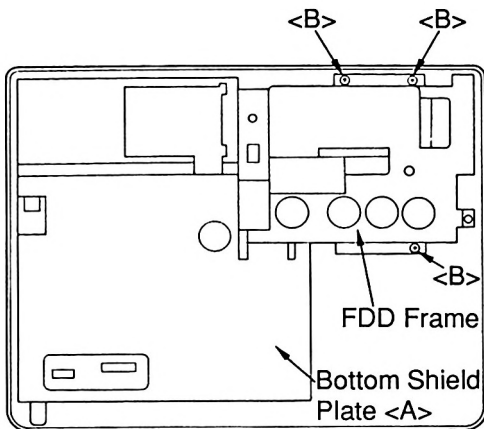


Figure 16

- (1) After removing the main PCB, gently lift up the bottom shield plate <A> from the bottom case as shown in Figure 16.
- (2) Remove three screws ($3\varnothing\times 8$) fixing the FDD frame as shown in Figure 16.

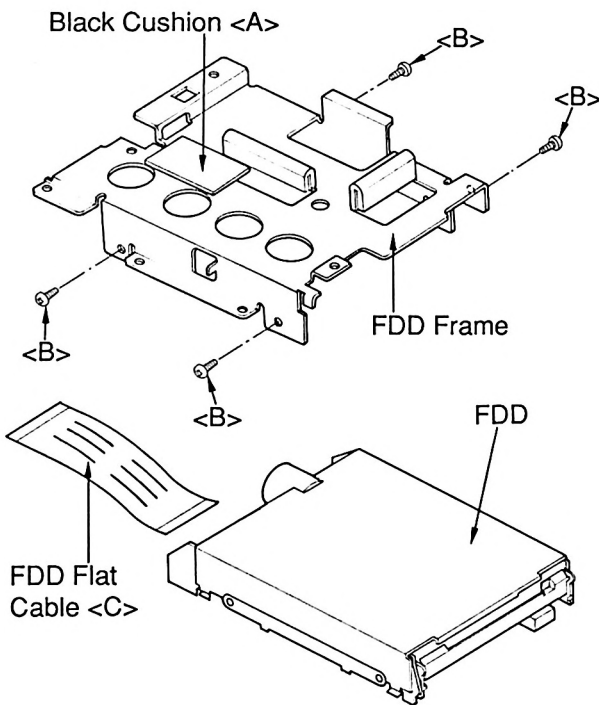


Figure 17

- (3) Gently peel off the black cushion <A> from the FDD frame as shown in Figure 17 and save it for the next use.
- (4) Remove four screws ($3\varnothing\times 6$) from the FDD frame as shown in Figure 17.
- (5) Detach the FDD flat cable <C> from the FDD.

Note: When connecting the FDD flat cable to the FDD, be sure the surface marked with the name of the cable manufacture is facing upward as shown in Figure 17.

LCD Unit

Note: Before disassembling the LCD Unit, remove the top case as mentioned on the page 2-1.

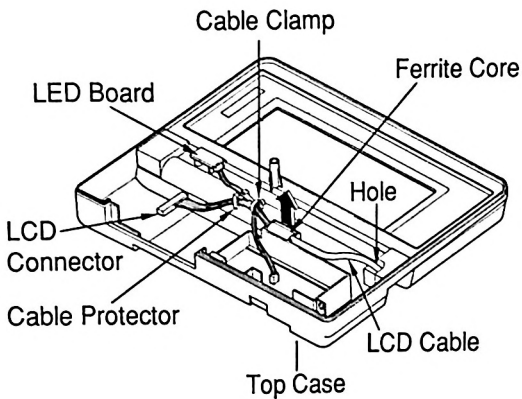


Figure 18

- (1) Turn over the display panel and the top case, and remove the cable clamp by cutting with a diagonal cutter as shown in Figure 18.
- (2) Take out the LED (CHARGE/LOW BATTERY) cable from the cable protector and remove the ferrite core from its compartment by gently pulling up the LCD cable as shown in Figure 18.
- (3) Remove the LCD cable from the hole opening next to the right hinge of the top case.

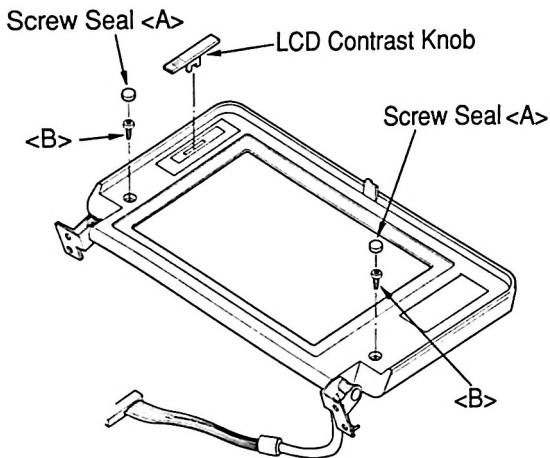


Figure 19

- (4) Gently lift up the LCD contrast knob by holding both ends as shown in Figure 19.
- (5) Gently remove two screw seals <A> on both sides by using a sort of ice pick and remove two screws (3Øx8) as shown in Figure 19.

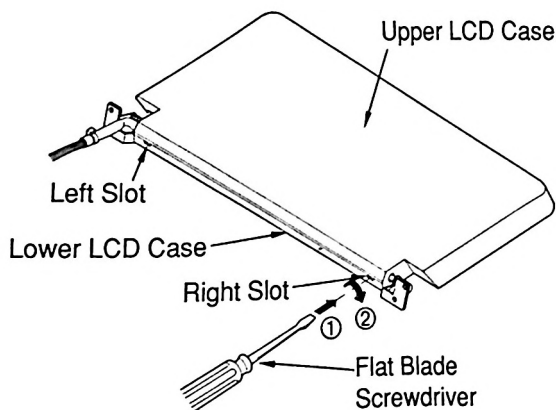


Figure 20

- (6) Turn over the LCD panel and insert the flat blade screwdriver in the slot of the lower LCD case as shown in Figure 20. Then, gently twist the screwdriver to separate the upper LCD case from the lower case.
- (7) Repeat the same procedure mentioned above for the left slot of the lower LCD case.

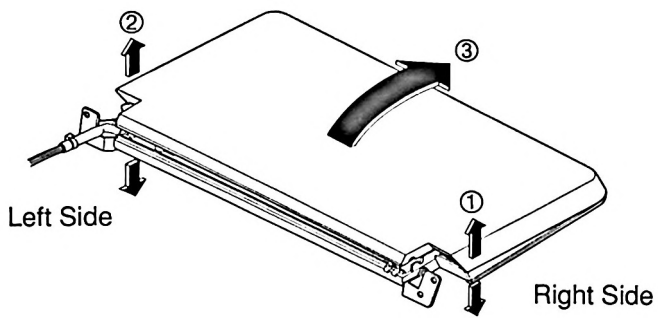


Figure 21

- (8) Gently lift up the right side of the upper LCD case a small amount and then lift up the left side. Remove the upper LCD case by gently lifting up the center of it as shown in Figure 21.

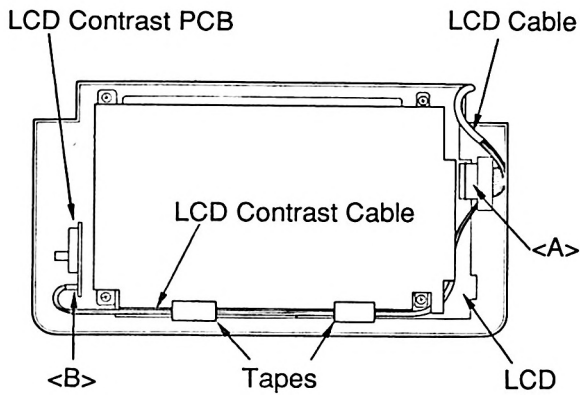


Figure 22

- (9) Place the LCD panel as shown in Figure 22 and remove the two connectors <A> and .
- (10) After peeling off the two pieces of tape fixing the LCD contrast cable, remove the LCD cable from the display panel as shown in Figure 22.

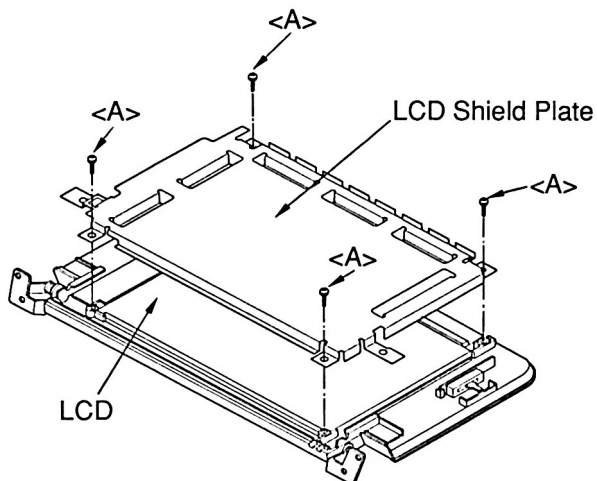


Figure 23

- (11) Remove four screws <A> (2.6 \varnothing ×6) fixing the LCD shield plate as shown in Figure 23. Remove hinges and lift off LCD shield plate.

*Reassemble in the reverse order.

PART III. PREVENTIVE MAINTENANCE

Main Board Adjustment

1) Adjustment items

- (1) Recharge Circuit
- (2) LOW Battery Indication Circuit
- (3) Reset Circuit
- (4) Backup Circuit
- (5) Real Time Clock Frequency

2) Test Equipment

- (1) DC Power Supply
- (2) Electronic Load (more than 200 mA)
- (3) Voltmeter
- (4) Oscilloscope
- (5) Frequency Counter

3) Preparations

- (1) Remove the upper cabinet, keyboard and shield plates.
(Refer to II. Disassembly Instructions.)
- (2) Connect the Test Equipment to the main board according to the individual procedures.

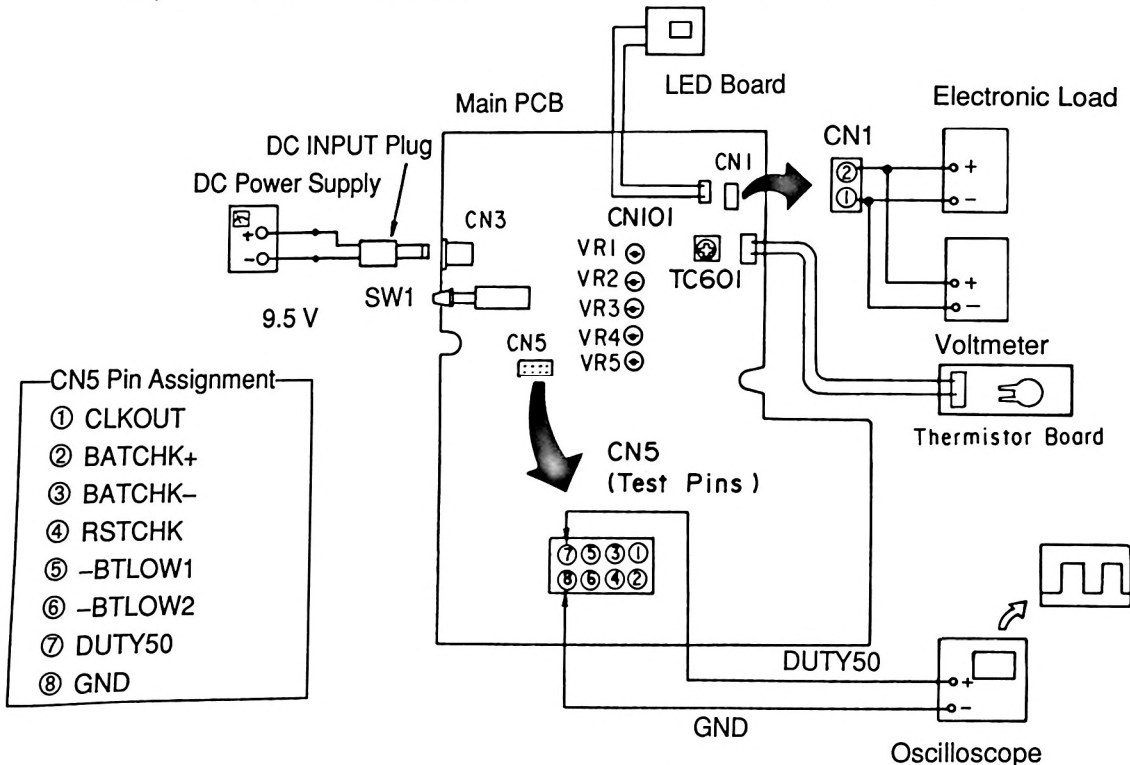
*Warning: The solder side of thermistor board must be insulated from any metal parts connecting to GND. Otherwise the fuse (F2) on the main board may be blown.

4) Adjusting Methods

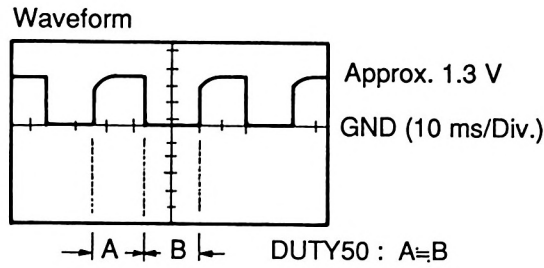
(1) Recharge Circuit Adjustment

Note: Be sure that the Power switch, SW1 is turned OFF.

- 1-1) Connect an Electronic Load and Voltmeter to Pins 1 (-) and 2 (+) of the CN1 as illustrated below.
- 1-2) Connect an oscilloscope to Pins 7 (DUTY50) and 8 (GND) of CN5 as illustrated below.

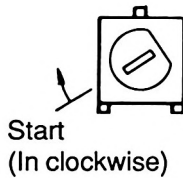


- 1-3) Apply 9.5 V to DC-IN Jack, CN3 with DC Power Supply.
- 1-4) Adjust the Electronic Load so that it can apply 100 mA.
- 1-5) Turn the Power switch, SW1 ON.
- 1-6) Adjust VR1 so that the waveform on the oscilloscope is shown as illustrated below.



Caution: a) When adjusting the potentiometers (VR1~VR5), set them between start and end position.

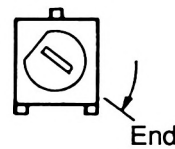
Start-position



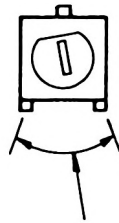
Center-position



End-position



b) DO NOT set the potentiometers (VR1~VR5) in the ineffective range as illustrated below.



DO NOT set in the ineffective range.

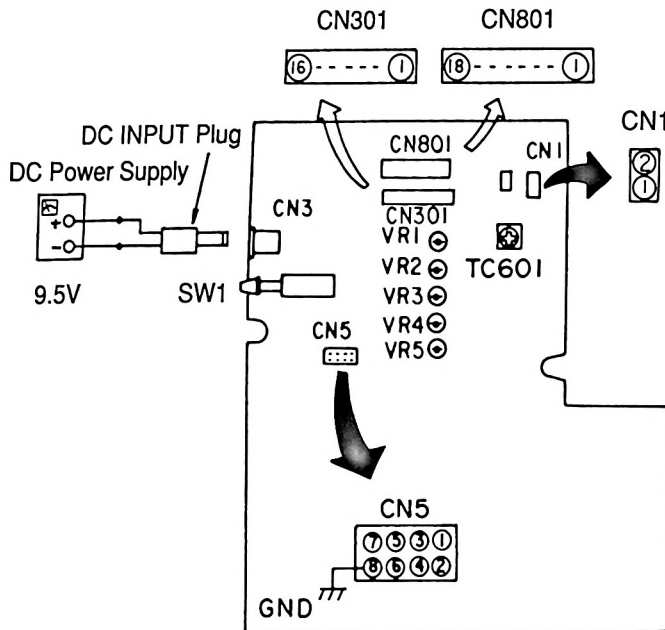
- 1-7) Adjust the Electronic Load so that it can apply 20 mA.
- 1-8) In accordance with environment temperature, adjust VR2 so that the voltage of Voltmeter shows in the tolerance range below.

Environment Temp.	(°C)	17.5~22.5	22.5~27.5	27.5~32.5	32.5~37.5
	(°F)	63.5~72.5	72.5~81.5	81.5~90.5	90.5~99.5
Tolerance of Voltage to be adjusted (V)		6.82~6.88	6.77~6.83	6.70~6.76	6.65~6.71

- 1-9) Adjust the Electronic Load so that it can apply 200 mA.
Then make sure the measured voltage with the voltmeter is in the "Voltage range of Confirmation" below according to the environment temperature.
If it is out of the "Voltage range of Confirmation", repeat the adjustments from the beginning.

Environment Temp.	(°C)	17.5~22.5	22.5~27.5	27.5~32.5	32.5~37.5
	(°F)	63.5~72.5	72.5~81.5	81.5~90.5	90.5~99.5
Voltage range of Confirmation (V)		7.18~7.48	7.15~7.45	7.08~7.38	7.00~7.30

- 1-10) Confirm that the LED on LED Board lights up.
1-11) Remove the voltmeter from the Electronic Load and connect it to Pin 8 (GND) of CN5 and appropriate pin in accordance to the table shown below.
Then confirm that the measured voltage at pins are in the "Tolerance of Measured Voltage (V)".
If it is out of the "Tolerance of measured Voltage (V)", repeat the adjustments from the beginning.



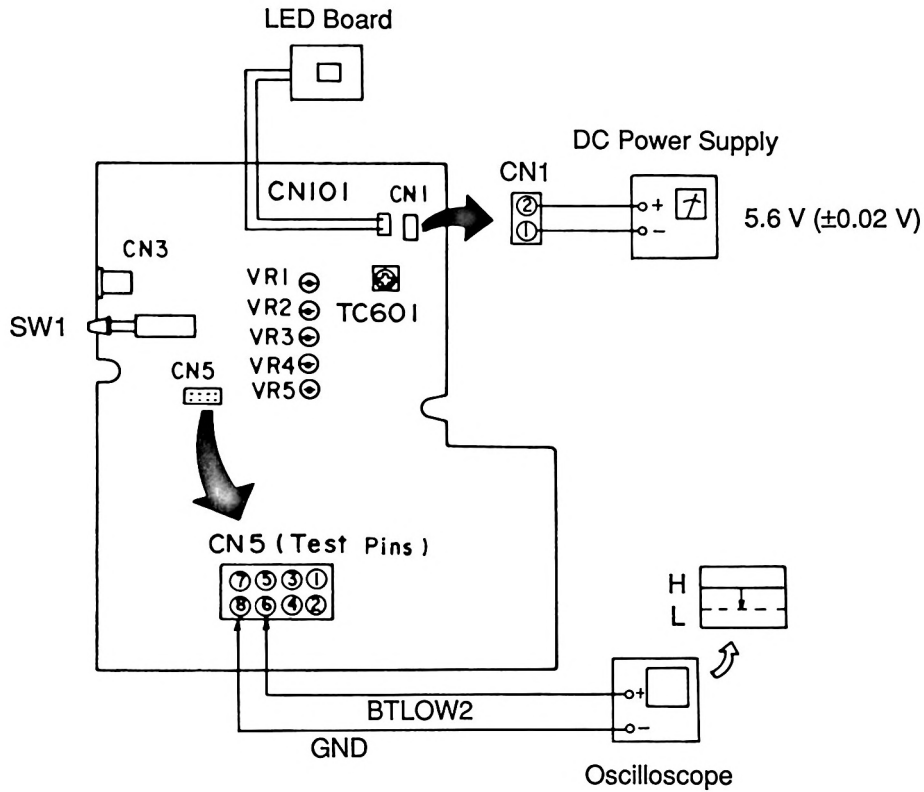
Pin No./Connector No.	Description	Tolerance of Measured Voltage (V)
Pin 5/CN301	VDD	4.75~5.25
Pin 7/CN301	Vlcd	-25.2~22.8
Pin 15/CN801	+12 V	11.4~12.6
Pin 17/CN801	-12 V	-12.6~11.4

- 1-12) Turn the Power switch, SW1 OFF.
1-13) Remove the DC Power Supply from the DC-IN Jack, CN3.

(2) LOW BATTERY Indication Circuit

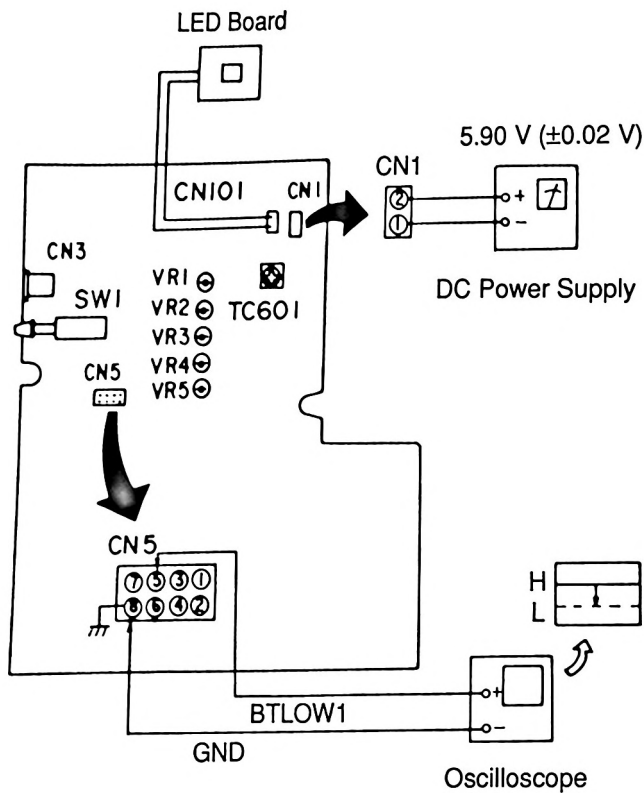
Note: Be sure that the Power switch, SW1 is turned OFF.

- 2-1) Connect the DC Power Supply to Pins 1 (-) and 2 (+) of CN1 and apply 5.60 V (± 0.02 V) as shown below.
- 2-2) Connect the oscilloscope to Pins 6 (BTLOW2) and 8 (GND) of CN5 as illustrated below.



- 2-3) Turn the Power switch, SW1 ON.
- 2-4) Adjust VR3 so that the voltage at Pin 6 of CN5 changes from "High" to "Low" level ($H \rightarrow L$) by observing the oscilloscope.

2-5) Connect the oscilloscope to Pins 5 (BTLOW1) and 8 (GND) as illustrated below.



2-6) Apply 5.90 V (±0.02 V) to CN1 with DC Power Supply.

2-7) Adjust VR4 so that the voltage at Pin 5 of CN5 changes from "High" to "Low" level (H \rightarrow L) by observing the oscilloscope.
Then confirm the LED on LED board blinks slowly. (approx. 1 sec blinking)

Note: Perform the following steps to confirm the adjustment done. If there is incorrect adjustment, repeat from the step 2-1).

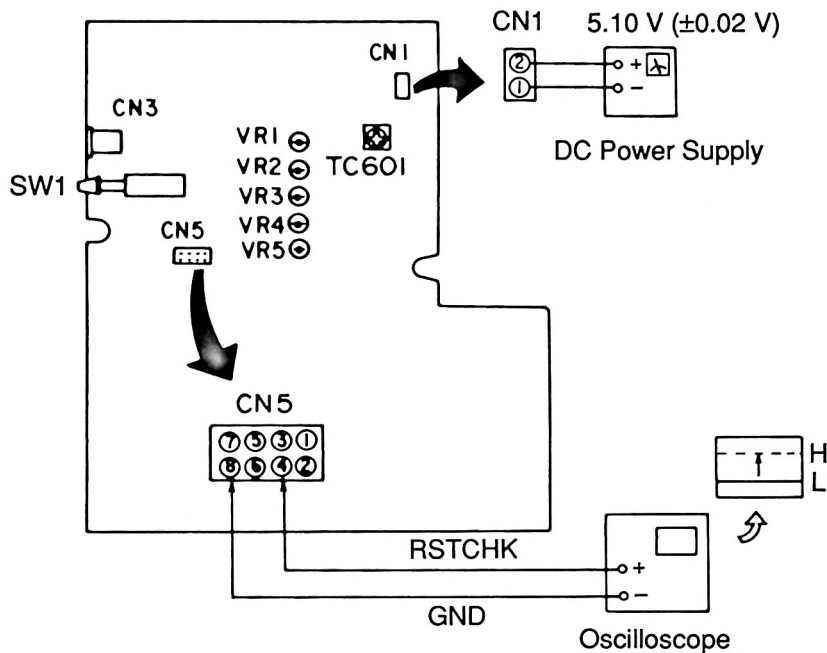
2-8) Set the supplied voltage to 5.60 V (±0.02 V) and then be sure the LED blinks rapidly. (approx. 250 msec blinking)

2-9) Set the supplied voltage to 5.90 V (±0.02 V) and then be sure the LED blinks slowly.

(3) Reset Circuit

Note: Be sure that the Power switch, SW1 is turned OFF.

3-1) Connect the oscilloscope to Pins 4 (RSTCHK) and 8 (GND) of CN5 as illustrated below.



3-2) Turn the Power switch, SW1 ON.

3-3) Apply 5.10 V (±0.02 V) to CN1 with DC Power Supply.

3-4) Please wait for approx. 5 sec. after a beep sound goes off. Then adjust VR5 so that the voltage at Pin 4 of CN5 changes from "Low" to "High" level (L→H), (approx. 3 V) by observing the oscilloscope.

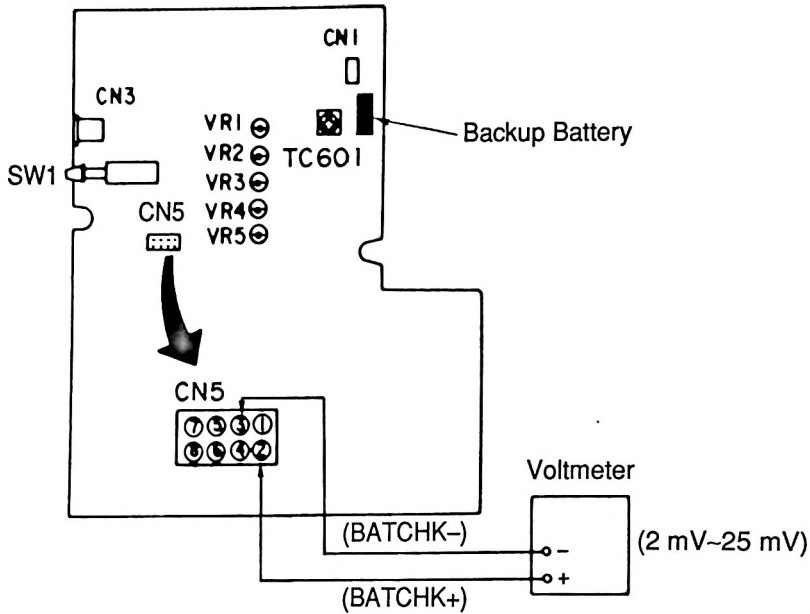
3-5) Set the supplied voltage to 6.10 V~6.40 V. Then confirm the voltage at Pin 4 of CN5 is "Low" level.

3-6) Set the supplied voltage to 5.05 V~5.15 V and then confirm the voltage at Pin 4 of CN5 is "High" level (approx. 3 V).

Note: If "Low" level at the Pin 4 of CN5 is found at the step 3-6) above, please repeat the adjustment from the step 3-3).

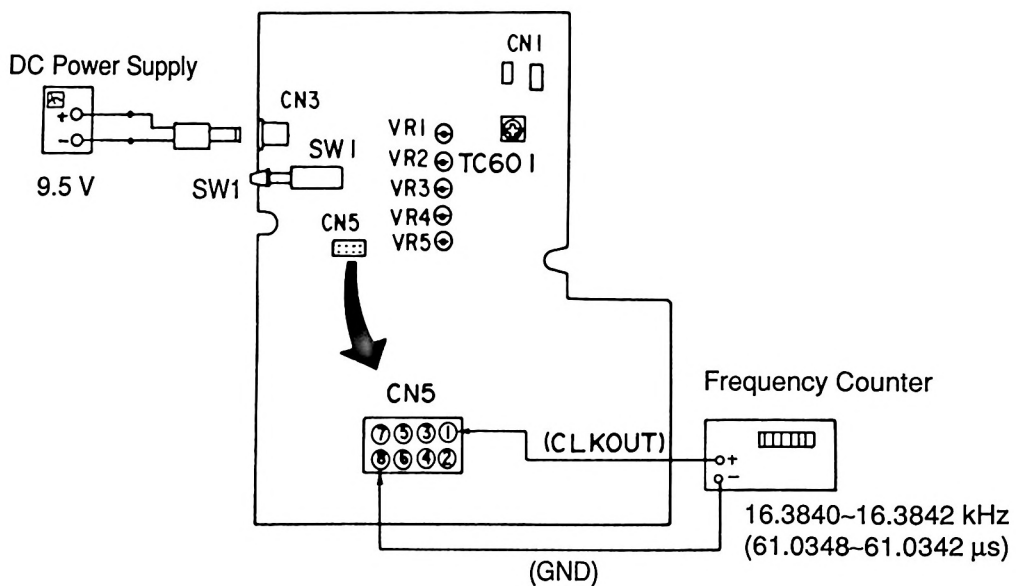
(4) Backup Battery Voltage Check

- 4-1) Remove the DC Power Supply from CN1.
- 4-2) Turn the Power switch, SW1 OFF.
- 4-3) Confirm the voltage of the Backup Battery is between 2.0 V and 3.0 V by connecting Voltmeter to Pins 3 (+) and 8 (-) of CN5.
- 4-4) Connect the Voltmeter to Pins 2 (BATCHK+) and 3 (BATCHK-) and then confirm the voltage is between 2 mV and 25 mV.



(5) TC601 (Real Time Clock) Adjustment

- 5-1) Apply 9.5 V to the connector, CN3 with DC Power Supply.
 - 5-2) Connect a Frequency Counter to Pins 1 (CLKOUT) and 8 (GND) of connector, CN5.
 - 5-3) Adjust the TC601 so that reading out frequency will be 16.3840~16.3842 kHz.
- Note: Refer to P. 5-13 about adding a pull up resistor.



PART IV. THEORY OF OPERATION

General

This section describes the theory of operation for the Tandy 1100FD.

Figure 4-1 shows how this section is organized and highlights significant areas.

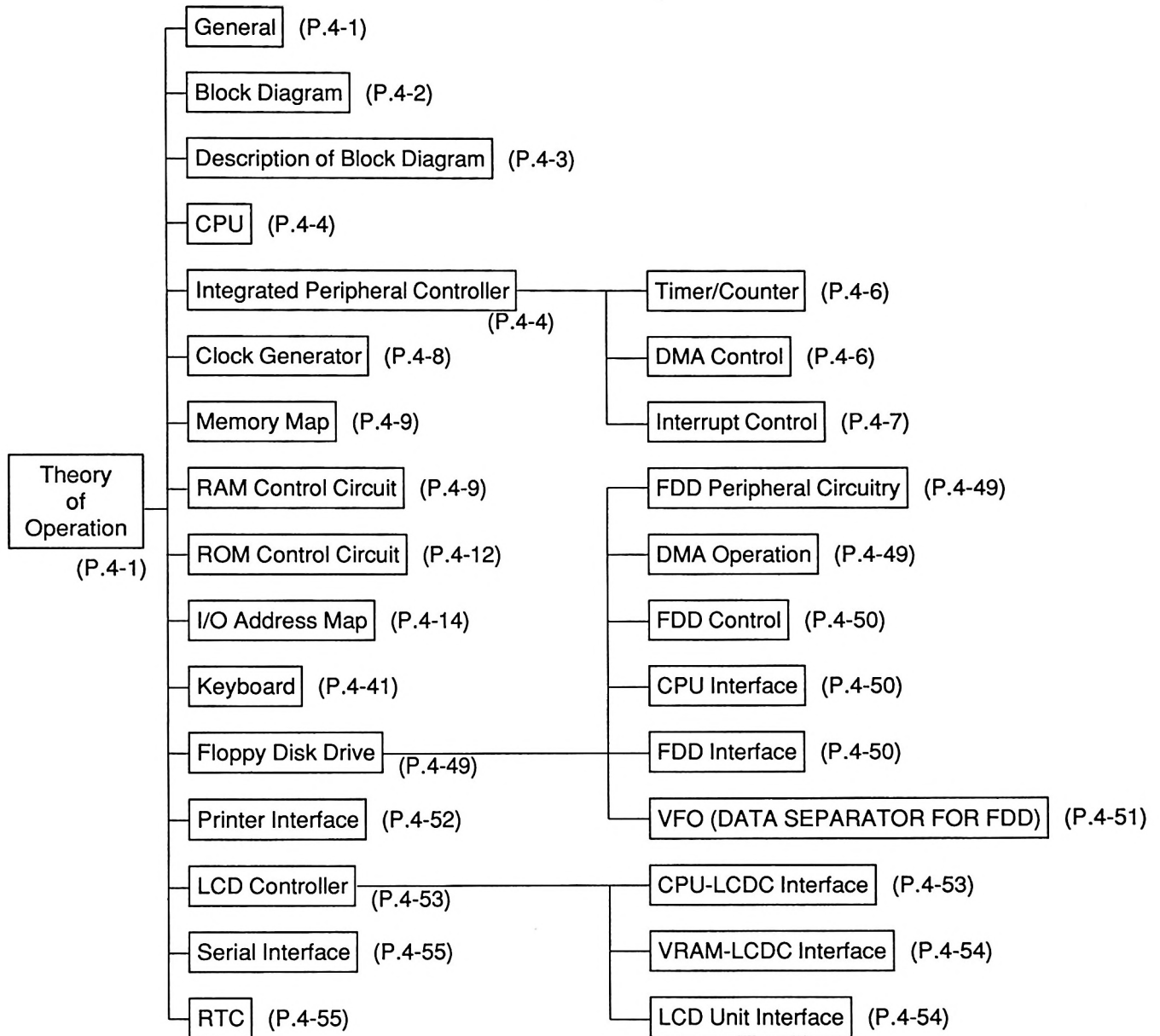


Figure 4-1 Organization of Part IV

Description of Block Diagram

The block diagram of the previous page shows the basic function divisions. The following are brief descriptions of the functions of each block.

CPU	NEC V20, (IC101)
Clock Generator	Custom IC (Gate Array), MN53030RFP (IC103)
DMA Control	Equivalent to 8237A 4-channel DMA controller (in MN12862), (IC102)
Interrupt Controller	Equivalent to 8259A 8-channel interrupt controller (in MN12862), (IC102)
Bus Control	Equivalent to 8288 bus controller (in MN53030RFP), (IC103)
Timer/Counter	Equivalent to 8254 3-channel timer/counter (in MN12862), (IC102)
Keyboard/Sense/Control Port	Subset of 8255 (in MN53030RFP), (IC103)
Keyboard CPU	49HG528 Microprocessor to scan keys and transmit codes to system (IC701)
Real Time Clock	RICOH RF5C15, (IC601)
Display Control	MN5502, (IC301)
UART/PARALLEL	VL16C452 RS-232C/Printer interface, (IC501)
FDC	EPSON SPC2050 CMOS type of 765 Floppy Disk Controller, (IC401)

CPU

The CPU (V20) is a CMOS 16-bit microprocessor provided with an 8/16-bit architecture and an 8-bit data bus. It has a powerful instruction set.

1. Packed BCD operation instruction
2. High-speed multiplication/division instruction
3. Internal memory high-speed block transfer
4. Bit operation instruction
5. High-speed calculation of effective addresses

The V20 is equipped with a 20-bit address bus that can access 1M byte memory. In addition, the V20 has emulation functions of 8080 and comes with a standby mode that significantly reduces power consumption. The V20 can be used in two scale systems: the minimum mode, which is suitable for a small system, and the maximum mode which is suitable for a large system.

The microprocessor is configured in the Tandy 1100FD in the maximum mode. The V20 operates with several different wait modes in the Tandy 1100FD.

Table 4-1 shows Wait states.

Figure 4-4 shows CPU.

Access mode	Number of Wait states
Memory Access (Main RAM) Address=00000H-9FFFFH	0
Memory Access (Video RAM) Address=A0000H-BFFFFH	2+ α
Memory Access Address=C0000H-EFFFFH	1
Memory Access (BIOS ROM) Address=F0000H-FFFFFH	0
I/O Access	2
INTA Access	1

Table 4-1 Wait States

Integrated Peripheral Controller

The MN12862 (IC102) is an Integrated Peripheral Controller has an Advanced Programmable Timer/Counter, a Direct Memory Access (DMA) Controller and a Programmable Interrupt Controller.

Figure 4-5 shows the block diagram of MN12862.

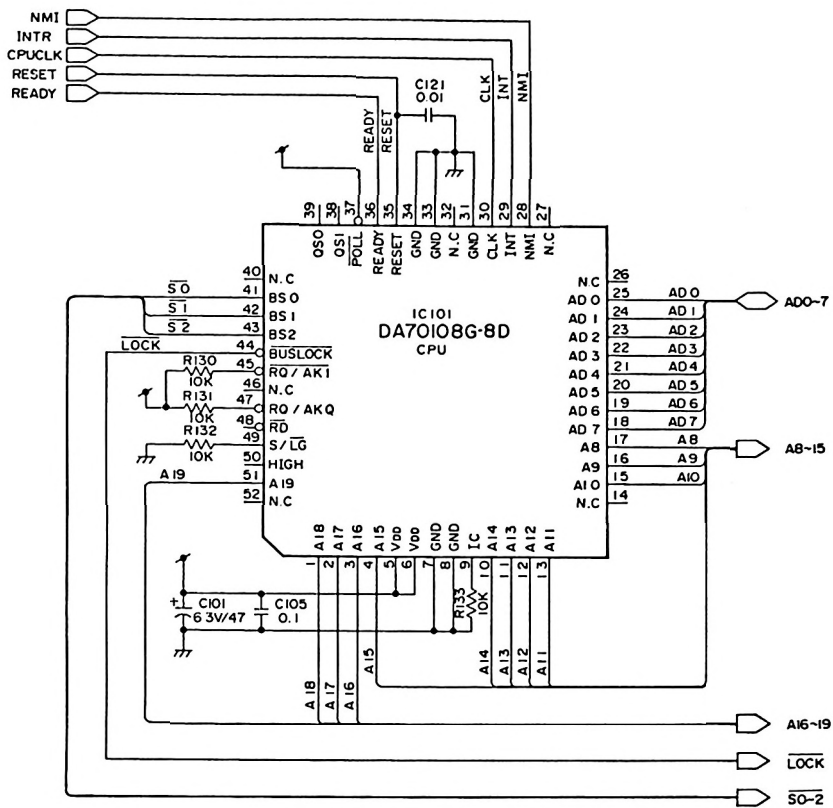


Figure 4-4 CPU (IC101)

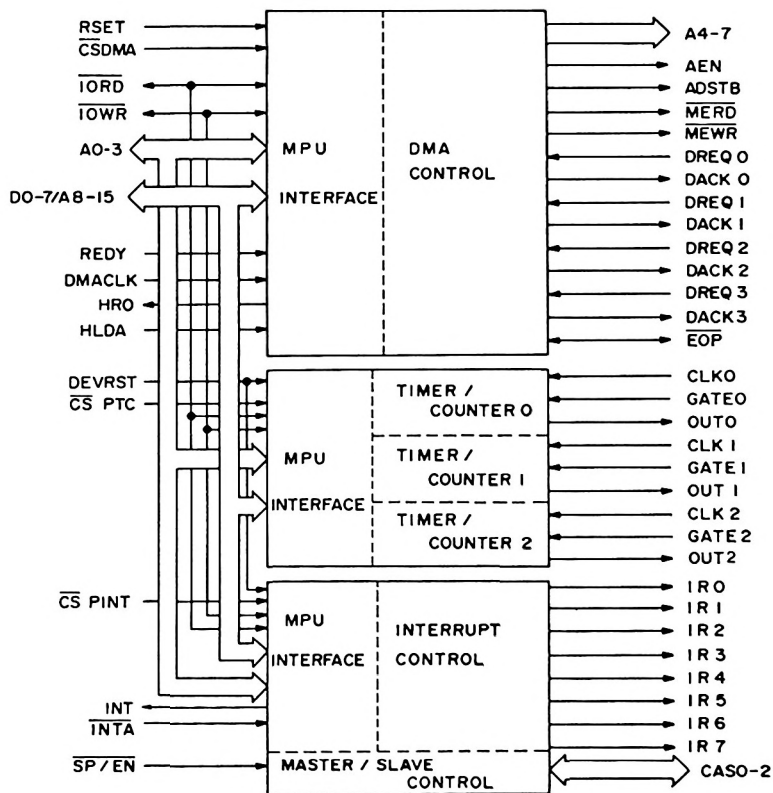


Figure 4-5 MN12862 (IC102) Block Diagram

Timer/Counter

The Advanced Programmable Time/Counter, MN12862, (IC102) is compatible with 8254. Three independent 16-bit Timer/Counters are used in the system.

- Channel 0: General-purpose timer, providing a constant time base for implementing a time-of-day clock.
- Channel 1: Time and request cycles from the DMA Channel 0.
- Channel 2: Tone generation for the beeper.

Figure 4-6 shows Timer/Counter control logic.

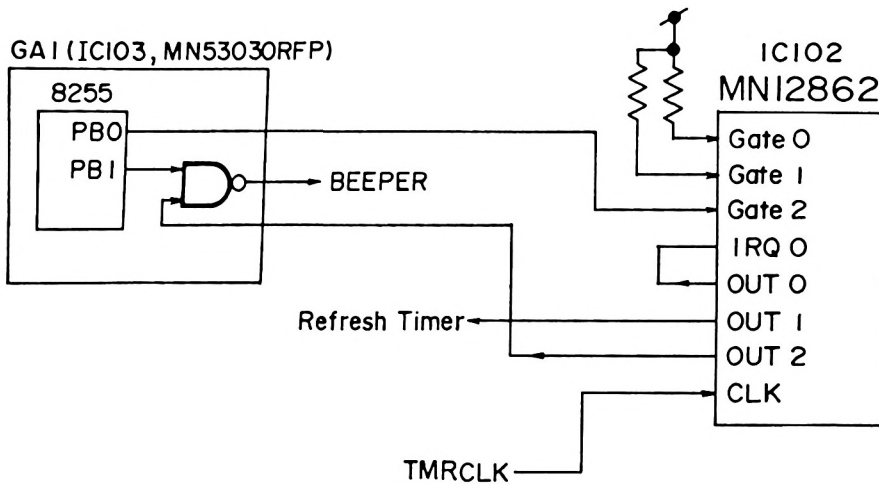


Figure 4-6 Timer/Counter Control Logic

DMA Control

The DMA Controller, MN12862, (IC102) is compatible with 8237A. Three of the four DMA channels are used in this system.

- Channel 0: Refresh the system dynamic memory. This is done by programming a channel of the timer-counter device to periodically request a dummy DMA transfer.
- Channel 1: Available on the I/O bus.
- Channel 2: Supports data transmission between the FDC and the CPU.

Interrupt Control

The V20 has abundant interrupt processing functions:

External interrupt: NMI (Non-maskable Interrupt)
INT (Maskable Interrupt)

Interrupt by software

The Interrupt Controller, MN12862, (IC102) is compatible with 8259A. It can process eight interrupt request inputs, allocating a priority level to each one.

Interrupt Controller Channel Assignment:

- IRQ 0—Timer interrupt for relative timer
- 1—Keyboard interrupt
- 2—Real Time Clock Alarm interrupt
- 3—COM2 interrupt
- 4—COM1 interrupt
- 5—Open for other use
- 6—Floppy Disk Controller interrupt
- 7—Printer interface interrupt

There are two NMI-Interrupt sources in the Tandy 1100FD.

1. Low Battery 1
2. Low Battery 2

The Low battery 1 and Low battery 2 are signals for battery voltage warning. The Low battery 1 signal becomes active at a battery voltage of 5.6 V~5.9 V. After the Low battery 1 signal becomes active, the system can be used for about 20 minutes with the FDD at 10% duty. Then the Low battery 2 signal becomes active at a battery voltage below 5.6 V. (The Low battery 1 and Low battery 2 signals are maskable by the I/O port 61H. Refer to I/O address map.)

The NMI interrupt is not maskable by the CPU, but it can be enabled or disabled by the hardware. The enable-state is activated by port 0A0H bit 7.

The enable-state is cleared by RESET.

Figure 4-7 shows NMI Logic.

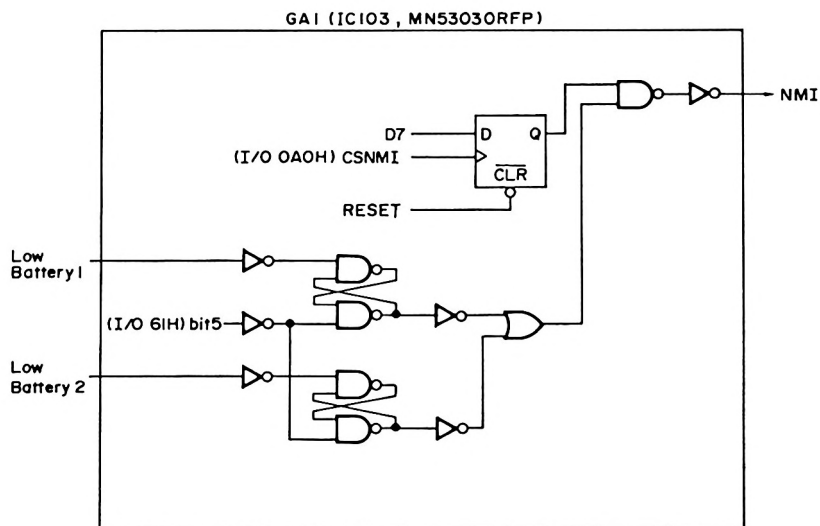


Figure 4-7 NMI Logic in GA1 (IC103)

Clock Generator (GA1)

This Clock Generator block of GA1, MN53030, (IC103) is a clock pulse generator/driver for microprocessors and their peripherals. This block receives a 16 MHz input clock and divides it by 2 to produce CPU CLK, and also divides it by 2 to produce DMACLK. Also this block receives a 14.318 MHz input clock and divides it by 2 to produce Keyboard Controller KBCCLK, and also divides it by 12 to produce Timer/Counter TMRCLK. Table 4-2 shows individual Clock speed.

MODE	FREQUENCY (Clock Speed)
CLK	8 MHz
DMACLK	4 MHz
KBCCLK	7.16 MHz
TMRCLK	1.19 MHz

Table 4-2 Clock Speed

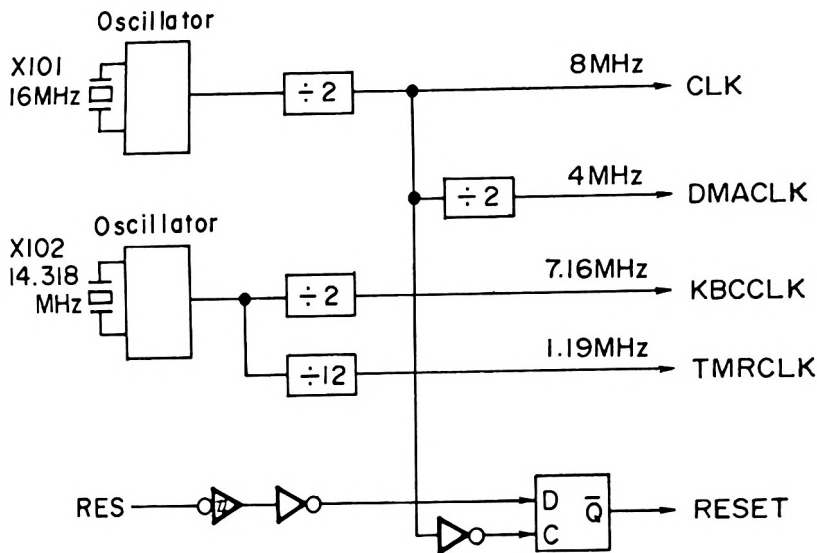


Figure 4-8 Clock Generator

When the power is turned on, the CPU and peripheral circuits are reset by GA1 using RES signal (this Schmitt-trigger input generates the RESET output). The reset timing is provided by RES input to Schmitt-trigger input gate and flip-flop, which synchronizes the reset timing to the falling edge of CLK.

Memory Map

Figure 4-9 Memory Map shows the location on the board of the IC and the corresponding memory ROW Address Strobe (RAS0, RAS1, RAS2, RAS3).

FFFFFH	IPL ROM BIOS	(32 KB)	
F8000H	EXPANSION ROM AREA	(224 KB)	
C0000H	(NOT USED)	(16 KB)	
BC000H	VIDEO RAM	(16 KB)	
B8000H	(NOT USED)	(96 KB)	
A0000H	RAM (IC207, 208)	(64 KB)	← $\overline{\text{RAS3}}$
90000H	RAM (IC205, 206)	(64 KB)	← $\overline{\text{RAS2}}$
80000H	RAM (IC203, 204)	(256 KB)	← $\overline{\text{RAS1}}$
40000H	RAM (IC201, 202)	(256 KB)	← $\overline{\text{RAS0}}$
00000H			

Figure 4-9 Memory Map

RAM Control Circuit

Figure 4-10 shows the DRAM refresh control logic. The Tandy 1100FD uses the Timer/Counter and DMAC for DRAM refresh.

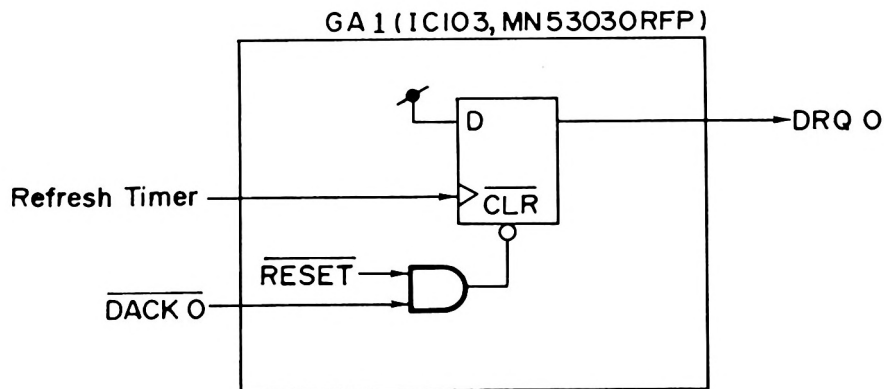


Figure 4-10 DRAM Refresh Control Logic in GA1 (IC103)

The Refresh Timer generates a pulse about every 15 μ sec.

Figure 4-11 shows the circuit of active low $\overline{\text{RAS0}}$, $\overline{\text{RAS1}}$, $\overline{\text{RAS2}}$ and $\overline{\text{RAS3}}$ signal generators.

Figure 4-12 shows the circuit of active low Column-Address strobe $\overline{\text{CAS}}$ and memory address multiplexer.

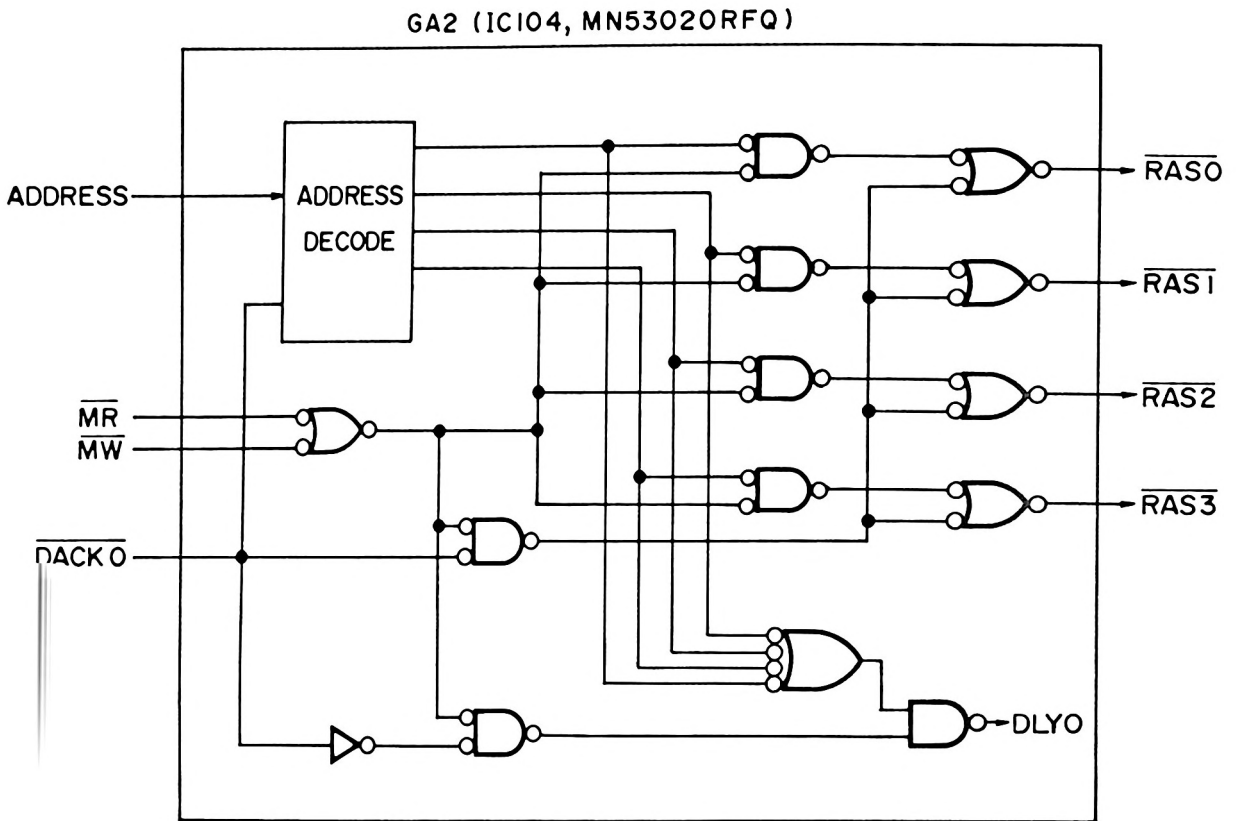


Figure 4-11 Circuit of $\overline{\text{RAS0}}$, $\overline{\text{RAS1}}$, $\overline{\text{RAS2}}$ and $\overline{\text{RAS3}}$ Signal Generators in GA2 (IC104)

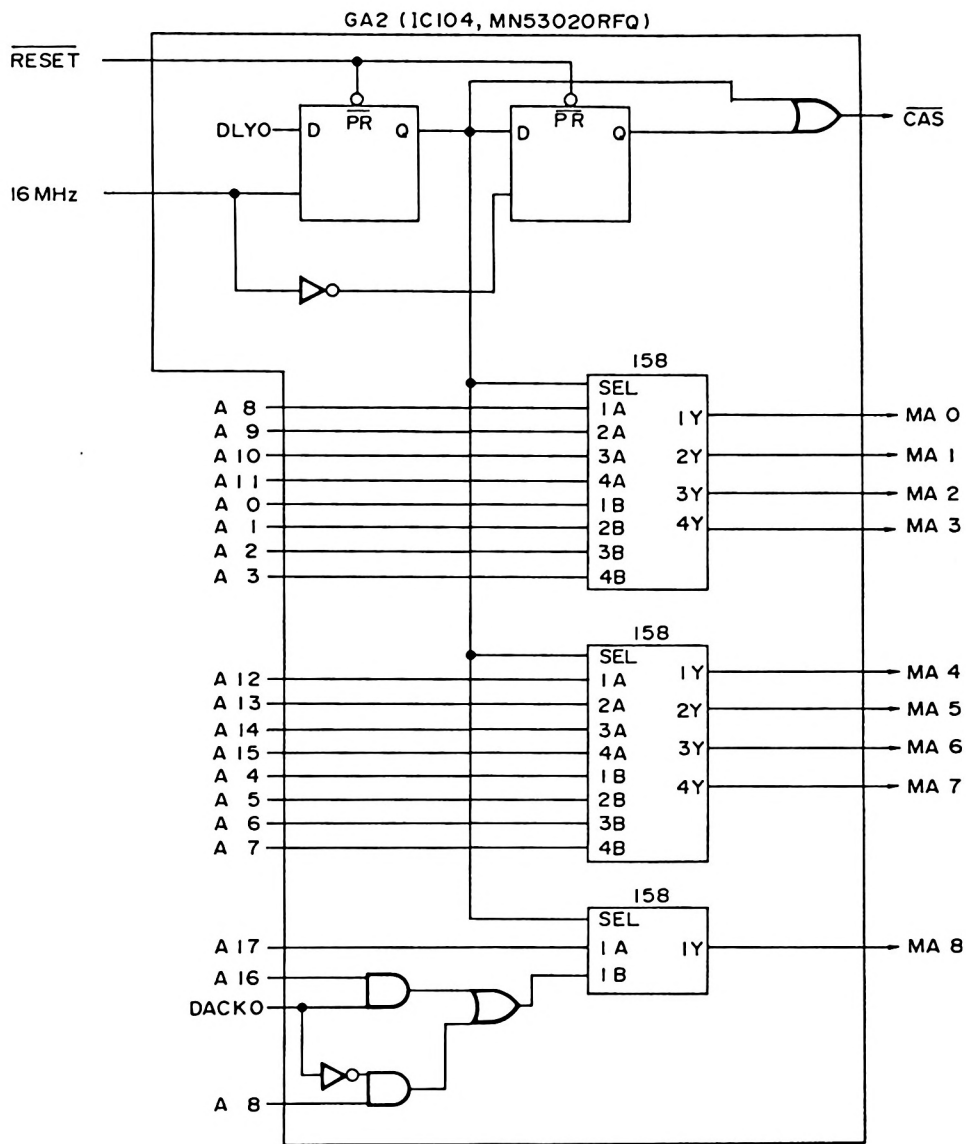


Figure 4-12 Circuit of $\overline{\text{CAS}}$ (Column Address Strobe) and Memory Address Multiplexer in GA2 (IC104)

ROM Control Circuit

The active low $\overline{\text{SELBIOS}}$ signal is a chip enable ($\overline{\text{CE}}$) signal for the BIOS ROM. It is decoded in GA2.

Figure 4-13 shows the BIOS ROM Control Circuit in GA2.

The active low $\overline{\text{APROM}}$ signal is a chip enable ($\overline{\text{CE}}$) signal for DESKMATE/DOS ROM. It is decoded in GA1.

Figure 4-14 shows the Address Decode Circuit in GA1. Figure 4-15 shows ROM BIOS and figure 4-16 shows DESKMATE/DOS ROM.

DESKMATE/DOS ROM is divided into eight 64 K byte blocks. The upper three Address bits of this ROM are used as bank select addresses. I/O address 210H is decoded to latch D0-D2 in order to generate the upper three Addresses.

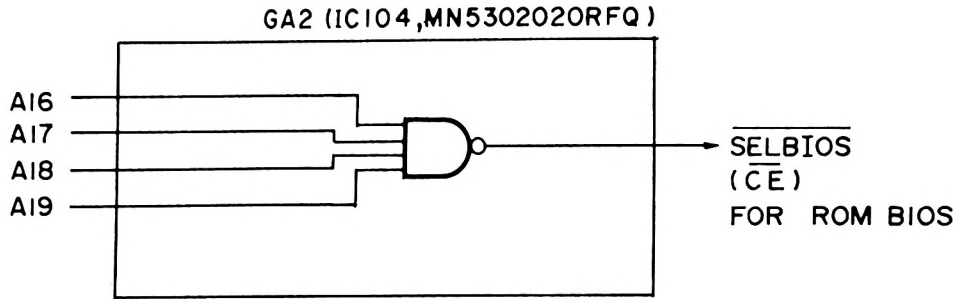


Figure 4-13 BIOS ROM Control Circuit in GA2 (IC104)

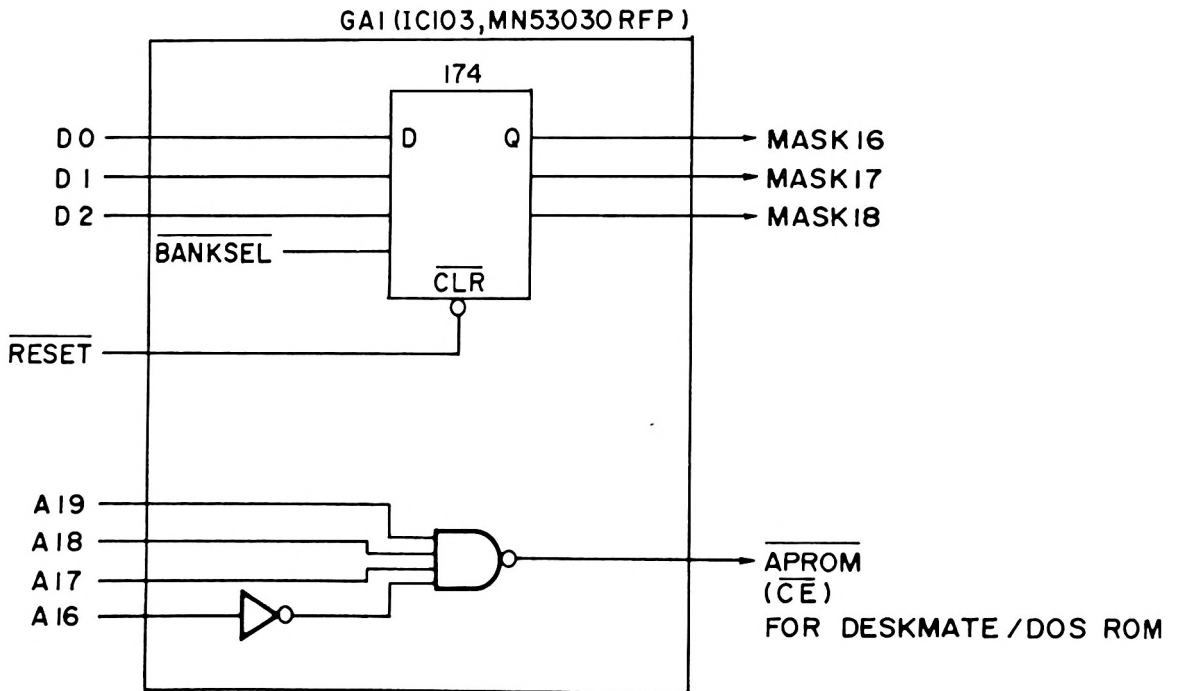


Figure 4-14 Address Decode Circuit in GA1 (IC103)

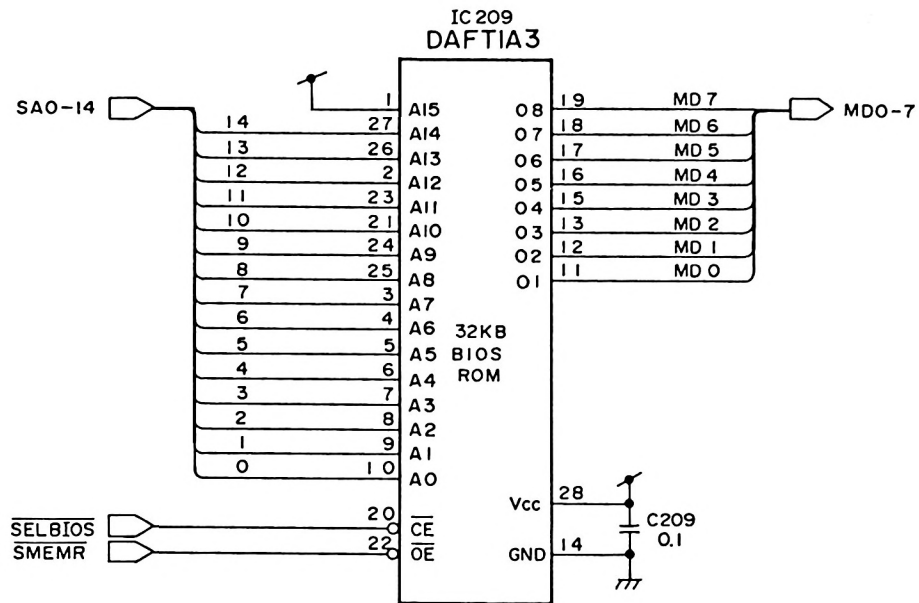


Figure 4-15 ROM BIOS

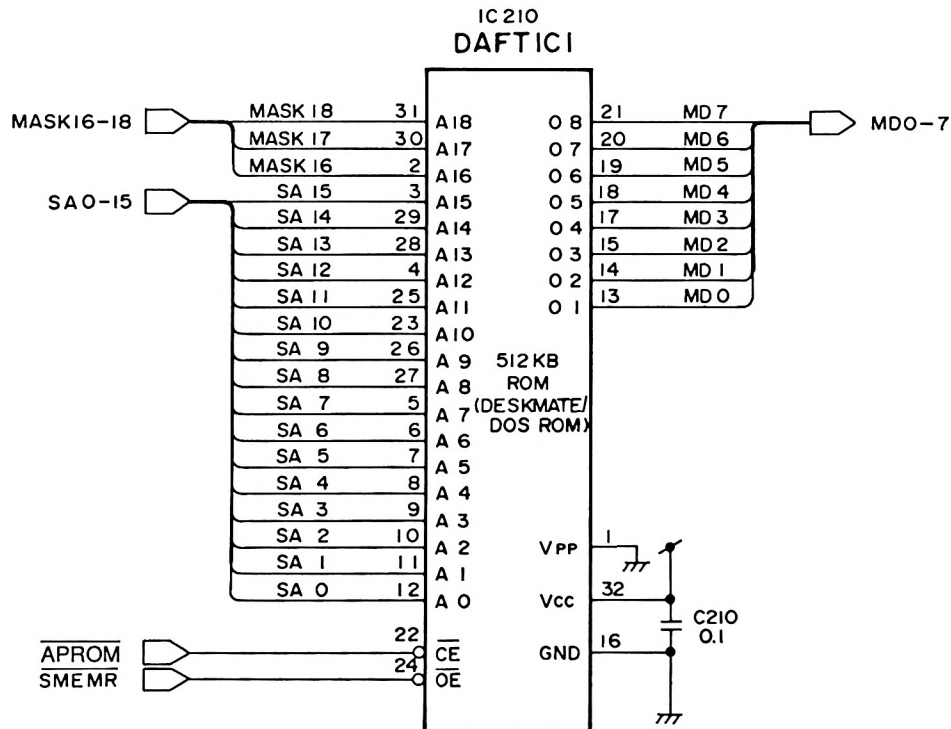


Figure 4-16 DESKMATE/DOS ROM

I/O Address Map

I/O Port Map of System

I/O Port Map Summary

<u>Block</u>	<u>Usage</u>	<u>Function</u>
0000-001F	0000-001F	DMA Function
0020-003F	0020-0027	Interrupt Controller
0040-005F	0040-0047	Timer
0060-007F	0060-0062	PIO Function
0080-009F	0080-008F	DMA Page Register
00A0-00BF	00A0	NMI-Mask Register
00E0-00FF	00E0	Control Register
0100-020F	—	(Reserved)
0210-021F	0210	Bank Select Register
0220-02F7	—	(Reserved)
02F8-02FF	02F8-02FF	Serial Port Secondary (COM2)
0300-031F	—	(Reserved)
0330-034F	—	(Reserved)
0350-035F	0350-035F	Real Time Clock
0370-0377	—	(Reserved)
0378-037B	0378-037B	Printer
037C-037F	037C	EEPROM
0380-03CF	—	(Reserved)
03D0-03DF	03D0-03DF	System Video
03E0-03EF	—	(Reserved)
03F0-03F7	03F0-03F7	Floppy Disk Controller
03F8-03FF	03F3-03FF	Serial Port Primary (COM1)
0400-FFE7	—	(Not usable)

<u>Address</u>	<u>Description</u>
0000	<p>DMA Controller</p> <p>IOW==0: Channel 0 Base and Current Address</p> <p>Internal Flip/Flop=0: Write A0–A7 Internal Flip/Flop=1: Write A8–A15</p> <p>IOR==0: Channel 0 Current Address</p> <p>Internal Flip/Flop=0: Read A0–A7 Internal Flip/Flop=1: Read A8–A15</p>
0001	<p>DMA Controller</p> <p>IOW==0: Channel 0 Current Word Count</p> <p>Internal Flip/Flop=0: Write W0–W7 Internal Flip/Flop=1: Write W8–W15</p> <p>IOR==0: Channel 0 Current Word Count</p> <p>Internal Flip/Flop=0: Read W0–W7 Internal Flip/Flop=1: Read W8–W15</p>
0002	<p>DMA Controller</p> <p>IOW==0: Channel 1 Base and Current Address</p> <p>Internal Flip/Flop=0: Write A0–A7 Internal Flip/Flop=1: Write A8–A15</p> <p>IOR==0: Channel 1 Current Address</p> <p>Internal Flip/Flop=0: Read A0–A7 Internal Flip/Flop=1: Read A8–A15</p>
0003	<p>DMA Controller</p> <p>IOW==0: Channel 1 Base and Current Word Count</p> <p>Internal Flip/Flop=0: Write W0–W7 Internal Flip/Flop=1: Write W8–W15</p> <p>IOR==0: Channel 1 Current Word Count</p> <p>Internal Flip/Flop=0: Read W0–W7 Internal Flip/Flop=1: Read W8–W15</p>

<u>Address</u>	<u>Description</u>
0004	<p>DMA Controller</p> <p>IOW=0: Channel 2 Base and Current Address</p> <p>Internal Flip/Flop=0: Write A0–A7 Internal Flip/Flop=1: Write A8–A15</p> <p>IOR=0: Channel 2 Current Address</p> <p>Internal Flip/Flop=0: Read A0–A7 Internal Flip/Flop=1: Read A8–A15</p>
0005	<p>DMA Controller</p> <p>IOW=0: Channel 2 Base and Current Word Count</p> <p>Internal Flip/Flop=0: Write W0–W7 Internal Flip/Flop=1: Write W8–W15</p> <p>IOR=0: Channel 2 Current Word Count</p> <p>Internal Flip/Flop=0: Read W0–W7 Internal Flip/Flop=1: Read W8–W15</p>
0006	<p>DMA Controller</p> <p>IOW=0: Channel 3 Base and Current Address</p> <p>Internal Flip/Flop=0: Write A0–A7 Internal Flip/Flop=1: Write A8–A15</p> <p>IOR=0: Channel 3 Current Address</p> <p>Internal Flip/Flop=0: Read A0–A7 Internal Flip/Flop=1: Read A8–A15</p>
0007	<p>DMA Controller</p> <p>IOW=0: Channel 3 Base and Current Word Count</p> <p>Internal Flip/Flop=0: Write W0–W7 Internal Flip/Flop=1: Write W8–W15</p> <p>IOR=0: Channel 3 Current Word Count</p> <p>Internal Flip/Flop=0: Read W0–W7 Internal Flip/Flop=1: Read W8–W15</p>

AddressDescription

0008

DMA Controller

IOW--=0: Write Command Register

<u>Bit</u>	<u>Description</u>
0	0=Memory to Memory Disable 1=Memory to Memory Enable
1	0=Channel 0 Address Hold Disable 1=Channel 0 Address Hold Enable X=If Bit 0 =0
2	0=Controller Enable 1=Controller Disable
3	0=Normal Timing 1=Compressed Timing X=If Bit 0 =1
4	0=Fixed Priority 1=Rotating Priority
5	0=Late Write Selection 1=Extended Write Selection X=If Bit 3 =1
6	0=DREQ Sense Active High 1=DREQ Sense Active Low
7	0=DACK Sense Active Low 1=DACK Sense Active High

IOR--=0: Read Status Register

<u>Bit</u>	<u>Description</u>
0	1=Channel 0 HAS Reached DMATC
1	1=Channel 1 HAS Reached DMATC
2	1=Channel 2 HAS Reached DMATC
3	1=Channel 3 HAS Reached DMATC
4	1=Channel 0 Request
5	1=Channel 1 Request
6	1=Channel 2 Request
7	1=Channel 3 Request

<u>Address</u>	<u>Description</u>
----------------	--------------------

0009 DMA Controller

IOW==0: Write Request Register

<u>Bit</u>	<u>Description</u>	
<u>Bits 0-1</u>		
<u>Bit 1</u>	<u>Bit 0</u>	
0	0	Select Channel 0
0	1	Select Channel 1
1	0	Select Channel 2
1	1	Select Channel 3
<u>Bit 2</u>		
0		Reset Request Bit
1		Set Request Bit
<u>Bit 3-7</u>		Don't Care

IOR==0: Illegal

000A DMA Controller

IOW==0: Write Single Mask Register

<u>Bit</u>	<u>Description</u>	
<u>Bits 0-1</u>		
<u>Bit 1</u>	<u>Bit 0</u>	
0	0	Select Channel 0 Mask Bit
0	1	Select Channel 1 Mask Bit
1	0	Select Channel 2 Mask Bit
1	1	Select Channel 3 Mask Bit
<u>Bit 2</u>		
0		Clear Mask Bit (Enable Channel)
1		Set Mask Bit (Disable channel)
<u>Bit 3-7</u>		Don't Care

IOR==0: Illegal

AddressDescription

000B

DMA Controller

IOW=0: Write Mode Register

<u>Bit</u>		<u>Description</u>
<u>Bits 0-1</u>		
<u>Bit 1</u>	<u>Bit 0</u>	
0	0	Channel 0 Select
0	1	Channel 1 Select
1	0	Channel 2 Select
1	1	Channel 3 Select
<u>Bit 2-3</u>		
0	0	Verify Transfer
0	1	Write Transfer to Memory
1	0	Read Transfer to Memory
1	1	Illegal
X		If Bits 6 and 7=11
<u>Bit 4</u>		
0		Autoinitialization Enable
1		Autoinitialization Disable
<u>Bit 5</u>		
0		Address Increment Select
1		Address Decrement Select
<u>Bit 6-7</u>		
<u>Bit 7</u>	<u>Bit 6</u>	
0	0	Demand Mode Select
0	1	Single Mode Select
1	0	Block Mode Select
1	1	Cascade Mode Select

IOR=0: Illegal

000C

DMA Controller

IOW=0: Clear Byte Pointer Flip/Flop

IOR=0: Illegal

<u>Address</u>	<u>Description</u>												
000D	DMA Controller IOW=0: Master Clear IOR=0: Read Temporary Register												
000E	DMA Controller IOW=0: Clear Mask Register IOR=0: Illegal												
000F	DMA Controller IOW=0: Write All Mask Register Bits												
	<table border="1"> <thead> <tr> <th><u>Bit</u></th> <th><u>Description</u></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0=Clear Channel 0 Mask Bit (Enable) 1=Set Channel 0 Mask Bit (Disable)</td> </tr> <tr> <td>1</td> <td>0=Clear Channel 1 Mask Bit (Enable) 1=Set Channel 1 Mask Bit (Disable)</td> </tr> <tr> <td>2</td> <td>0=Clear Channel 2 Mask Bit (Enable) 1=Set Channel 2 Mask Bit (Disable)</td> </tr> <tr> <td>3</td> <td>0=Clear Channel 3 Mask Bit (Enable) 1=Set Channel 3 Mask Bit (Disable)</td> </tr> <tr> <td>4-7</td> <td>Don't Care</td> </tr> </tbody> </table>	<u>Bit</u>	<u>Description</u>	0	0=Clear Channel 0 Mask Bit (Enable) 1=Set Channel 0 Mask Bit (Disable)	1	0=Clear Channel 1 Mask Bit (Enable) 1=Set Channel 1 Mask Bit (Disable)	2	0=Clear Channel 2 Mask Bit (Enable) 1=Set Channel 2 Mask Bit (Disable)	3	0=Clear Channel 3 Mask Bit (Enable) 1=Set Channel 3 Mask Bit (Disable)	4-7	Don't Care
<u>Bit</u>	<u>Description</u>												
0	0=Clear Channel 0 Mask Bit (Enable) 1=Set Channel 0 Mask Bit (Disable)												
1	0=Clear Channel 1 Mask Bit (Enable) 1=Set Channel 1 Mask Bit (Disable)												
2	0=Clear Channel 2 Mask Bit (Enable) 1=Set Channel 2 Mask Bit (Disable)												
3	0=Clear Channel 3 Mask Bit (Enable) 1=Set Channel 3 Mask Bit (Disable)												
4-7	Don't Care												
	IOR=0: Illegal												
0010-001F	Same as 0000-000F												

Address

Description

0020

8259A Interrupt Controller

Note: Initialization words are set up by the operating system and are generally not to be changed. Writing an initialization word might cancel pending interrupts.

<u>Bit</u>	<u>Description</u>
Bit 4=1	Initialization Command Word 1
<u>Bit 0</u>	
0	
1	ICW4 Needed
<u>Bit 1</u>	
0	Cascade Mode
1	Single Mode
Bit 2	Not used
<u>Bit 3</u>	
0	Edge Triggered Mode
1	Level Triggered Mode
Bit 5-7	Not used
Bit 4=0	Operation Command Word 2
Bit 3=0	Bit0-2: Determine the Interrupt level acted on when the SL Bit is active

<u>Interrupt Level</u>	<u>=</u>	<u>0</u>	<u>1</u>	<u>2</u>	<u>3</u>	<u>4</u>	<u>5</u>	<u>6</u>	<u>7</u>
Bit 0 (L0)	:	0	1	0	1	0	1	0	1
Bit 1 (L1)	:	0	0	1	1	0	0	1	1
Bit 2 (L2)	:	0	0	0	0	1	1	1	1

Bits 5-7: Control Rotate and End of Interrupt modes (SL)

<u>B7</u>	<u>B6</u>	<u>B5</u>	<u>Description</u>	
0	0	1	Non-Specific EOI Command	End of Interrupt
0	1	1	Specific EOI Command	End of Interrupt
1	0	1	Rotate On Non-Specific EOI	Auto Rotation
1	0	0	Rotate In Automatic EOI Mode	(Set) Auto Rotation
0	0	0	Rotate In Automatic EOI Mode	(Clear) Rotation
1	1	1	*Rotate On Specific EOI Command	Specific Rotation
1	1	0	*Set Priority Command	Specific Rotation
0	1	1	No Operation	

(*L0-L2 Are Used)

Address

Description

0020

8259A Interrupt Controller

<u>Bit</u>	<u>Description</u>
Bit 4=0 & Bit 3=1 Operation Command Word 1	
Bit 0-1:0	
<u>Bit 1</u>	<u>Bit 0</u> —Read Register Command
0	0 No Action
0	1 No Action
1	0 Read IR Register On Next IOR- Pulse
1	1 Read IS Register On Next IOR- Pulse
Bit 2	
<u>0</u>	No Poll Command
1	Poll Command
Bit 5-6	
<u>Bit 5</u>	<u>Bit 6</u> —Special Mask Mode
0	0 No Action
0	1 No Action
1	0 Reset Special Mask
1	1 Set Special Mask

Bit 7=0

0021

8259A Interrupt Controller

Initialization Command Word 2

<u>Bit</u>	<u>Description</u>
Bit 0-7	Not used (8080/8085 Mode)
Bit 3-7:	T3-T7 of Interrupt Vector Address (8086/8088 Mode)

Initialization Command Word 3 (Master Device)

Bits 0-7	1 Indicated IR Input has a Slave 0 Indicated IR Input does not have a Slave
----------	--

Address

Description

0021

8259A Interrupt Controller

Initialization Command Word 3 (Slave Device)

<u>Bit</u>		<u>Description</u>	
Bits 0-2		ID0-2	
<u>Bit 2</u>	<u>Bit 1</u>	<u>Bit 0</u>	<u>Slave ID #</u>
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Bits 3-7=0 (Not used)

Initialization Command Word 4

<u>Bit 0</u>	<u>Type of Processor</u>	
0	8080/8085 Mode	
1	8086/8088 Mode	
<u>Bit 1</u>	<u>Type of End of Interrupt</u>	
0	Normal EOI	
1	Auto EOI	
<u>Bit 2-3</u>		<u>Buffering Mode</u>
<u>Bit 3</u>	<u>Bit 2</u>	
0	X	Non-Buffered Mode
1	0	Buffered Mode/Slave
1	1	Buffered Mode/Master
<u>Bit 4</u>	<u>Nesting Mode</u>	
0	Not Special Fully Nested Mode	
1	Special Fully Nested Mode	

Bit 5-7= (Not used)

<u>Address</u>	<u>Description</u>								
0021	8259A Interrupt Controller Operation Command Word 1 IOR-								
	<table border="1"> <thead> <tr> <th><u>Bit</u></th> <th><u>Description</u></th> </tr> </thead> <tbody> <tr> <td>Bit 0-7</td> <td>Interrupt Mask For IRQ0-IRQ7</td> </tr> <tr> <td>0</td> <td>Mask Reset (Enable)</td> </tr> <tr> <td>1</td> <td>Mask Set (Disable)</td> </tr> </tbody> </table>	<u>Bit</u>	<u>Description</u>	Bit 0-7	Interrupt Mask For IRQ0-IRQ7	0	Mask Reset (Enable)	1	Mask Set (Disable)
<u>Bit</u>	<u>Description</u>								
Bit 0-7	Interrupt Mask For IRQ0-IRQ7								
0	Mask Reset (Enable)								
1	Mask Set (Disable)								

Note: Peripherals requesting an interrupt service must generate a low to high edge and then remain at a logic high level until service is acknowledged. Failure to do so results in a Default Service for IRQ7.

0022-0027	Same as 0020-0021
0028-003F	Not used
0040/0044	8254-2 Timer IOW-=0: Load Counter No. 0 IOR-=0: Read Counter No. 0
0041/0045	8254-2 Timer IOW-=0: Load Counter No. 1 IOR-=0: Read Counter No. 1
0042/0046	8254-2 Timer IOW-=0: Load Counter No. 2 IOR-=0: Read Counter No. 2

<u>Address</u>	<u>Description</u>
----------------	--------------------

0043/0047 8254-2 Timerupt Controller

IOW==0: Write Control Word

Control Word Format

<u>Bit</u>	<u>Description</u>
Bit 0	BCD
0	Binary Counter 16 Bits
1	BCD Counter (4 Decades)

Bits 1-3 Mode Selection

<u>Bit 3</u>	<u>Bit 2</u>	<u>Bit 1</u>	<u>Mode</u>
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

0043/0047 8254-2 Timer

<u>Bit</u>	<u>Description</u>	
Bit 4-5	Read/Load	
<u>Bit 5</u>	<u>Bit 4</u>	
0	0	Counter Latching Operation
0	1	Read/Load LSB Only
1	0	Read/Load MSB Only
1	1	Read/Load LSB First, then MSB

Bit 6-7 Select Counter

<u>Bit 7</u>	<u>Bit 6</u>	<u>Description</u>
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
2	1	Read Back Operation

IOR==0: No-Operation 3-State

0048-005F Not used

<u>Address</u>	<u>Description</u>
0060	Port A/Keyboard Interface Control Ports (Read Only)

<u>Bit</u>	<u>Description</u>
0	Keyboard Bit 0—LSB
1	Keyboard Bit 1
2	Keyboard Bit 2
3	Keyboard Bit 3
4	Keyboard Bit 4
5	Keyboard Bit 5
6	Keyboard Bit 6
7	Keyboard Bit 7—MSB

0061 Port B Read or Write

<u>Bit</u>	<u>Description</u>
0	+8254 #2 gate for Beeper Tone
1	+Enable Beeper
2	Not used
3	Not used
4	Not used
5	+Low Battery NMI Mask On
6	–Keyboard clock low
7	–Enable keyboard

0062 Port C (Read Only)

<u>Bit</u>	<u>Description</u>
0	Not used
1	Not used
2	Not used
3	Not used
4	EEPROM Serial Data Out
5	8254 #2 out
6	Not used
7	Not used

0063–007F Reserved

0080 DMA Page Register (Reserved for Diagnostics)
(Write Only)

0081 DMA Channel 2 Page Register (Write Only)

<u>Bit</u>	<u>Description</u>
Bit 0	Address A16
Bit 1	Address A17
Bit 2	Address A18
Bit 3	Address A19

<u>Address</u>	<u>Description</u>										
0082	DMA Channel 3 Page Register (Write Only)										
	<table border="1"> <thead> <tr> <th><u>Bit</u></th> <th><u>Description</u></th> </tr> </thead> <tbody> <tr> <td>Bit 0</td> <td>Address A16</td> </tr> <tr> <td>Bit 1</td> <td>Address A17</td> </tr> <tr> <td>Bit 2</td> <td>Address A18</td> </tr> <tr> <td>Bit 3</td> <td>Address A19</td> </tr> </tbody> </table>	<u>Bit</u>	<u>Description</u>	Bit 0	Address A16	Bit 1	Address A17	Bit 2	Address A18	Bit 3	Address A19
<u>Bit</u>	<u>Description</u>										
Bit 0	Address A16										
Bit 1	Address A17										
Bit 2	Address A18										
Bit 3	Address A19										
0083	DMA Channel 0–1 Page Register (Write Only)										
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<u>Bit</u>	<u>Description</u>										
Bit 0	Address A16										
Bit 1	Address A17										
Bit 2	Address A18										
Bit 3	Address A19										
0084–008F	Same as 0080–0083										
0090–009F	Not used										
00A0	NMI-Mask register, (Write Only)										
	<table border="1"> <thead> <tr> <th><u>Bit</u></th> <th><u>Description</u></th> </tr> </thead> <tbody> <tr> <td>0–6</td> <td>Not used</td> </tr> <tr> <td>7</td> <td>1 NMI-Enabled 0 NMI-Disabled</td> </tr> </tbody> </table>	<u>Bit</u>	<u>Description</u>	0–6	Not used	7	1 NMI-Enabled 0 NMI-Disabled				
<u>Bit</u>	<u>Description</u>										
0–6	Not used										
7	1 NMI-Enabled 0 NMI-Disabled										
00A1–00A7	Reserved										
00A8–00AF	Not used										
00B0–00DF	Not used										

<u>Address</u>	<u>Description</u>
----------------	--------------------

00E0 Control Port (Read/Write)

<u>Bit</u>	<u>Description</u>
0	Not used
1	Reserved
2	CPU Clock Select 0=8 MHz
3	Serial Port Select 0=COM1: RS-232C, COM2: MODEM 1=COM1: MODEM, COM2: RS-232C
4	Not used
5	Not used
6	LCD Power Control 0=Power off 1=Power on
7	Internal MODEM Power Control 0=Power off 1=Power on

(Read)

<u>Bit</u>	<u>Description</u>
0	Not used
1	Reserved
2	CPU Clock Status
3	Serial Port Status
4	Not used
5	Not used
6	LCD Power Status
7	Internal MODEM Power Status

00E1-00FF Reserved

0100-020F Reserved

0210/0214 Bank select Register (Write Only)

Note: There are 8 banks of 64 K bytes in 512 K Bytes MASK ROM (We call DESKMATE/DOS ROM). When CPU selects this Bank, the data included in the selected bank is loaded in memory address E0000H-EFFFFH.

<u>Bank Select</u>	<u>D2</u>	<u>D1</u>	<u>D0</u>
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

0211-0213 Not used
 0215-021F Not used
 0220-02F7 Reserved

<u>Address</u>	<u>Description</u>
02F8-02FF	Serial Port Secondary (COM2 Optional)
02F8	Write Transmitter Holding Register (Character to send DLAB="0")

<u>Bit</u>	<u>Description</u>
0	Bit 0—LSB (First Bit Sent Serially)
1	Bit 1
2	Bit 2
3	Bit 3
4	Bit 4
5	Bit 5
6	Bit 6
7	Bit 7—MSB

02F8 Read Receiver Buffer Register (Character Received DLAB="0")

<u>Bit</u>	<u>Description</u>
0	Bit 0—LSB (First Bit Received Serially)
1	Bit 1
2	Bit 2
3	Bit 3
4	Bit 4
5	Bit 5
6	Bit 6
7	Bit 7—MSB

02F8 Divisor Latch LSB (Divisor Latch Access Bit DLAB="1")

<u>Bit</u>	<u>Description</u>
0	Bit 0
1	Bit 1
2	Bit 2
3	Bit 3
4	Bit 4
5	Bit 5
6	Bit 6
7	Bit 7

02F9 Divisor Latch MSB (Divisor Latch Access Bit DLAB="1" LAB="0")

<u>Bit</u>	<u>Description</u>
0	Bit 0
1	Bit 1
2	Bit 2
3	Bit 3
4	Bit 4
5	Bit 5
6	Bit 6
7	Bit 7

<u>Address</u>	<u>Description</u>																															
02F9	Interrupt Enable Register (DLAB="0")																															
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02FA	Interrupt Identification Register (Read Only)																															
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7	"0"=Access Receiver Buffer "1"=Access Divisor Latches																															

AddressDescription

02FC

Modem Control Register

<u>Bit</u>	<u>Description</u>
0	"0"=Data Terminal Ready (DTR) Output High "1"=Data Terminal Ready (DTR) Output Low
1	"0"=Request to send (RTS) Output High "1"=Request to send (RTS) Output Low
2	Not Connected
3	"0"=Interrupt Disable "1"=Interrupt Enable
4	"0"=Loop Disabled "1"=Loop Enabled
5-7	Always Logical "0"

02FD

Line Status Register

<u>Bit</u>	<u>Description</u>
0	"0"=Data Ready (DR) Not Ready "1"=Data Ready (DR) Ready
1	"0"=Overrun Error (OE) No Error "1"=Overrun Error (OE) Error
2	"0"=Parity Error (PE) No Error "1"=Parity Error (PE) Error
3	"0"=Framing Error (FE) No Error "1"=Framing Error (FE) Error
4	"0"=Break Interrupt (BI) No Break "1"=Break Interrupt (BI) Break
5	"0"=Transmitter Holding Register Empty (THRE) Not Empty "1"=Transmitter Holding Register Empty (THRE) Empty
6	"0"=Transmitter Empty (TEMT) Not Empty "1"=Transmitter Empty (TEMT) Empty
7	Always Logical "0"

Address	Description
---------	-------------

02FE MODEM Status Register

Bit	Description
0	Delta Clear to Send (DCTS)
1	Delta Data Set Ready (DDSR)
2	Trailing Edge of Ring Indicator "1"=On "0"=Off
3	Delta Received Line Signal Detect (If Bit 0, 1, 2, or 3 is set to a "1", MODEM status interrupt is generated.)
4	"0"=Clear to Send (CTS)
5	"0"=Data Set Ready (DSR)
6	"0"=Ring Indicator (RI)
7	"0"=Received Line Signal Detect (RLSD)

02FF Reserved

0300-034F Reserved

0350-035F
(BANK 0) Real Time Clock

Address	Bit 3	Bit 2	Bit 1	Bit 0	Description
0350					1 sec. Counter
0351	x				10 sec. Counter
0352					1 min. Counter
0353	x				10 min. Counter
0354					1 hr. Counter
0355	x	x			10 hr. Counter
0356	x				Week Counter
0357					1 day Counter
0358	x	x			10 days Counter
0359					1 month Counter
035A	x	x	x		10 months Counter
035B					1 year Counter
035C					10 years Counter
035D	Timer EN	Alarm EN		BANK 1/0	MODE Register
035E	Test3	Test2	Test1	Test0	Test Register
035F	1 Hz ON	16 Hz ON	Timer Reset	Alarm Reset	Reset Register

Address	Description
---------	-------------

0350-035F Real Time Clock
(BANK 1)

Address	Bit 3	Bit 2	Bit 1	Bit 0	Description
0350	x				CLK OUT Select Register
0351	x	x	x		Adjust
0352					Alarm 1 min. Register
0353	x				Alarm 10 min. Register
0354					Alarm 1 hr. Register
0355	x	x			Alarm 10 hr. Register
0356	x				Alarm Week Register
0357					Alarm 1 day Register
0358	x	x			Alarm 10 days Register
0359	x	x	x	x	1 month Counter
035A	x	x	x		12/24 Hour Selector
035B	x	x			Leap Year Counter
035C	x	x	x	x	10 years Counter
035D	Timer EN	Alarm EN		BANK 1/0	MODE Register
035E	Test3	Test2	Test1	Test0	Test Register
035F	1 Hz ON	16 Hz ON	Timer Reset	Alarm Reset	Reset Register

0370-0377 Reserved

<u>Address</u>	<u>Description</u>																		
0378	Printer—Data Latch (Read/Write)																		
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0379	Printer—Read Status																		
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<u>Bit</u>	<u>Description</u>																		
0	"1"																		
1	"1"																		
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3	"0"=Error																		
4	"1"=Printer Select																		
5	"0"=Out of Paper																		
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037A(037E)	Printer—Control Latch (Read/Write)																		
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037B	Not used																		
037C	<table border="1"> <thead> <tr> <th><u>Bit</u></th> <th><u>Description</u></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>EEPROM Serial Data Input</td> </tr> <tr> <td>1</td> <td>+EEPROM Chip Select</td> </tr> <tr> <td>2</td> <td>EEPROM Serial Data Clock</td> </tr> </tbody> </table>	<u>Bit</u>	<u>Description</u>	0	EEPROM Serial Data Input	1	+EEPROM Chip Select	2	EEPROM Serial Data Clock										
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0	EEPROM Serial Data Input																		
1	+EEPROM Chip Select																		
2	EEPROM Serial Data Clock																		
037D–03D3	Not used																		
03D4	6845 Address Register																		

AddressDescription

03D5 6845 Data Register

Register	Address No.	Register Designation	Read/Write
AR	—	Address Register	W
R0	00	Horizontal Total	W
R1	01	Horizontal Displayed	W
R2	02	HYSNC Position	W
R3	03	HSYNC/VSYNC Width	W
R4	04	Vertical Total	W
R5	05	Vertical Total Adjust	W
R6	06	Vertical Displayed	W
R7	07	VSYNC Position	W
R8	08	Reserved	—
R9	09	Max. Scan Line Address	W
R10	0A	Cursor Start Scan Line	W
R11	0B	Cursor End Scan Line	W
R12	0C	Start Address (H)	R/W
R13	0D	Start Address (L)	R/W
R14	0E	Cursor Address (H)	R/W
R15	0F	Cursor Address (L)	R/W
R16	10	VRAM Address (H)	W
R17	11	VRAM Address (L)	W
R18	12	Extend	R/W
R19	13	Duty Control	R/W
R20	14	Reserved	—
R21	15	Reserved	—
R22	16	Reserved	—
R23	17	Reserved	—
R24	18	Reserved	—
R25	19	Reserved	—
R26	1A	Under Line Start Raster	R/W
R27	1B	Write Protect	R/W
R28	1C	Write Protect	R/W
R29	1D	Reserved	—
R30	1E	Display Control	R/W
R31	1F	Hard Control	R/W

R: Read, W: Write

03D6 Not used

03D7 Not used

<u>Address</u>	<u>Description</u>																		
03D8	Mode Control Register (Write Only)																		
	<table border="1"> <thead> <tr> <th><u>Bit</u></th> <th><u>Description</u></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Change the 80 x 25 character mode</td> </tr> <tr> <td>1</td> <td>Select the graphic character</td> </tr> <tr> <td>2</td> <td>Select the color set</td> </tr> <tr> <td>3</td> <td>Display data enable</td> </tr> <tr> <td>4</td> <td>Select 640 x 200 graphic mode</td> </tr> <tr> <td>5</td> <td>Alternate the background and change the blink timing</td> </tr> <tr> <td>6</td> <td>Not used</td> </tr> <tr> <td>7</td> <td>Not used</td> </tr> </tbody> </table>	<u>Bit</u>	<u>Description</u>	0	Change the 80 x 25 character mode	1	Select the graphic character	2	Select the color set	3	Display data enable	4	Select 640 x 200 graphic mode	5	Alternate the background and change the blink timing	6	Not used	7	Not used
<u>Bit</u>	<u>Description</u>																		
0	Change the 80 x 25 character mode																		
1	Select the graphic character																		
2	Select the color set																		
3	Display data enable																		
4	Select 640 x 200 graphic mode																		
5	Alternate the background and change the blink timing																		
6	Not used																		
7	Not used																		
03D9	Color Select Register (Write Only)																		
	Note: This register determines the color in the CRT mode. It is invalid to the display status in the LCD and PDP mode.																		
03DA	Status Register (Read Only)																		
	<table border="1"> <thead> <tr> <th><u>Bit</u></th> <th><u>Description</u></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Indicate the period of the display</td> </tr> <tr> <td>1</td> <td>Indicate the status of VRAM Address strobe signal</td> </tr> <tr> <td>2</td> <td>Not used</td> </tr> <tr> <td>3</td> <td>Indicate the period of the Vertical retrace</td> </tr> <tr> <td>4</td> <td>Not used</td> </tr> <tr> <td>5</td> <td>Not used</td> </tr> <tr> <td>6</td> <td>Not used</td> </tr> <tr> <td>7</td> <td>Not used</td> </tr> </tbody> </table>	<u>Bit</u>	<u>Description</u>	0	Indicate the period of the display	1	Indicate the status of VRAM Address strobe signal	2	Not used	3	Indicate the period of the Vertical retrace	4	Not used	5	Not used	6	Not used	7	Not used
<u>Bit</u>	<u>Description</u>																		
0	Indicate the period of the display																		
1	Indicate the status of VRAM Address strobe signal																		
2	Not used																		
3	Indicate the period of the Vertical retrace																		
4	Not used																		
5	Not used																		
6	Not used																		
7	Not used																		
03DB	Clear VRAM Address Latch (Write Only)																		
03DC	Preset VRAM Address Latch (Write Only)																		
	Note: When this register is preset, VRAM Address Signal (MA14–MA0) is latched to the VRAM Address Registers (R16 and R17).																		
03DD–03DE	Reserved																		
03DF	Register Access Enable Register (Read/Write)																		
	Note: It is 8-bit register to be used write protection for extend register (R18–R31) of “6845” Like Register. Writing in R18–R31 is available when this register value is “7EH”. And it is prohibited to write except for ‘7EH’. All bits are cleared when reset.																		
03F0–03F1	Not used																		

<u>Address</u>	<u>Description</u>																														
03F2	DOR Register (Write Only)																														
	Bits 0–1 Drive Select																														
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<u>Bit 1</u>	<u>Bit 0</u>	<u>Description</u>																													
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Bit 5		Not used																													
Bit 6		Not used																													
Bit 7		Not used																													
03F3	Not used																														
03F4	(Read) FDC—Status (See FDC Specification) (Write) Standby Control Register																														
	Bit 0–1																														
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03F5	FDC—Data (Read/Write) (See FDC Specification)																														
03F6	Reserved																														
03F7	(Read) Digital Input Register																														
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Bit 3		Not used																													
Bit 4		Not used																													
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Bit 7		Not used																													

AddressDescription

03F8–03FF

Serial Port Primary (COM1 Optional)

03F8

Write Transmitter Holding Register (Character to send DLAB="0")

<u>Bit</u>	<u>Description</u>
0	Bit 0—LSB (First Bit Sent Serially)
1	Bit 1
2	Bit 2
3	Bit 3
4	Bit 4
5	Bit 5
6	Bit 6
7	Bit 7—MSB

03F8

Read Receiver Buffer Register (Character Received DLAB="0")

<u>Bit</u>	<u>Description</u>
0	Bit 0—LSB (First Bit Received Serially)
1	Bit 1
2	Bit 2
3	Bit 3
4	Bit 4
5	Bit 5
6	Bit 6
7	Bit 7—MSB

Divisor Latch LSB (Divisor Latch Access Bit DLAB="1")

<u>Bit</u>	<u>Description</u>
0	Bit 0
1	Bit 1
2	Bit 2
3	Bit 3
4	Bit 4
5	Bit 5
6	Bit 6
7	Bit 7

03F9

Divisor Latch MSB (Divisor Latch Access Bit DLAB="1")

<u>Bit</u>	<u>Description</u>
0	Bit 8
1	Bit 9
2	Bit 10
3	Bit 11
4	Bit 12
5	Bit 13
6	Bit 14
7	Bit 15

<u>Address</u>	<u>Description</u>																																																																							
03F9	Interrupt Enable Register (DLAB="0")																																																																							
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03FA	Interrupt Identification Register (Read Only)																																																																							
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<u>Address</u>	<u>Description</u>																		
03FC	MODEM Control Register																		
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6	"0"=Ring Indicator (RI)																		
7	"0"=Received Line Signal Detect (RLSD)																		
03FF	Reserved																		

Keyboard

Figure 4-17 shows the block diagram in GA1. The data from the keyboard is serial 8-bit data. The data goes to the data bus through I/O Port 60H (Subset of 82C55). The keyboard is controlled by IC701 (μ PD49HG). IC701 is a single chip, 8-bit microprocessor that contains 8-bit CPU, ROM, RAM, I/O Ports, and control circuit. IC701 generates strobe signal with every keystroke.

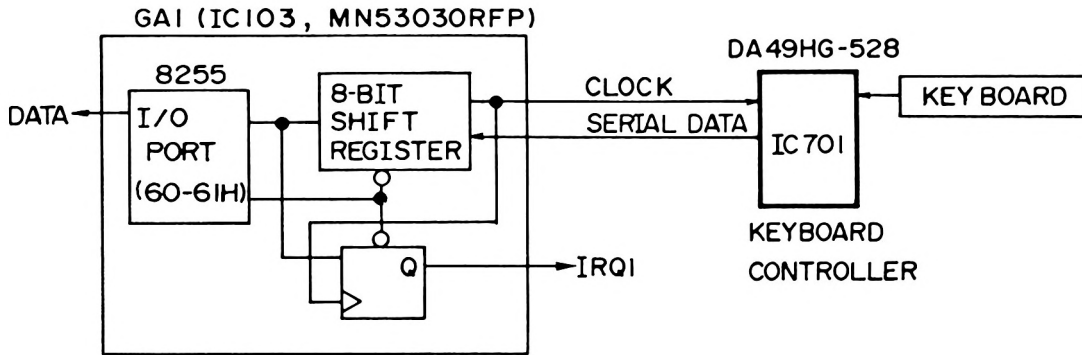


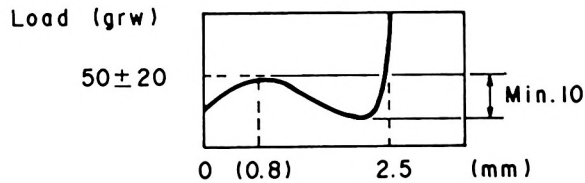
Figure 4-17 Block Diagram in GA1

Keyboard Configuration

1. Switches

1-1 Mechanical

—Function	Non-Lock release
—Operation Force	
1) Operation Force:	50±20 grW
2) Feeling:	No jamming, No abnormal sound
3) On-point load:	Max. 70 grW

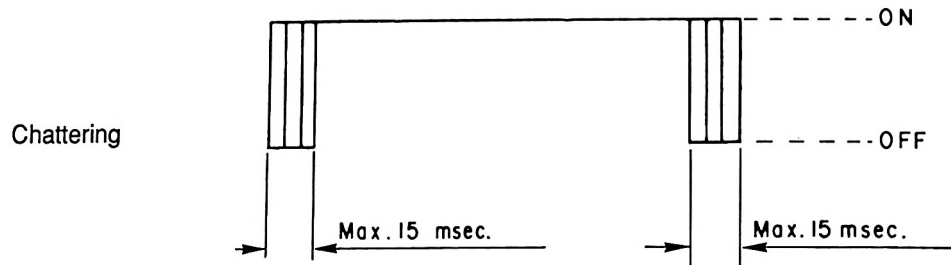


—Stroke

- | | |
|--------------------------------|------------------------------|
| 1) Full stroke
(On stroke): | 2.5±0.4 mm (at 100 grW load) |
|--------------------------------|------------------------------|

1-2 Electrical

—Circuit	1P 1T
—Max Rating	DC 5 V/2 mA
—Contact Resistance	4.5 kohms±1.5 kohms (measured with Digital Tester at 200 grW load)
—Insulation Resistance	Min. 50 Mohms (measured by Meg ohm tester at DC 100V)
—Dielectric strength	AC 100 V (RMS)/1 minute
—Chattering	Leakage Current: 1 mA (Measured with Oscilloscope) Shall be capable of satisfactory performance as mentioned below. Keytop has to be pushed to the end sufficiently by finger.



1-3 Performance Test

—Life	The switch shall operate 5 million times of make and break at 5 to 6 cycles per second with about 100 grW force at a current of 1 mA/DC and a potential of 5 V/DC under resistive load.
-------	---

Keyboard Controller Specifications

1. Keyboard Description

The keyboard has 84 keys and emulates the enhanced 101-key keyboard in XT mode. The keys consist of the following:

- 1—Fn key
 - 1—Keypad key
 - 10—Separate cursor pad
 - 60—Base keypad
 - 12—Function key
-
- 84—key (Total)

2. 10 Key Mode

The keyboard emulates the numeric keypad. Fn+Keypad toggles the state of the keyboard controller's internal flag. This emulation is called 10 Key Mode.

In normal mode, these keys produce alphabetic scan codes as shown in Table 1 on the next page.

In 10 Key Mode, these keys produce numeric keypad scan codes as shown in Table 2 on the page 4-45.

The cursor pad always produces enhanced cursor keys as shown in Table on the page 4-45. On keyboard reset, the NumLock status flag in both the keyboard controller and computer should be set to NumLock OFF.

3. Fn Key

The Fn key provides the special functions described below.

Table 4 on Page 4-46 defines the scan codes generated when Fn is active.

Fn changes the scan code of some keys. If a key is pressed before Fn, the keyboard controller should continue to send the normal scan code until the key is released.

- a. Fn+F1 through Fn+F12 provide additional function codes.
- b. Fn+Keypad toggles between 10-Key Mode and Normal Mode.
- c. Fn+Esc+NumLock toggles the internal NumLock status flag to avoid a problem when there is a mismatch between the BIOS NumLock flag and the keyboard controller NumLock flag. The mismatch occurs due the software changing the BIOS NumLock flag.

5. Limitations

The emulation of the 101 Enhanced keyboard has the following limitations:

- a. Ctrl-NumLock is never sent to the computer, the BIOS normally ignores this combination in enhanced mode.
- b. Right Ctrl and Right Alt are not supported.
- c. The International key is not supported.
- d. On the cursor pad, the E02A and E0AA during the break sequence is not sent until a non-cursor key is pressed.

Keyboard Scan Code

Table 1: Normal Mode (Fn not pressed)

Key position No.	Character Code	Make Code	Break Code	Comments
1	Esc	01	81	
2	F1	3B	BB	
3	F2	3C	BC	
4	F3	3D	BD	
5	F4	3E	BE	
6	F5	3F	BF	
7	F6	40	C0	
8	F7	41	C1	
9	F8	42	C2	
10	F9	43	C3	
11	F10	44	C4	
12	F11	57	D7	
13	F12	58	D8	
14	NumLk	45	C5	
	Pause	9DE11D45E19DC51D	—	Ctrl pressed, send once
15	Scrllk	46	C6	
	Break	E046E0C6	—	Ctrl pressed, send once
16	*	37	B7	Base case
	PrtSc	E037	E0B7	Alt, Ctrl, or Shift
17	Keypad	54	D4	
18	1!	02	82	
19	2@	03	83	
20	3#	04	84	
21	4\$	05	85	
22	5%	06	86	
23	6^	07	87	
24	7&(7)	08	88	Also see Numpad
25	8*(8)	09	89	Also see Numpad
26	9((9)	0A	8A	Also see Numpad
27	0)(*)	0B	8B	Also see Numpad

Table 1: Normal Mode (Fn not pressed)

Key position No.	Character Code	Make Code	Break Code	Comments
28	-	0C	8C	
29	=+	0D	8D	
30	Backspace	0E	8E	
31	Home	See cursor pad		
32	Tab	0F	8F	
33	Q	10	90	
34	W	11	91	
35	E	12	92	
36	R	13	93	
37	T	14	94	
38	Y	15	95	
39	U (4)	16	96	Also see Numpad
40	I (5)	17	97	Also see Numpad
41	O (6)	18	98	Also see Numpad
42	P (-)	19	99	Also see Numpad
43	[{	1A	9A	
44] }	1B	9B	
45	\.	2B	AB	
46	PgUp	See cursor pad		
47	CapsLock	3A	BA	
48	A	1E	9E	
49	S	1F	9F	
50	D	20	A0	
51	F	21	A1	
52	G	22	A2	
53	H	23	A3	
54	J (1)	24	A4	Also see Numpad
55	K (2)	25	A5	Also see Numpad
56	L (3)	26	A6	Also see Numpad
57	;; (+)	27	A7	Also see Numpad
58	""	28	A8	
59	Enter	1C	9C	
60	PgDn	See cursor pad		
61	Shift (Left)	2A	AA	
62	Z	2C	AC	
63	X	2D	AD	
64	C	2E	AE	
65	V	2F	AF	
66	B	30	B0	
67	N	31	B1	
68	M (0)	32	B2	Also see Numpad
69	, <	33	B3	
70	. > (.)	34	B4	Also see Numpad
71	/? (/)	35	B5	Also see Numpad
72	Shift (Right)	36	B6	
73	Up arrow (up)	See cursor pad		
74	End	See cursor pad		
75	Cntrl (Left)	1D	9D	
76	Fn	—	—	
77	Alt (Left)	38	B8	
78	'~	29	A9	
79	Insert	See cursor pad		
80	Delete	See cursor pad		
81	Left arrow	See cursor pad		
82	Down arrow	See cursor pad		
83	Right arrow	See cursor pad		
84	Spacebar	39	B9	

Table 2: Numpad (Numeric keypad)

Key Position No.	Character Code	Normal Mode Keypad OFF		10-key Mode Keypad On	
		Make	Break	Make	Break
24	7& (7)	08	88	47	C7
25	8* (8)	09	89	48	C8
26	9((9)	0A	8A	49	C9
27	0) (*)	0B	8B	37	B7
39	U (4)	16	96	4B	CB
40	I (5)	17	97	4C	CC
41	O (6)	18	98	4D	CD
42	P (-)	19	99	4A	CA
54	J (1)	24	A4	4F	CF
55	K (2)	25	A5	50	D0
56	L (3)	26	A6	51	D1
57	; : (+)	27	A7	4E	CE
59	Enter	1C	9C	E01C	E09C
68	M (0)	32	B2	52	D2
70	. < (.)	34	B4	53	D3
71	/? (/)	35	B5	E035	E0B5

Table 3: Cursor Pad, Separate Cursor Controls

Table 3A: Base case or NumLock ON and Shift

Table 3B: Shift case

Key Position No.	Character Code	Keypad ON or OFF Make	Keypad ON or OFF Break
31	Home	E047	E0C7
46	PgUp	E049	E0C9
60	PgDn	E051	E0D1
74	End	E04F	E0CF
79	Insert	E052	E0D2
80	Delete	E053	E0D3
73	Up arrow	E048	E0C8
81	Left arrow	E04B	E0CB
82	Down arrow	E050	E0D0
83	Right arrow	E04D	E0CD

Key Position No.	Character Code	Keypad ON or OFF Make	Keypad ON or OFF Break
31	Home	E0AA,E047	E0C7
46	PgUp	E0AA,E049	E0C9
60	PgDn	E0AA,E051	E0D1
74	End	E0AA,E04F	E0CF
79	Insert	E0AA,E052	E0D2
80	Delete	E0AA,E053	E0D3
73	Up arrow	E0AA,E048	E0C8
81	Left arrow	E0AA,E04B	E0CB
82	Down arrow	E0AA,E050	E0D0
83	Right arrow	E0AA,E04D	E0CD

- Notes:
1. When left shift is pressed, E0AA is used in the shift portion as shown in Table 3B. However, shift portion is sent only once, and the key part is typematic.
 2. If right shift is pressed, E0B6 is used in Table 3B.
 3. If left and right shifts are pressed, both shift codes are used.
 4. When a non-cursor key is pressed or shift is released, E02A and/or E036 is sent before the scan code of the new key is sent.
Normally, this would be sent when the cursor is released.
The break of the cursor portion is sent when the key is released.

Table 3C: NumLock ON case

Key Position No.	Character Code	Keypad ON or OFF Make	OFF Break
31	Home	E02A,E047	E0C7
46	PgUp	E02A,E049	E0C9
60	PgDn	E02A,E051	E0D1
74	End	E02A,E04F	E0CF
79	Insert	E02A,E052	E0D2
80	Delete	E02A,E053	E0D3
73	Up arrow	E02A,E048	E0C8
81	Left arrow	E02A,E04B	E0CB
82	Down arrow	E02A,E050	E0D0
83	Right arrow	E02A,E04D	E0CD

- Notes:
1. Shift portion is sent only once, however the cursor portion is typematic.
 2. When a non-cursor key (including Shift keys) is pressed, E0AA is sent before the scan code of the new key is sent. Normally, this would be sent when the cursor keys is released. The break of the cursor portion is sent when the key is released.

Table 4: Fn Scan codes

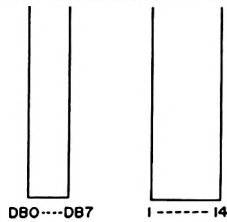
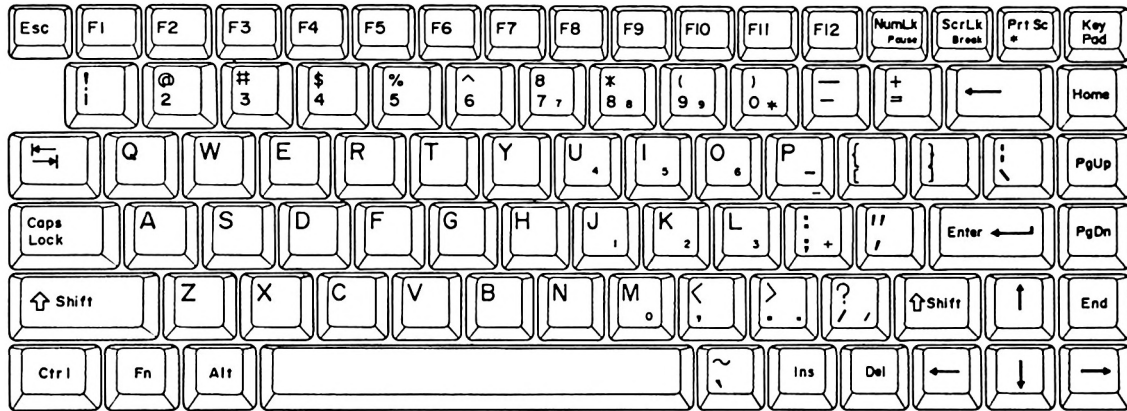
Key Position No.	Character Code	Make Code	Break Code	Comments
2	F1	71	—	not Fn+Shift, make one
3	F2	72	—	not Fn+Shift, make one
4	F3	73	—	not Fn+Shift, make one
5	F4	74	—	not Fn+Shift, make one
6	F5	75	—	not Fn+Shift, make one
7	F6	76	—	not Fn+Shift, make one
8	F7	77	—	not Fn+Shift, make one
9	F8	78	—	not Fn+Shift, make one
10	F9	79	—	not Fn+Shift, make one
11	F10	7A	—	not Fn+Shift, make one
12	F11	7B	—	not Fn+Shift, make one
13	F12	7C	—	not Fn+Shift, make one
14	NumLock	—	—	Fn+Esc pressed
17	Keypad	—	—	Toggle internal NumLock Toggle for Normal Mode and 10-key Mode

- Note: 1. Keys not shown here do not produce a scan code.

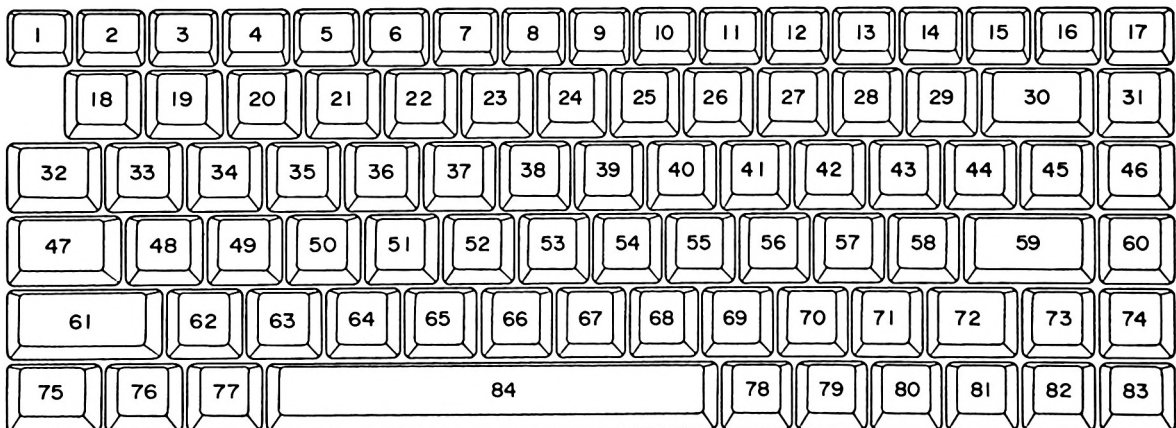
Key Matrix

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
DB0		Q	L	O	W	* ₈	S	T	R	{	}	Pg Up	NC	NC
DB1		↔	;	K		U	D	G	F	''	;	Pg Dn		
DB2			? /	< ,	A	I	X	H	C	Enter ↵	↑	End		
DB3	↑Shift	Caps Lock	> .	M	Z	J		V	Space	←	↓			
DB4	↑Shift	Ctrl	Ins	~	Fn	N	Alt	B		Del		→		
DB5		! _	P	(9	@ 2	& 7	E	Y	\$ 4	- _	←	Home		
DB6		F1) 0	F9	F2	F8	# 3	^ 6	% 5	+ =	NumLk	Prt Sc *		
DB7		Esc	F11	F10	F3	F7	F4	F6	F5	F12	ScrLk	KeyRad		

Keyboard Layout

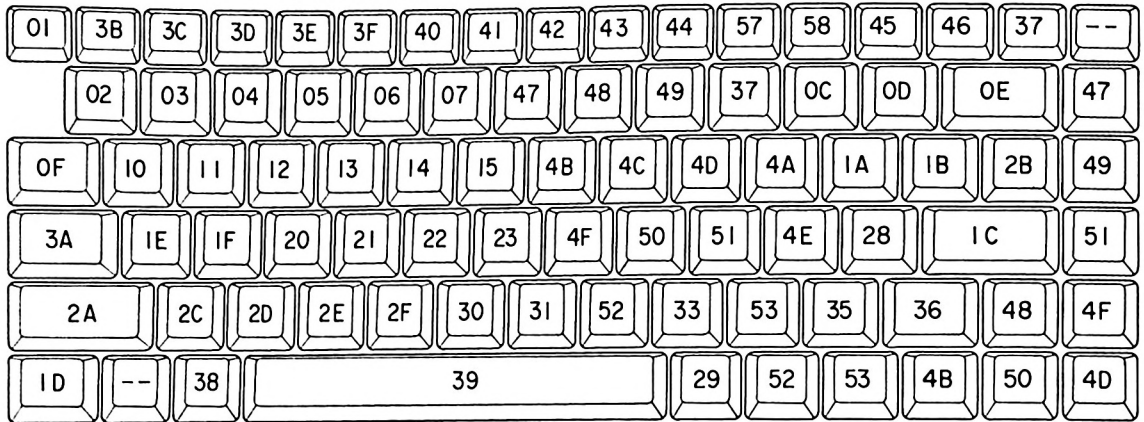


Keyboard Position Layout

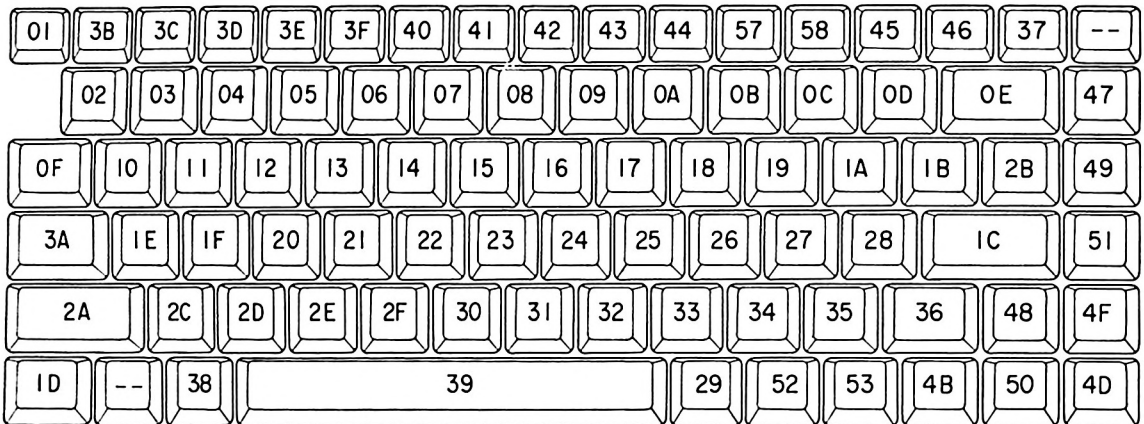


Scan Code (Make Code)

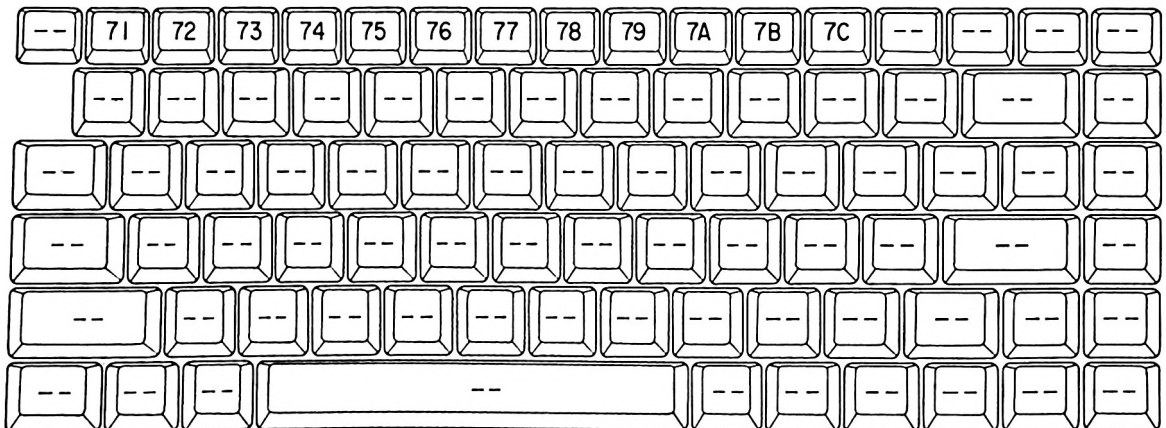
1. Normal Case



2. 10-Key Mode



3. Fn +



Floppy Disk Drive

FDD Peripheral Circuitry

The Tandy 1100FD is equipped with one 3.5-inch floppy disk drive. Figure 4-18 shows the FDD and peripheral block diagram. The Tandy 1100FD uses DA2050F, IC401 for floppy disk controller and VFO. Data transmission from the FDD is performed in the DMA mode and is controlled by MN12862, IC102.

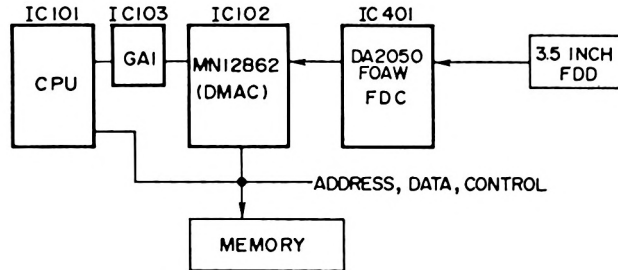


Figure 4-18 FDD and Peripheral Block Diagram

DMA Operation

A DMA request (DRQ2) is generated by the FDC (IC401). After receiving the DMA request, the DMA controller (IC102) issues a Hold request (HRQ signal) to the GA1 (IC103). The system buses are not released to the DMA controller until a Hold Acknowledge signal (HLDA signal) is returned to the DMA controller from the GA1. After the Hold Acknowledge has been received, address and control signals are generated by the DMA controller to accomplish the DMA transfer. Then DATA is transferred directly from the FDC to memory.

In advance, the segment address is sent to GA2. In the DMA cycle, GA2 encodes the DMA Acknowledge signal and outputs the address of the permitted DMA channel to the A16-A19 bus.

DMA Control

All data transmissions between the FDC and the CPU are performed in DMA mode. Figure 4-19 shows the DMA controller (in MN12862, IC102) and peripheral circuitry.

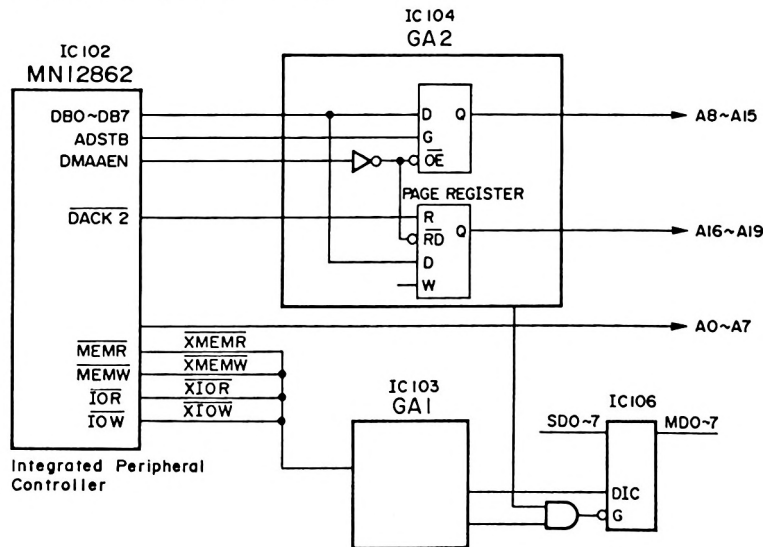


Figure 4-19 DMA Controller and Peripheral Circuitry

FDD Control

The IC 401 (DA2050F) is a one-chip Floppy Disk Controller (FDC) combined with a data separator (analog PLL), a driver/receiver for host interface, a driver/receiver for drive interface and a transfer rate select circuit.

CPU Interface

Figure 4-20 shows the CPU interface for FDC. The signals A0-A9 select which internal register to use. Active low signal $\overline{\text{SIOR}}$, ($\overline{\text{SIOW}}$) is input to allow the transfer of data from (to) the FDC to (from) the S data bus. The FDC sets the INT signal to High when the command is executed.

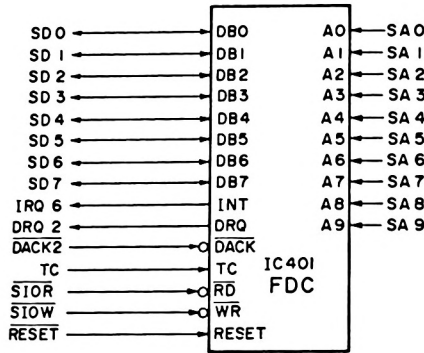


Figure 4-20 CPU Interface for FDC

FDD Interface

Figure 4-21 shows the FDD interface circuitry. The signal for FDD, active low $\overline{\text{DRIVESEL}}$ and $\overline{\text{MOTORENA}}$, are latched in FDC. These are set by the I/O system command. The FDD control signals for the input system are pulled up by the resistors.

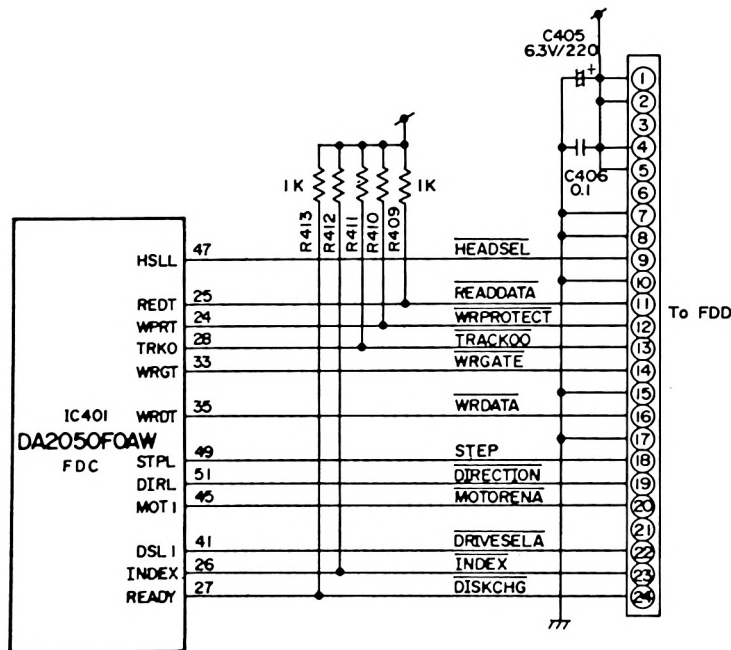


Figure 4-21 FDD Interface Circuitry

VFO (DATA SEPARATOR FOR FDD)

The VFO removes the bit phase shift origination in variations in disk rotation speed or peak shifts from disk drive read data to generate the data window and reproduces read data pulse signals for output to the FDC.

Timing Chart

(1) Select Loop Gain

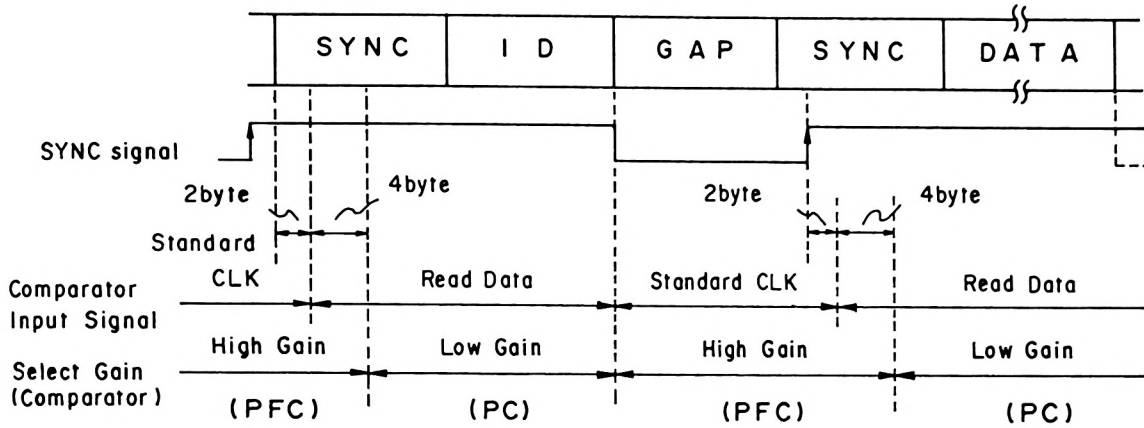
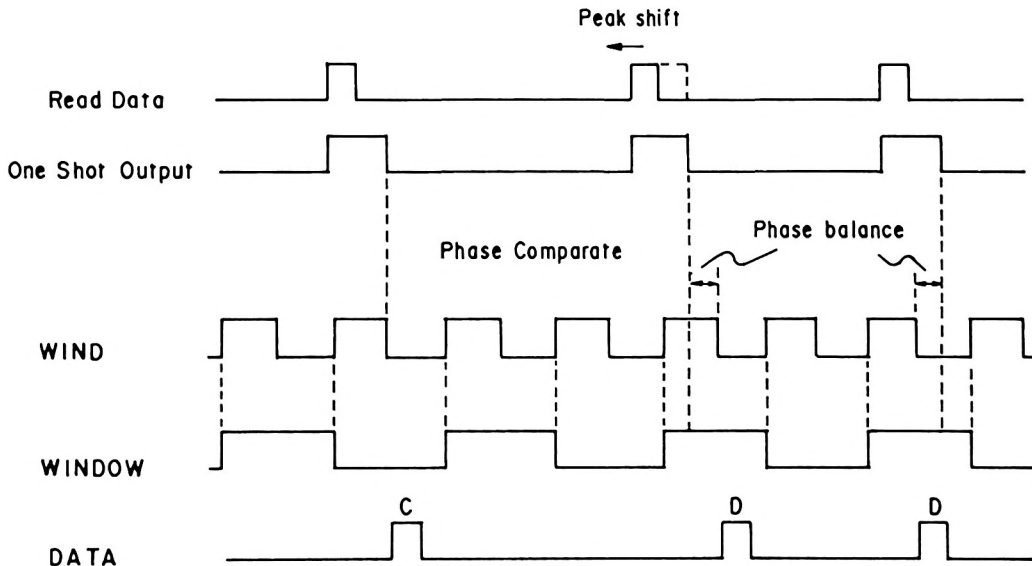


Figure 4-22 Select Loop Gain Timing Chart

A comparator signal is input and PFC is changed from standard CLK to Read Data if 2 bytes of 00h is detected continuously after SYNC goes high. Then if 4 bytes of 00h is detected continuously again, Loop filter is changed to Low gain, Comparator is changed to phase Comparator PC and read operation. After that, if SYNC is low, the same operation is repeated again.

(2) Data and Window (At selecting PC)



WIND is VCO output wich is twice WINDOW.

Figure 4-23 DATA and Window

Printer Interface

Figure 4-24 shows the printer interface circuit. The data or command to the printer is loaded to an 8-bit latched output port, and active low "STROBE" signal is activated by writing data to the printer.

The printer interface program then reads the status pins of the printer port to see if the next character can be sent. If the printer is ready, the program activates IRQ7, indicating to the system program that the printer is not busy.

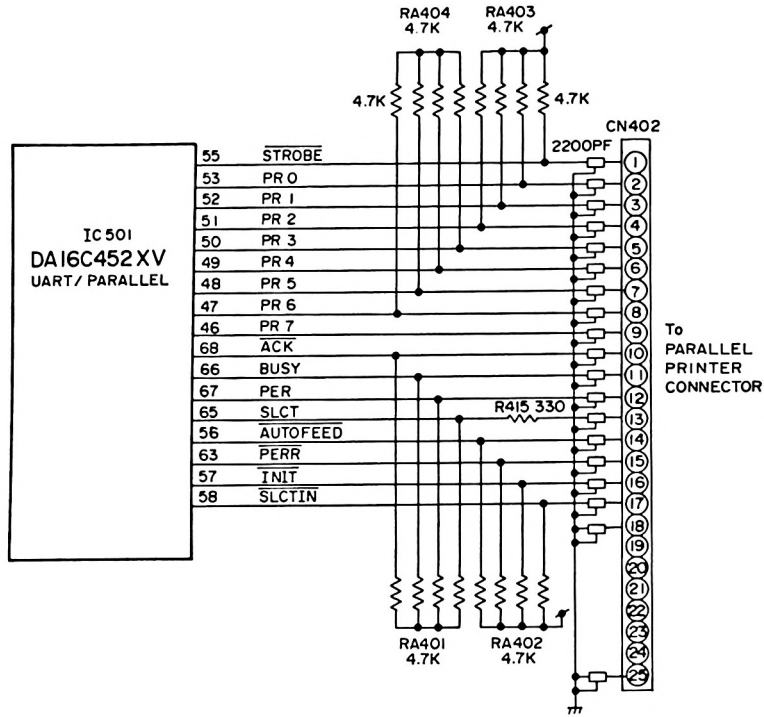


Figure 4-24 Printer Interface Circuitry

Figure 4-25 shows the timing diagram between the CPU and the printer.

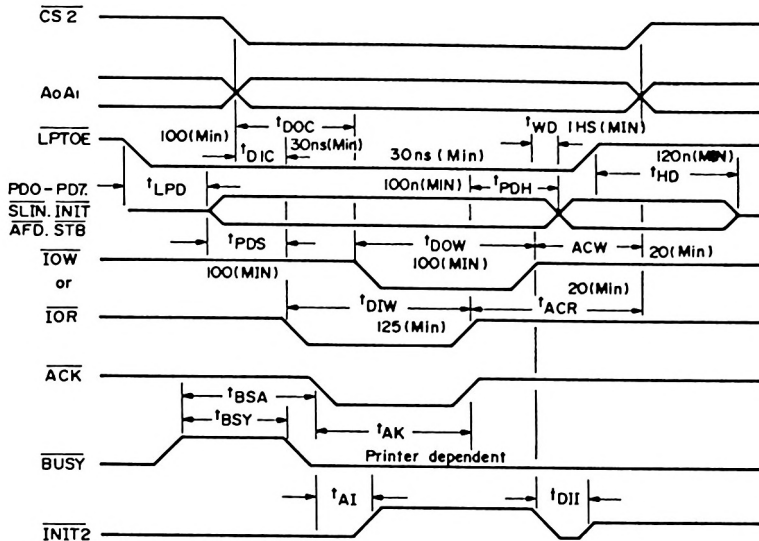


Figure 4-25 Timing Chart between CPU and Printer

LCD Controller

CPU-LCDC Interface

Figure 4-26 shows CPU - LCDC interface. Data Bus (D0-D7), COMMAND (\overline{SIOW} , \overline{SIOR} , \overline{SMEMW} , \overline{SMEMR}), AENBRD (Address enable), $\overline{IOCHRDY}$ (Memory request), CPUCLK, VDEC (VRAM chip select) and Address Bus (SA0-SA15) serve as the interface between the CPU and the LCDC. An Address decoder is included in the LCDC (IC301).

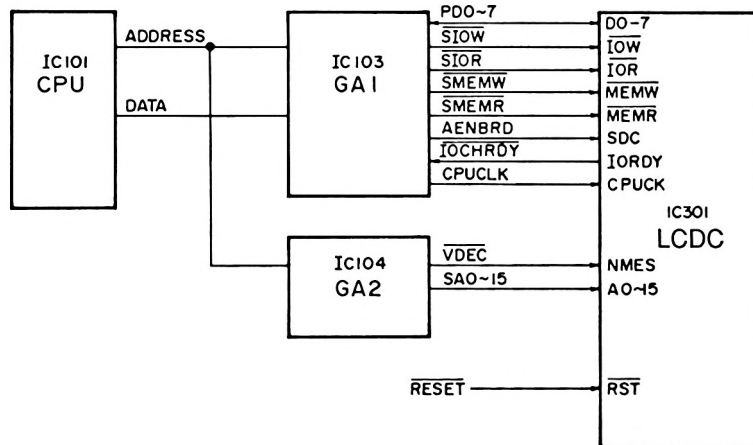


Figure 4-26 CPU-LCDC Interface

VRAM-LCDC Interface

The Tandy 1100FD uses two 8K-byte static RAMs (total 16K-byte) for the VIDEO RAM. This memory contains 640 x 200 dots of data for graphic display. The CPU can access it anytime without display flicker. The VIDEO RAM can be accessed completely in the same way as accessing normal memory RAM from the CPU. WRITE and READ functions are freely executed without checking the status of the display control device. This controller will be selected by active low \overline{VDEC} (VRAM chip select signal) and active low \overline{SMEMW} or \overline{SMEMR} . Figure 4-27 shows the VRAM-LCDC interface.

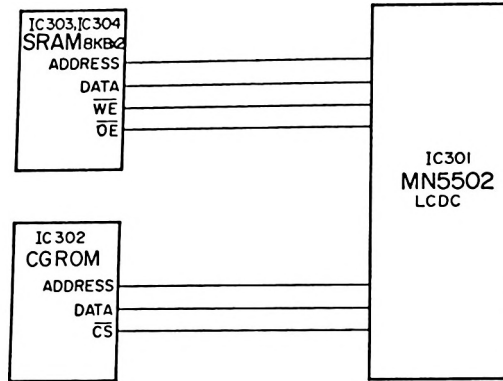


Figure 4-27 VRAM-LCDC Interface

LCD Unit Interface

The interface signal between the LCD controller and the LCD unit is shown in figure 4-28.

Signal	Function
STF/V	Start signal of each display cycle
LOAD	Signal for latching 1 line shift register
CPX	The shift clock signal of display data
DU0-3	The display data (DU0-DU3) is input at the falling edge of this signal.
RF1, 2	LCD contrast control

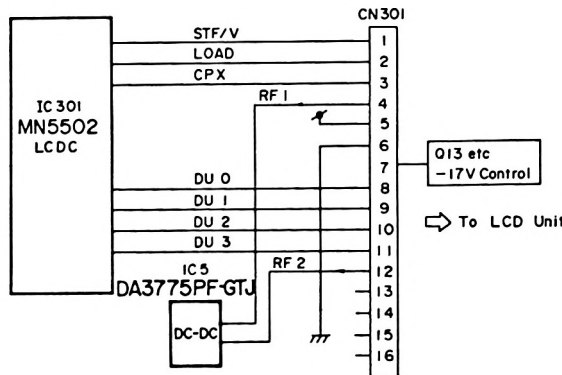


Figure 4-28 Interface Signal between LCDC and LCD Unit

Serial Interface

The Tandy 1100FD is equipped with two serial interfaces. The RS-232C interface and MODEM connector interface are assigned to COM1 and COM2 (software selectable). Figure 4-29 shows a block diagram of the interface.

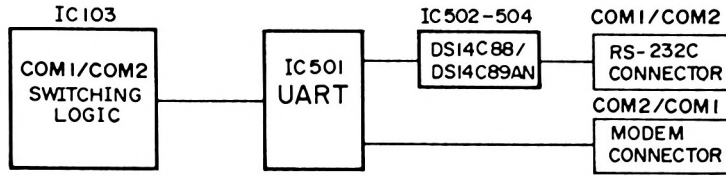


Figure 4-29 Serial Interface Block Diagram

Serial data for the Tandy 1100FD is controlled by the UART (DA16C452, IC501). The UART performs serial-to-parallel conversion on data characters received from the RS-232C or MODEM and parallel to serial conversion on data characters received from the CPU. The CPU can read the complete status of the UART at any time during the functional operation. The status information reported includes the type and condition of the transfer operations being performed by the UART as well as any error conditions (parity, overrun, framing or break interrupt).

RTC

The RTC (Real Time Clock) RF5C15, (IC601) has an internal counter for time (hours, min. and sec.) and date (100 years, leap years, months, dates and days-of-the-week). Time can be written to or read from the RTC in the same way as writing to or reading from the RAM. Time counting function is maintained by the back-up battery even when the system is turned off.

(The RTC has an alarm function and the CPU can be notified by IRQ2.)

Figure 4-30 shows the RTC and peripheral circuitry.

The following external parts are required for constructing the oscillator circuit.

1. A quartz oscillator with a frequency of 32.768 kHz
2. Two capacitors (including one trimmer capacitor)

The accuracy of the oscillation frequency can be measured by using a standard clock signal to be output from terminal 3 (CKOUT, TP1). In order to read the oscillation frequency, connect the frequency counter to the terminal TP1.

(The measuring probes of a frequency counter or oscilloscope should not be connected directly to the OSCIN (Pin 16) or OSCOUT (Pin 17) terminal, since the capacity of the probes alters the oscillation conditions and makes correct measurement impossible.)

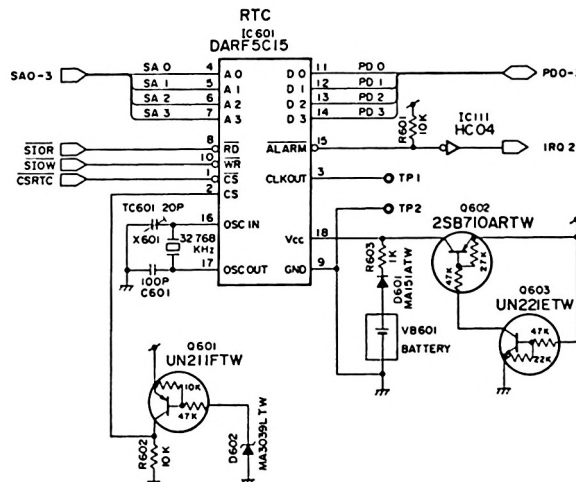


Figure 4-30 RTC and Peripheral Circuitry

Beeper Circuit

The system has a 21/32 inches (17 mm) piezo beeper. The beeper control circuit is on the Main PCB. The control circuit allows the beeper to be driven by four different methods.

1. Direct program control with an I/O address, 61H bit 1, can be toggled to generate a tone pulse.
2. Output from channel 2 of the timer counter can be programmed to generate a tone pulse.
3. TMRCLK clock input to timer counter can be modulated with I/O address, 61H bit 0.
4. SPKR signal to reflect the line status on the MODEM card generates a tone pulse.

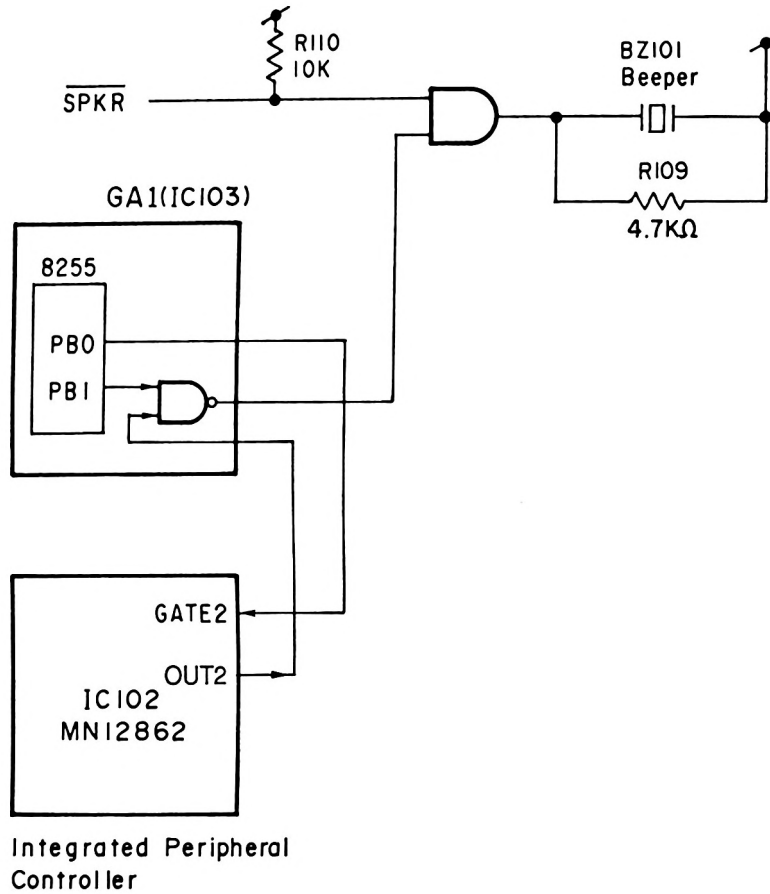


Figure 4-31 Beeper Block Diagram

Power Supply

The system DC power supply has an approximately 4.3 W, 4 voltage-level regulator. It is integrated into the system unit and supplies power for the system unit and its options.

The supply provides 370 mA of +5 Vdc, 60 mA of +12 Vdc, 40 mA of -12 Vdc and 10 mA of -17 Vdc.

The system unit takes approximately 270 mA of +5 Vdc, thus it allows approximately 100 mA of +5 Vdc for the MODEM slot. The +12 Vdc and -12 Vdc are used for powering the Electric Industries Association (EIA) drivers for the communications on the main PCB. The -17 Vdc level is used for LCD bias.

Input Requirements

The normal power requirements are listed below.

Input Voltage

Normal input: 9.5 Vdc
Minimum input: 9.03 Vdc
Maximum input: 9.98 Vdc

Current: 860 mA at 9.5 Vdc

Output

Voltage (V)	Max. current (mA)	Regulation
+5	370	±5%
+12	60	±10%
-12	40	±10%
-17	10	Changeable

Power Source

Main Battery: +6 V, 1800 mAh, sealed Lead-acid battery.

Backup Battery: A lithium battery of 3 V, 1000 mAh to hold the time and date of RTC.

Battery Voltage Warning

The first warning is a one-second flashing of the LED. The user is instructed to charge the battery voltage to 5.9-6.0 V. After the first warning, the system can be used for about 20 minutes with FDD 10% duty. The second warning is a 250 msec flashing of the Low Battery LED. The user is instructed to shut down the system at a battery voltage of 5.1 V-5.6 V. User should close current task file. About 5 minutes after the second warning, the system shuts down and clears all RAM data.

Power Save Mode

When nothing is input for pre-set time (Software selectable), the system automatically turns to standby mode. Pressing any key brings the computer out of STANDBY MODE.

The program being used when STANDBY MODE is engaged is maintained intact.

1. The time of auto standby mode can be set from 0 to 255 minutes with the "POWER11.COM" program.
2. In standby mode, memory contents will be maintained by the main battery for 5 hours at the condition of full charge. When the main battery is discharged, memory contents will be lost. The Low Battery warning is also displayed in standby mode.
3. Input power rating (AC Adapter) Voltage 9.5 V, 2100 mA.
4. Current consumption (typical data).

	AC Operation	Battery Operation
Normal use mode:	250 mA	330 mA
FDD Seek:	600 mA	830 mA
FDD Motor ON:	730 mA	1000 mA
Standby Mode:	210 mA	285 mA

AC Adapter Specifications

1. Rating: Input: AC 120 V, 60 Hz, 25 W
 Output: DC 9.5 V, 2100 mA
2. Electrical Characteristics:

Operating Temperature Range	50°F~104°F (10°C~40°C)
Rated Input Voltage	AC 120 V, 60 Hz
Power Consumption	25 W maximum
Rated Load Current	2100 mA DC maximum
Output Voltage	DC 9.5 V ±5%
Ripple Voltage	100 mV (p-p)
Maximum Case Temperature	Applied to UL 1310 Standard
Allowable Variation of Input Voltage	AC 85 ~135 V
Dielectric Withstanding	DC 1000 V, 1 minute
Insulation Resistance	more than 20 Mohms (DC 500 V)

Pin Assignments of Connectors

CN401, FDD Connector

Pin No.	Signal Name	I/O	Description
1	+5 Vdc	—	—
2	+5 Vdc	—	—
3	N.C.	—	—
4	+5 Vdc	—	—
5	+5 Vdc	—	—
6	N.C.	—	—
7	GND	—	—
8	GND	—	—
9	<u>HEADSEL</u>	O	This signal is used for Head Selection. "Low" level: Head 1, "High" level: Head 0
10	<u>GND</u>	—	—
11	<u>READDATA</u>	I	This signal is the data of the inversion of the disk magnetization read out by the head.
12	<u>WPROTECT</u>	I	This signal indicates that a write-protected disk is loaded.
13	<u>TRACK00</u>	I	This signal indicates that the head is in the track 00 position (outermost track).
14	<u>WRGATE</u>	O	Writing in the disk is possible by this signal.
15	<u>GND</u>	—	—
16	<u>WRDATA</u>	O	This signal provides data to be written on the disk.
17	<u>GND</u>	—	—
18	<u>STEP</u>	O	This signal causes the R/W Heads to move.
19	<u>DIRECTION</u>	O	This signal determines the direction of R/W Heads movement. "High" level: Out (toward Track 00) "Low" level: In (toward Track 79)
20	<u>MOTORENA</u>	O	The motor starts when this signal becomes "Low".
21	<u>N.C.</u>	—	—
22	<u>DRIVESELA</u>	O	This signal selects Drive A.
23	<u>INDEX</u>	I	This signal is used for indicating the reference position of a track.
24	<u>DISKCHG</u>	I	This indicates that the disk is unloaded.

Pin No.	Signal Name	I/O	Description
1	$\overline{\text{STROBE}}$	O	Line Printer Strobe: This I/O line provides communication between the VL16C452 and the line printer. When it is active low, it provides the line printer with a signal to latch the data currently on the parallel port.
2	PRD0	O	Parallel Data Bits (0-7): These eight lines provide a byte-wide input or output port to the system.
3	PRD1	O	
4	PRD2	O	
5	PRD3	O	
6	PRD4	O	
7	PRD5	O	
8	PRD6	O	
9	$\overline{\text{PRD7}}$	O	
10	$\overline{\text{ACK}}$	I	Line Printer Acknowledge: This input goes low to indicate a successful data transfer.
11	BUSY	I	Line printer Busy: This is an input line from the line printer that goes high when the line printer has a local operation in progress.
12	PER	I	Line Printer Paper Empty: This is an input line from the line printer that goes high when the line printer is out of paper.
13	SLCT	I	Line Printer Selected: This is an input line from the line printer that goes high when the line printer has been selected.
14	$\overline{\text{AUTOFEED}}$	O	Line Printer Autofeed: This I/O line provides the line printer with an active low signal when continuous paper is to be autofed to the printer.
15	$\overline{\text{PERR}}$	I	Line Printer Error: This is an input line from the line printer. The line printer reports an error by holding this line low during the error condition. This causes IRQ to be asserted high.
16	$\overline{\text{INIT}}$	O	Line Printer Initialize: This I/O provides the line printer with a signal that allows the line printer initialization routine to be started.
17	$\overline{\text{SLCTIN}}$	O	Line Printer Selected: This I/O line selects the printer when it is active low.
18	N.C.	—	—
19	N.C.	—	—
20	N.C.	—	—
21	N.C.	—	—
22	N.C.	—	—
23	N.C.	—	—
24	N.C.	—	—
25	N.C.	—	—

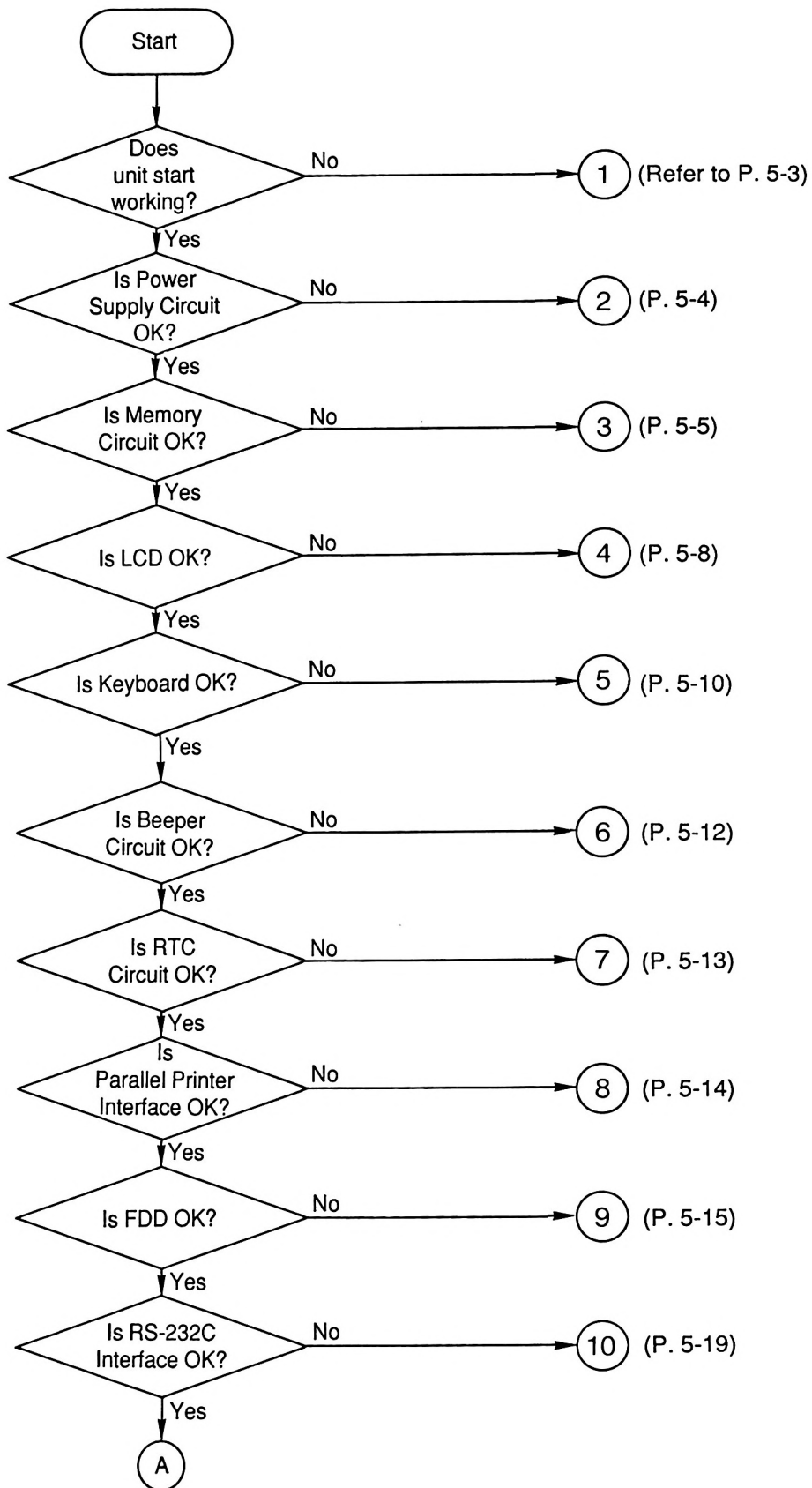
CN801, MODEM Interface

Pin No.	Signal Name	I/O	Description
1	CTS	I	Clear to Send
2	GND	—	—
3	DSR	I	Data Set Ready
4	+5 Vdc	—	100 mA max.
5	RSLD	I	Data Carrier Detect
6	MSTBY	O	MODEM Standby (Not used)
7	RI	I	Ring Indicator
8	RXD	I	Receive Data
9	SPKR	I	Acoustic Sound
10	RTS	O	Request to Send
11	DTR	O	Data Terminal Ready
12	SOUT	O	Transmit Data
13	RST	O	Reset
14	GND	—	—
15	+12 Vdc	—	50 mA max.
16	GND	—	—
17	-12 Vdc	—	30 mA max.
18	GND	—	—

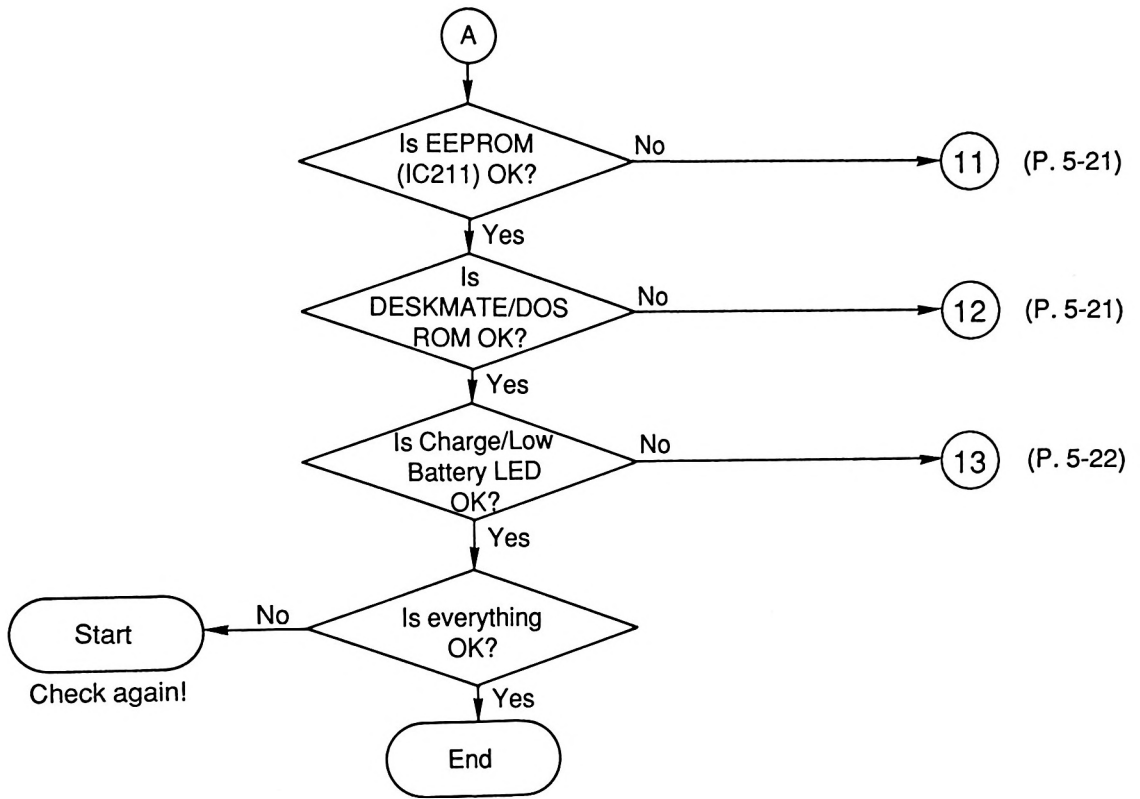
CN301, LCD Interface

Pin No.	Signal Name	I/O	Description
1	STF/V	O	Start signal for each display cycle
2	LOAD	O	Signal for latching 1 line shift register
3	CPX	O	Shift clock signal of display data
4	Rf1	I	LCD contrast control
5	+5 Vdc	—	—
6	GND	—	—
7	Vlcd	—	—
8	DU0	O	Data input signal for displaying
9	DU1	O	Data input signal for displaying
10	DU2	O	Data input signal for displaying
11	DU3	O	Data input signal for displaying
12	Rf2	I	LCD contrast control
13	N.C.	—	—
14	GND	—	—
15	N.C.	—	—
16	N.C.	—	—

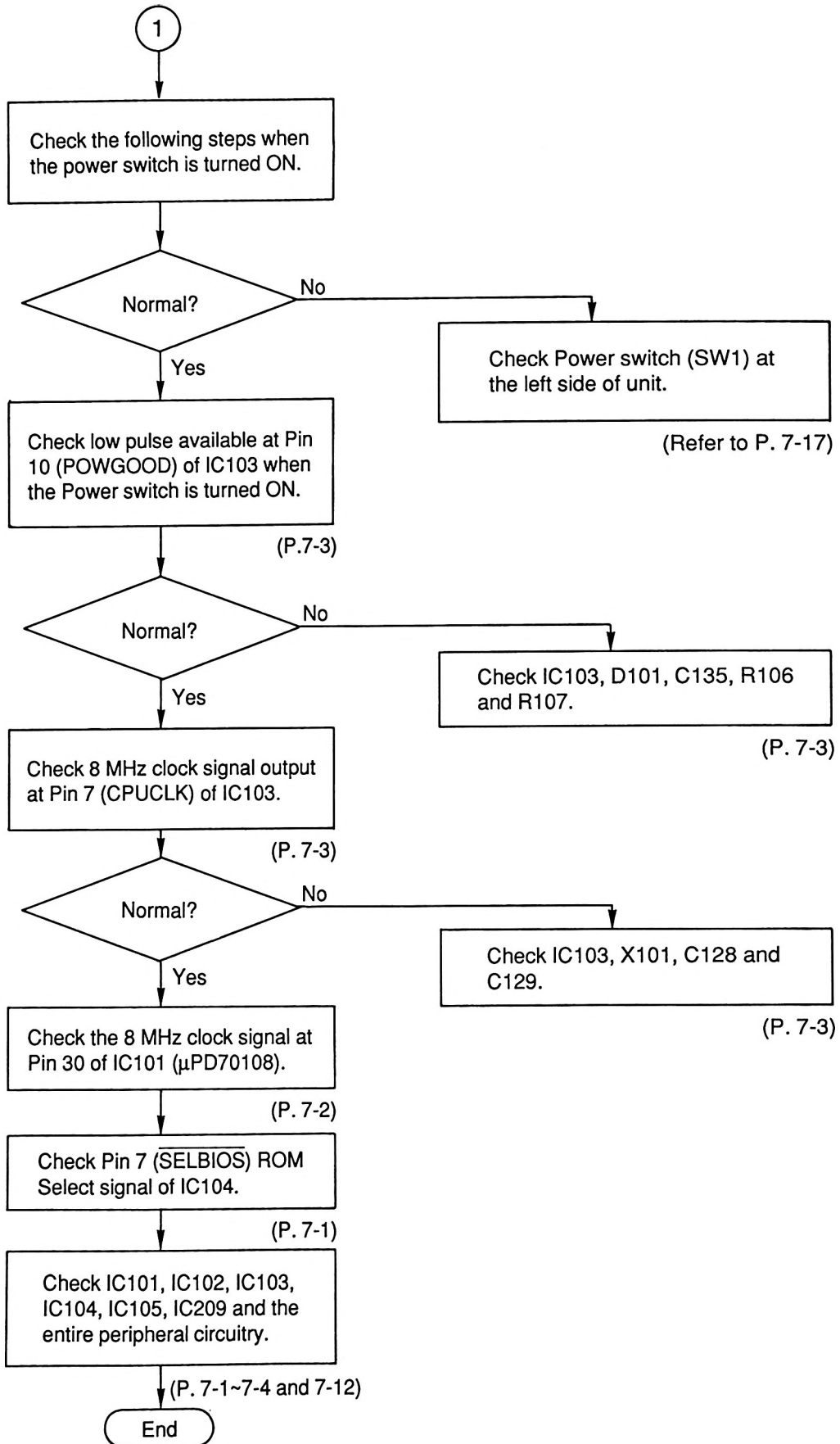
PART V. TROUBLESHOOTING



(Refer to next page)

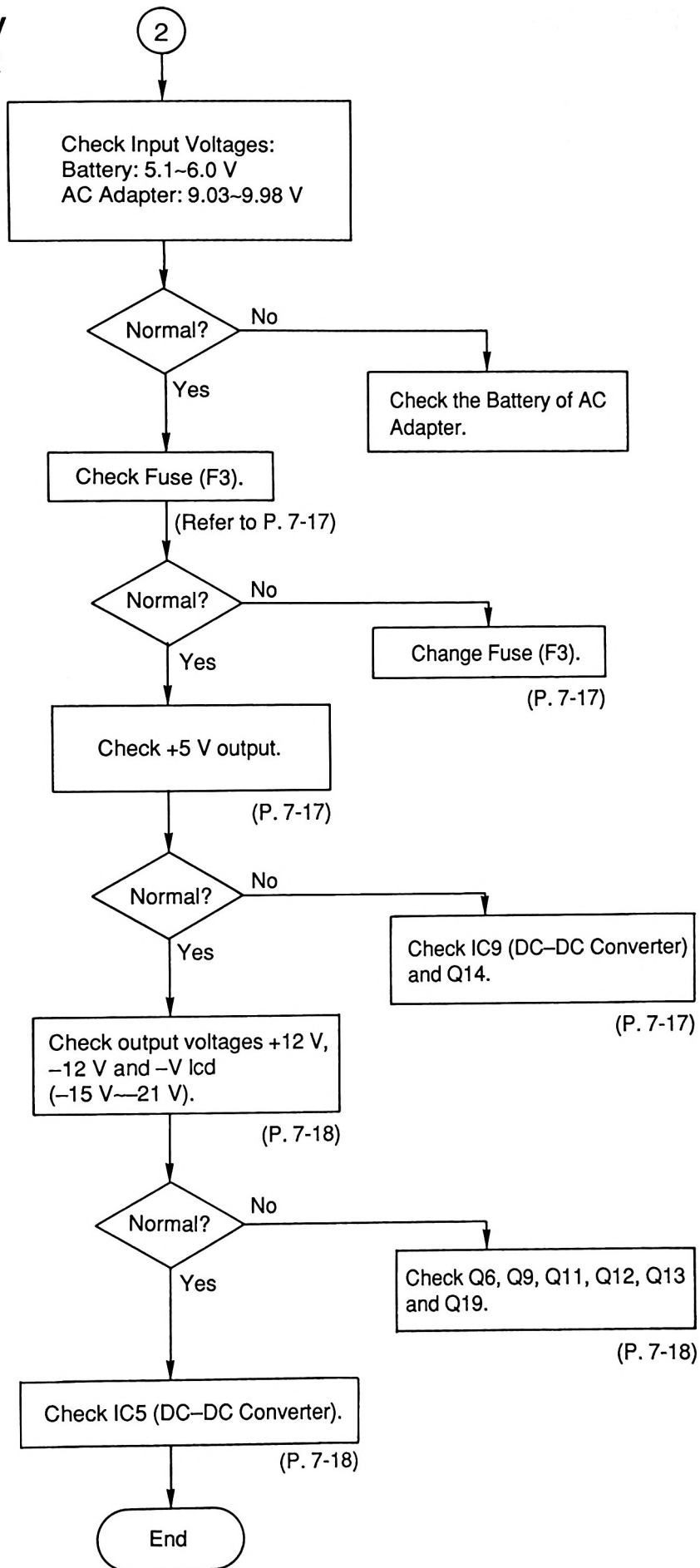


① Will Not Start Working

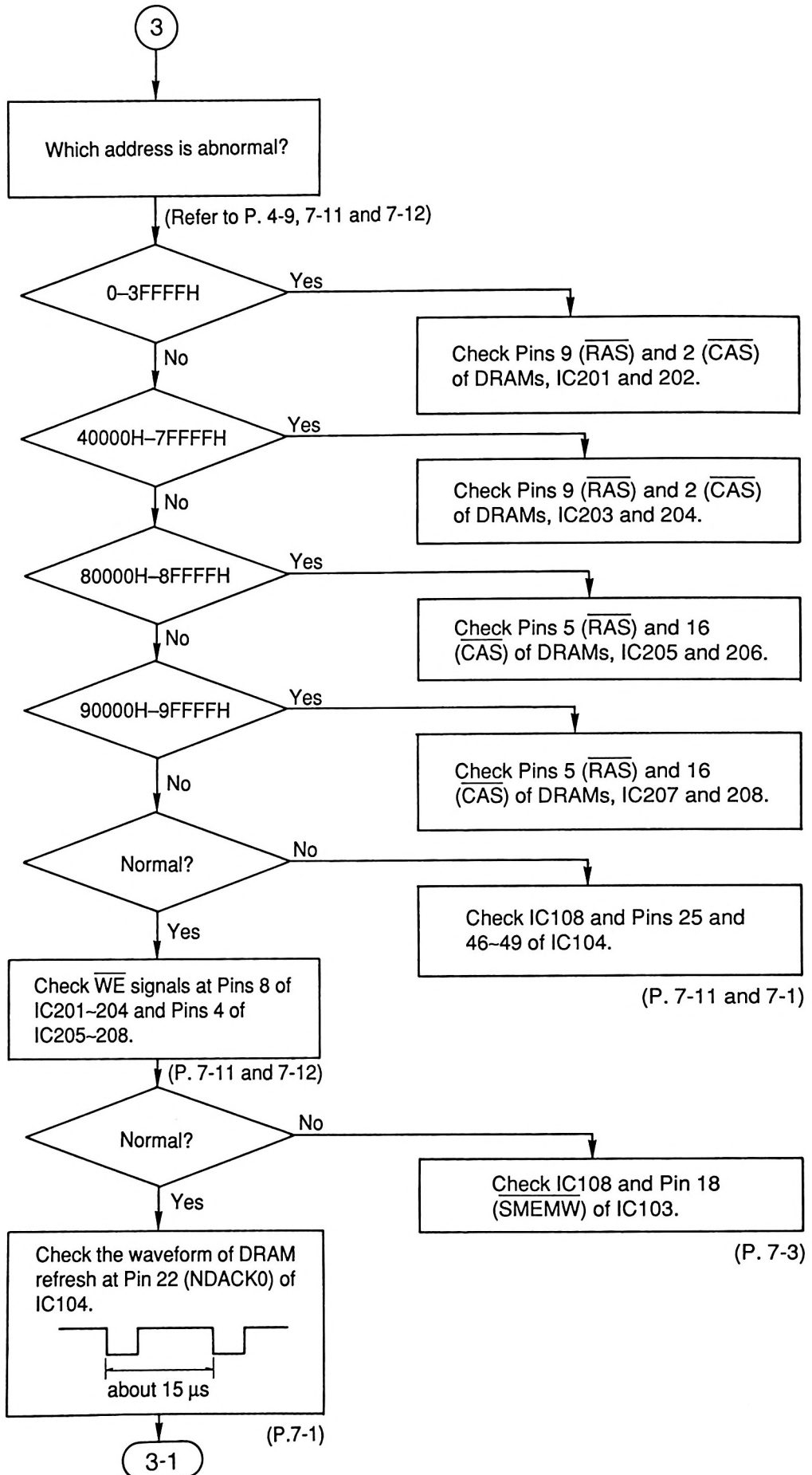


●If you need to replace defective BIOS ROM (IC209) chip, please peel off the original copyright label from the chip, and put it on the new chip.

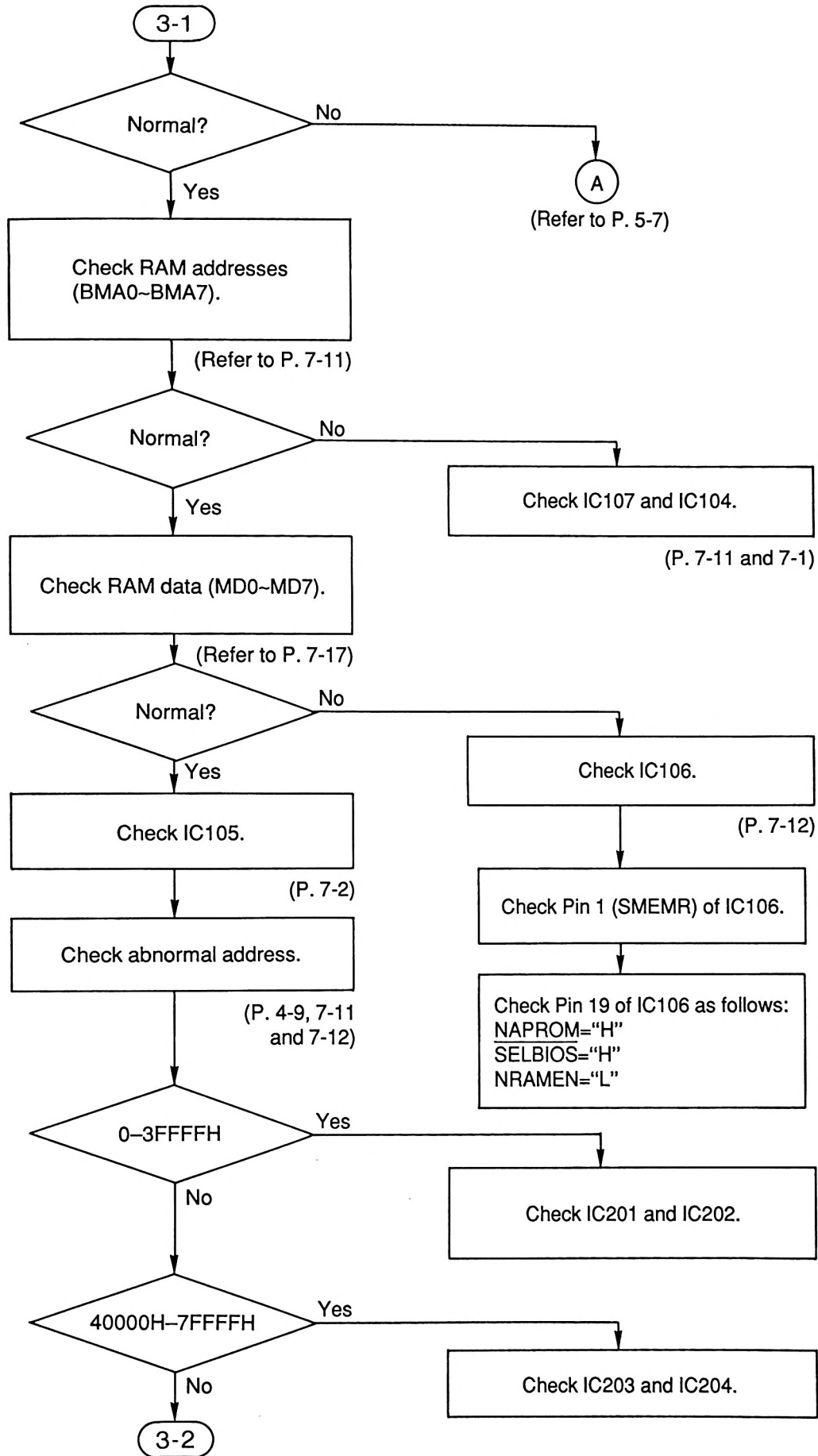
② Power Supply
Circuit Check



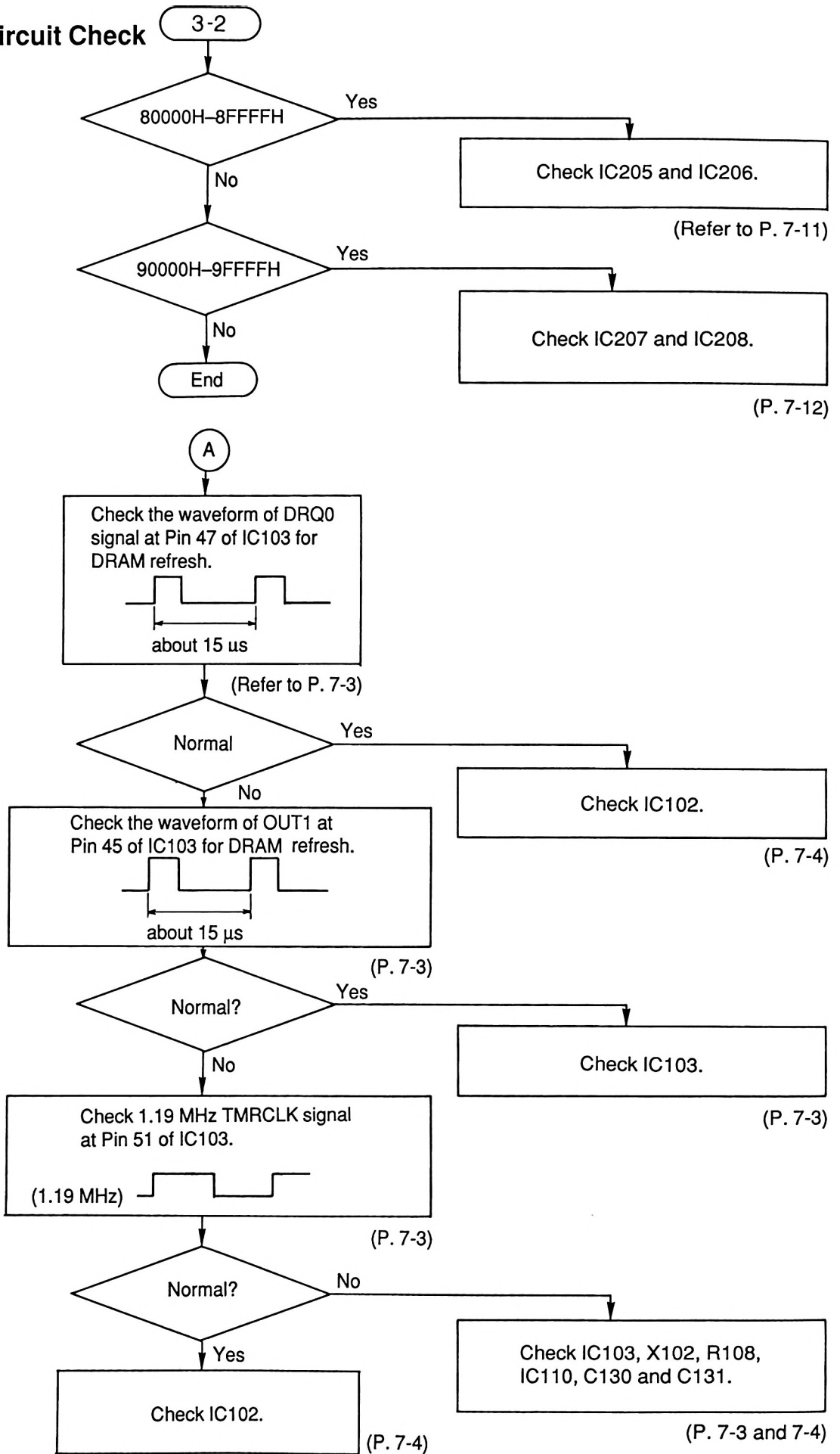
③ Memory Circuit Check



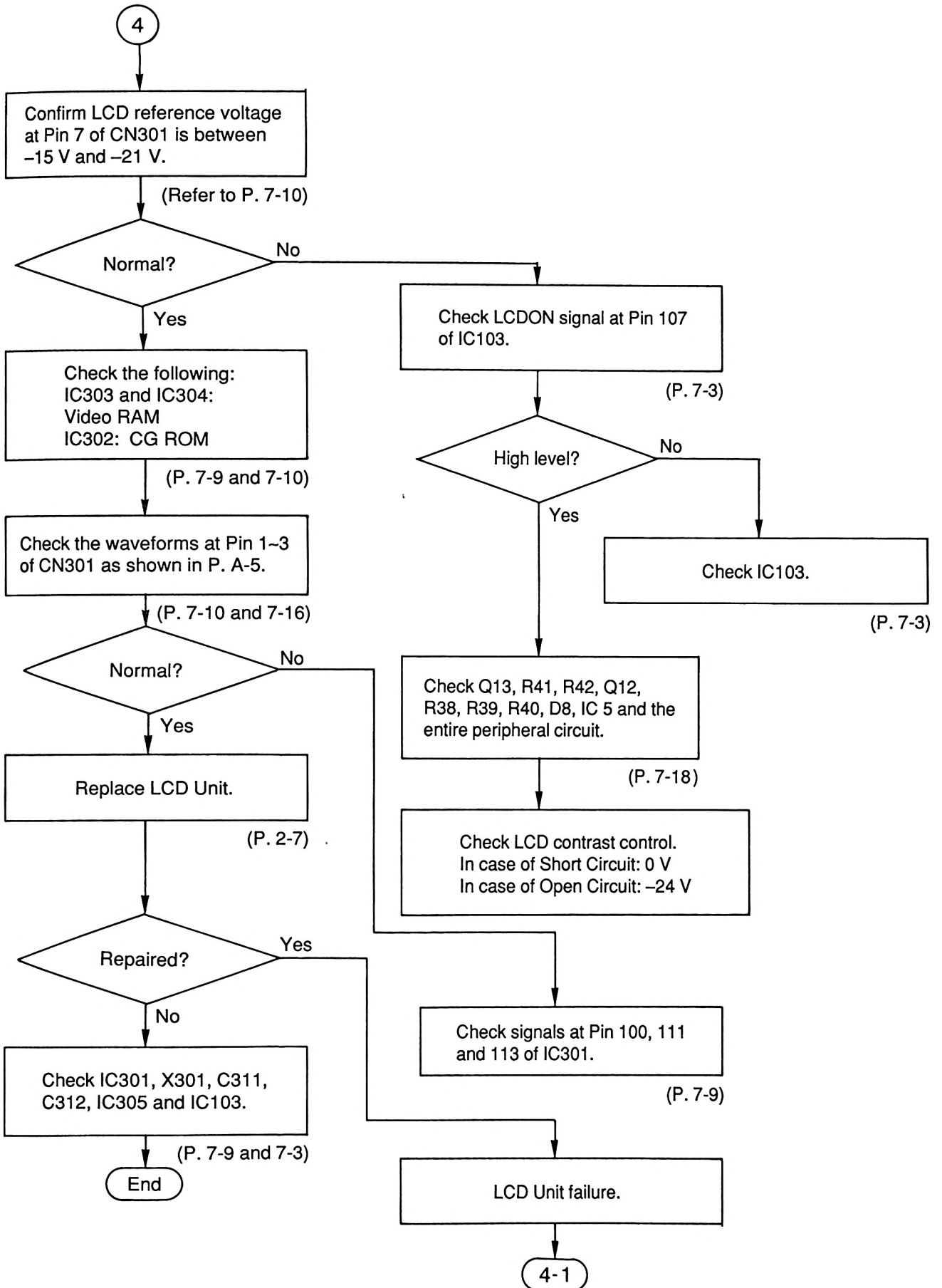
Memory Circuit Check



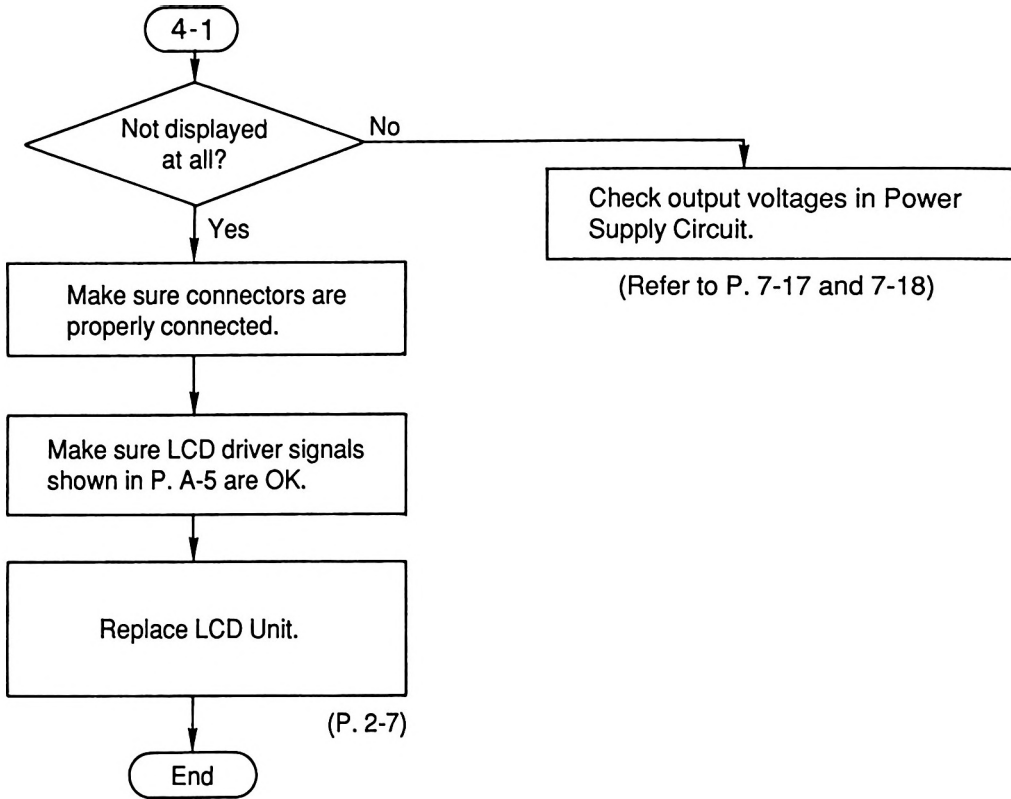
Memory Circuit Check



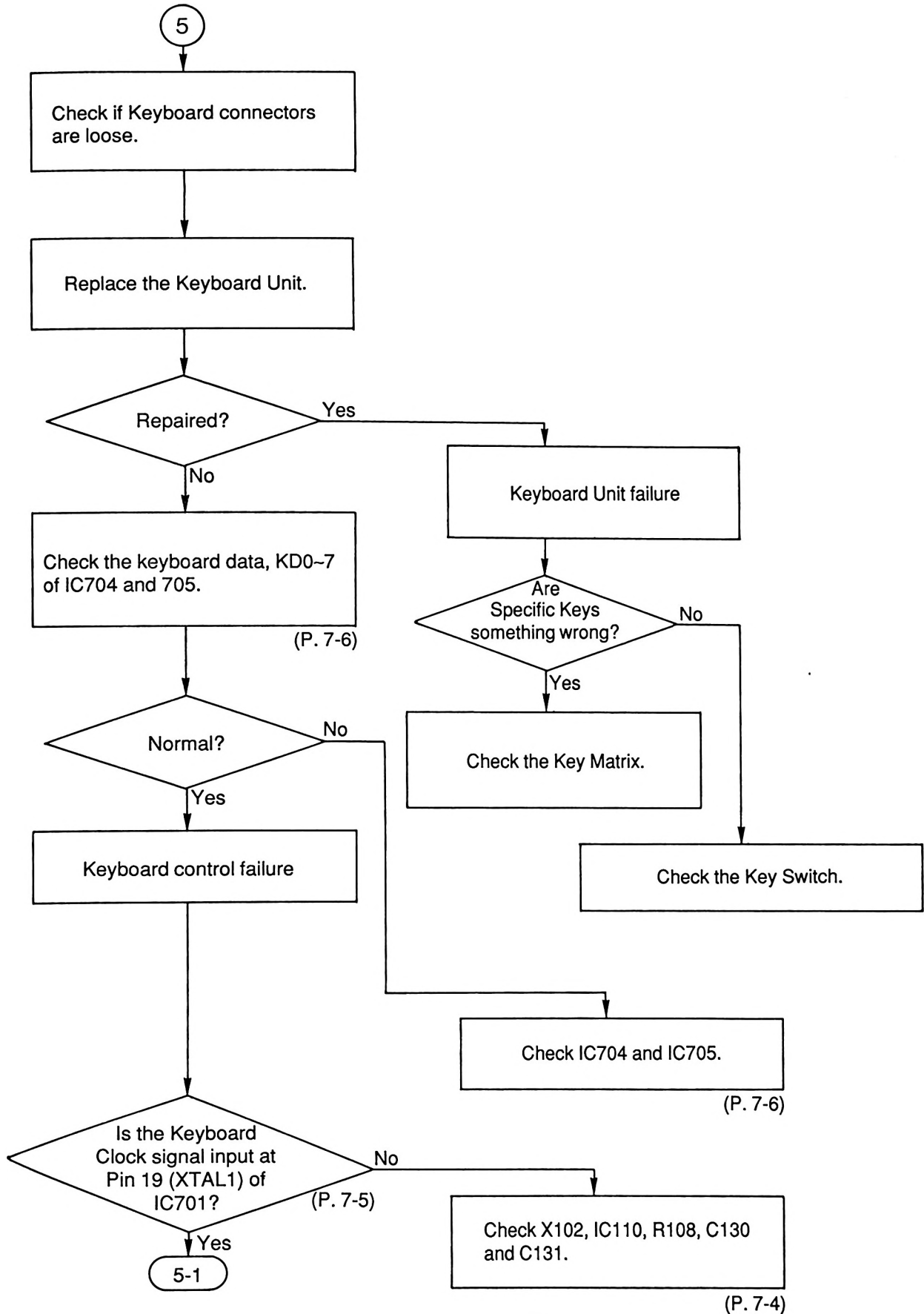
④ LCD Check



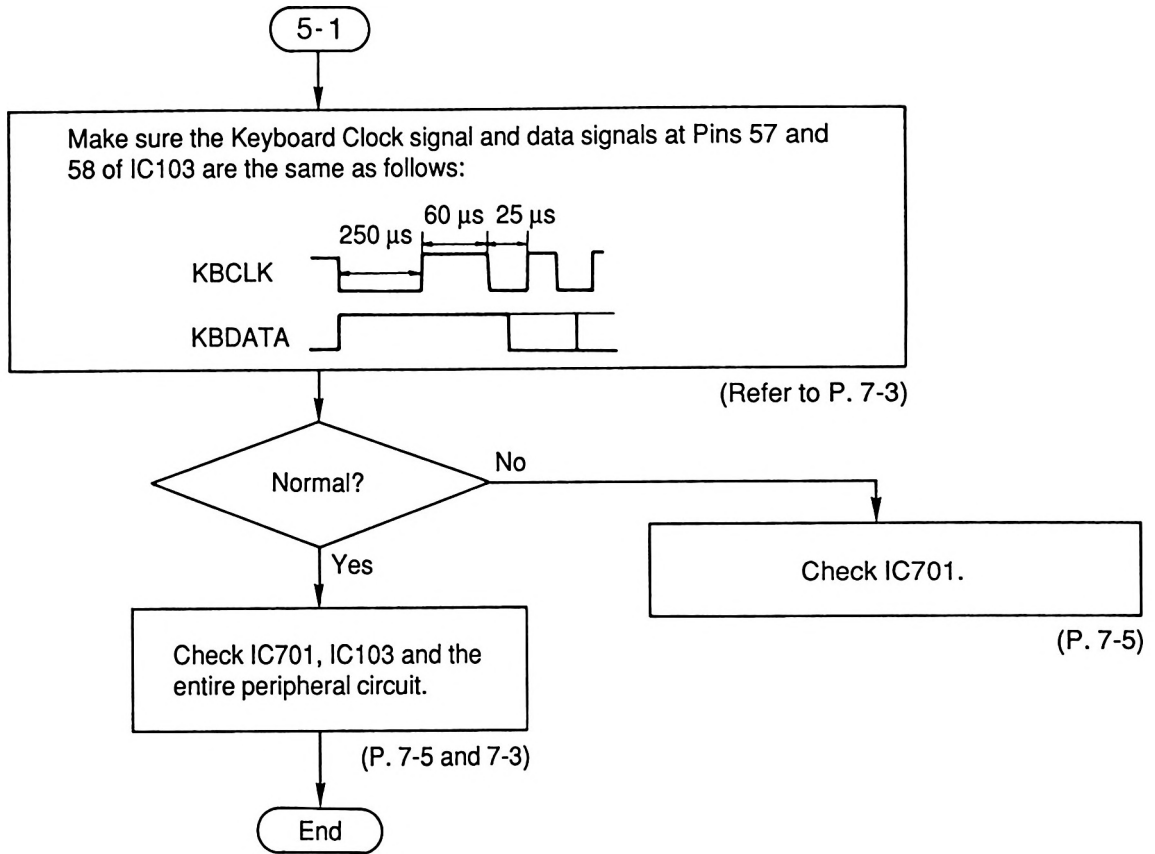
LCD Check



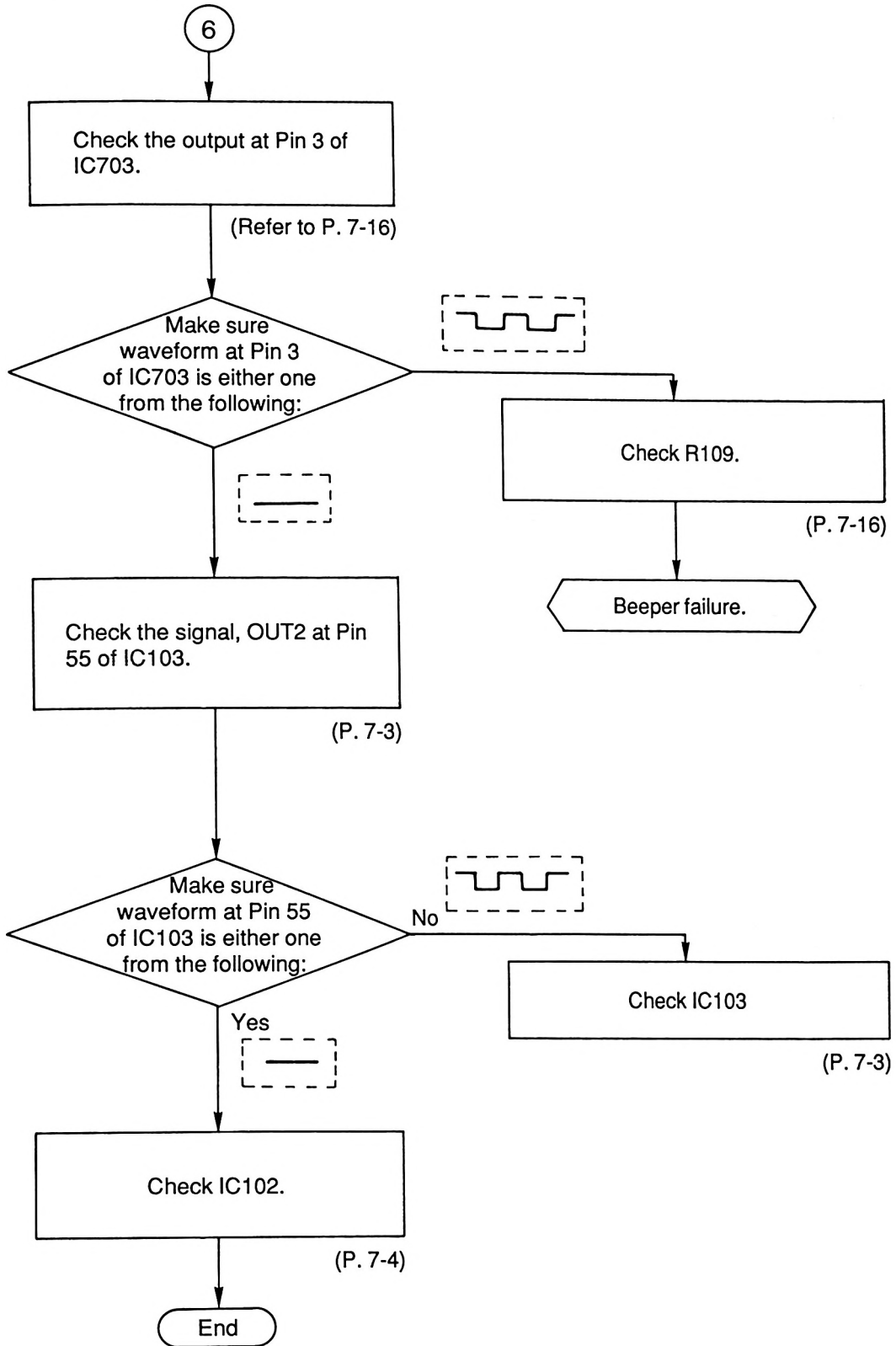
⑤ Keyboard Check



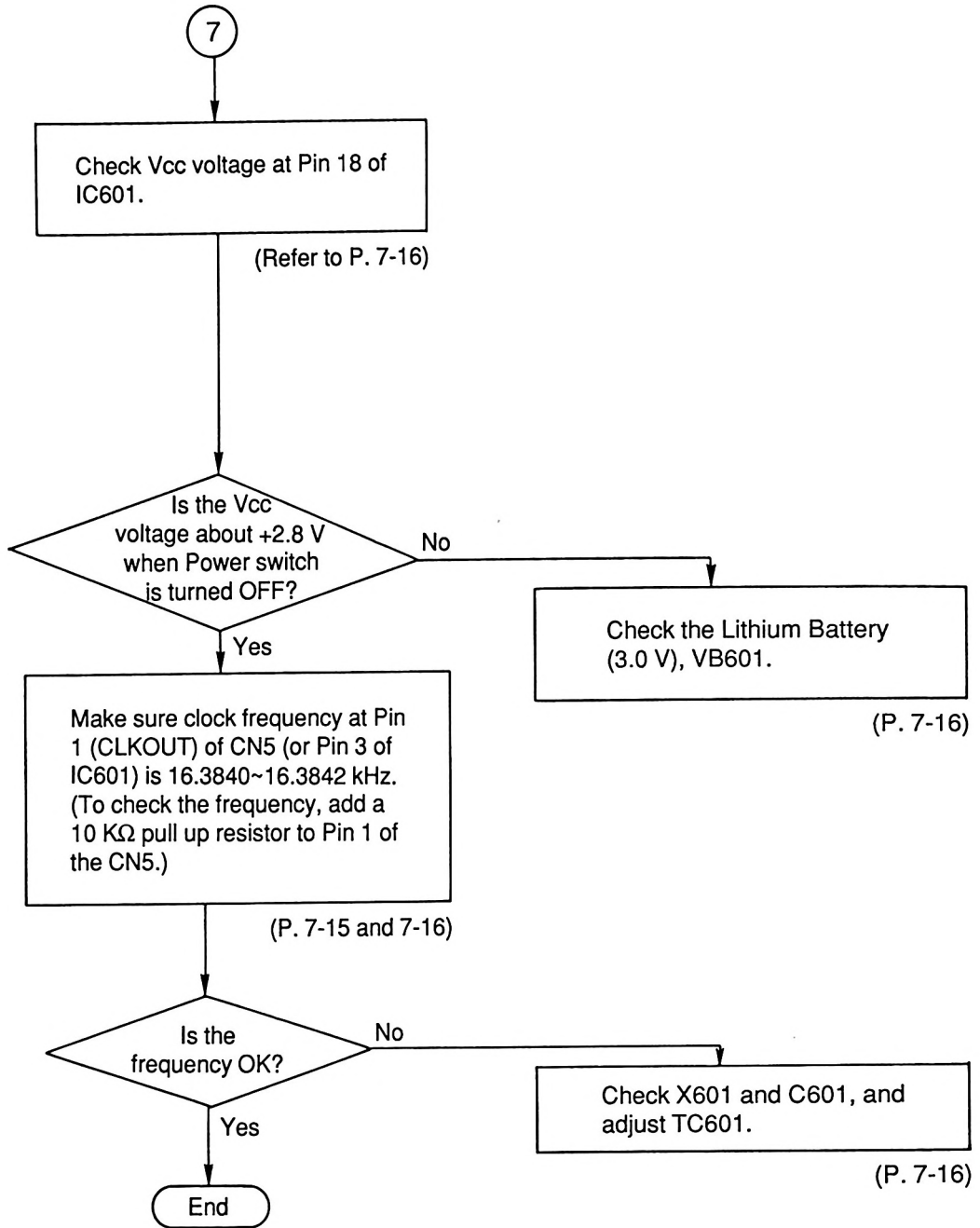
Keyboard Check



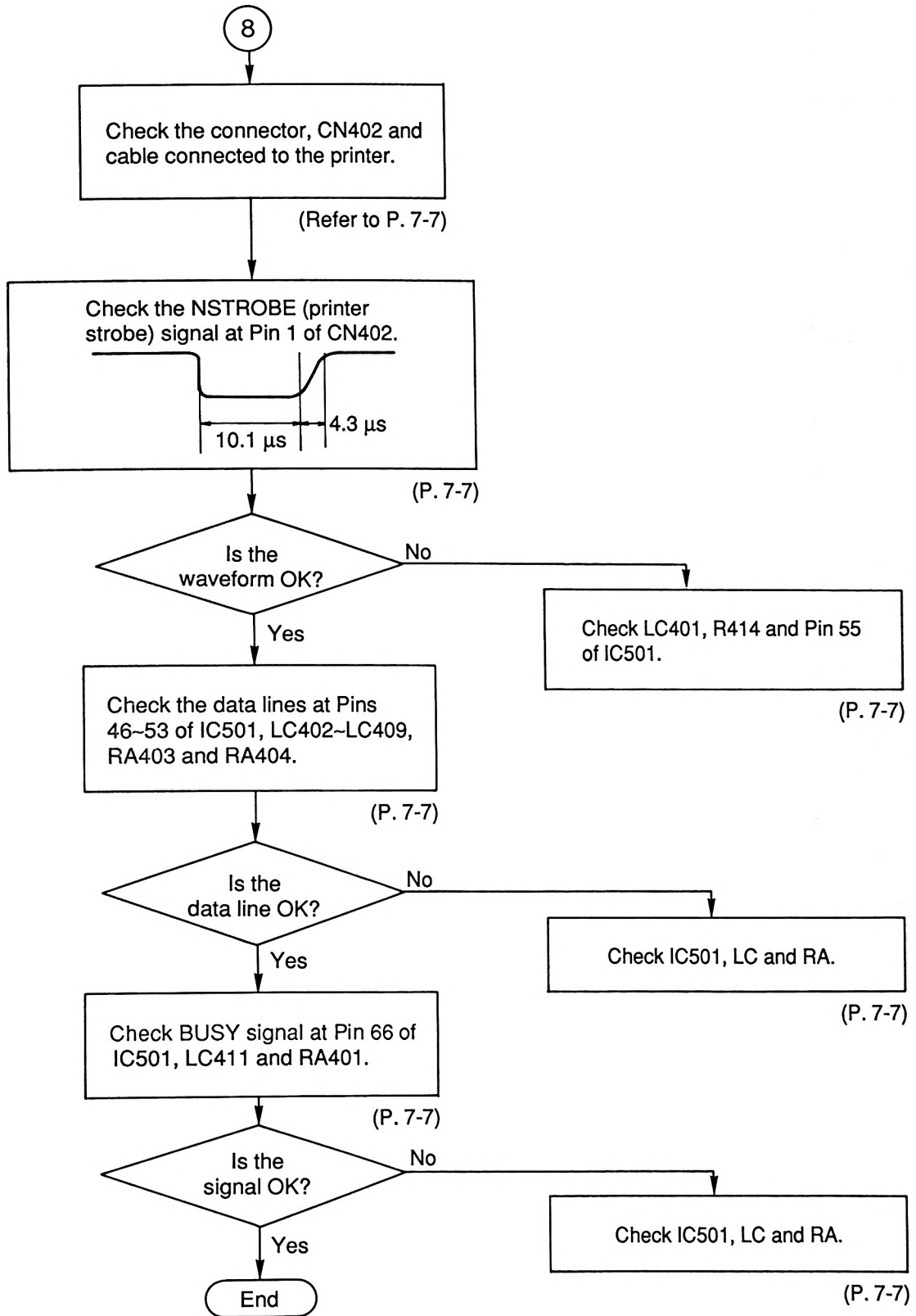
⑥ Beeper Circuit Check



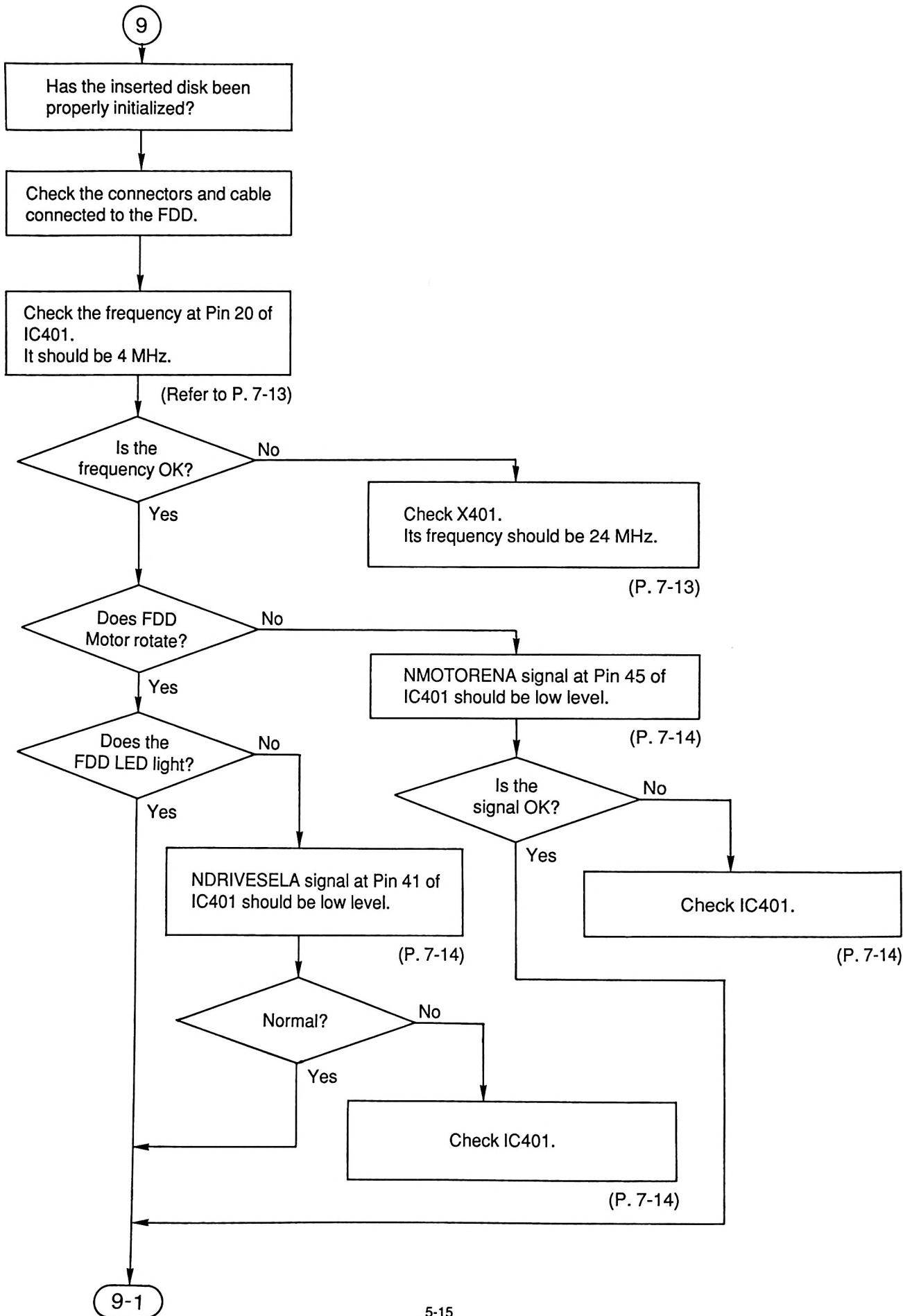
⑦ RTC Circuit Check



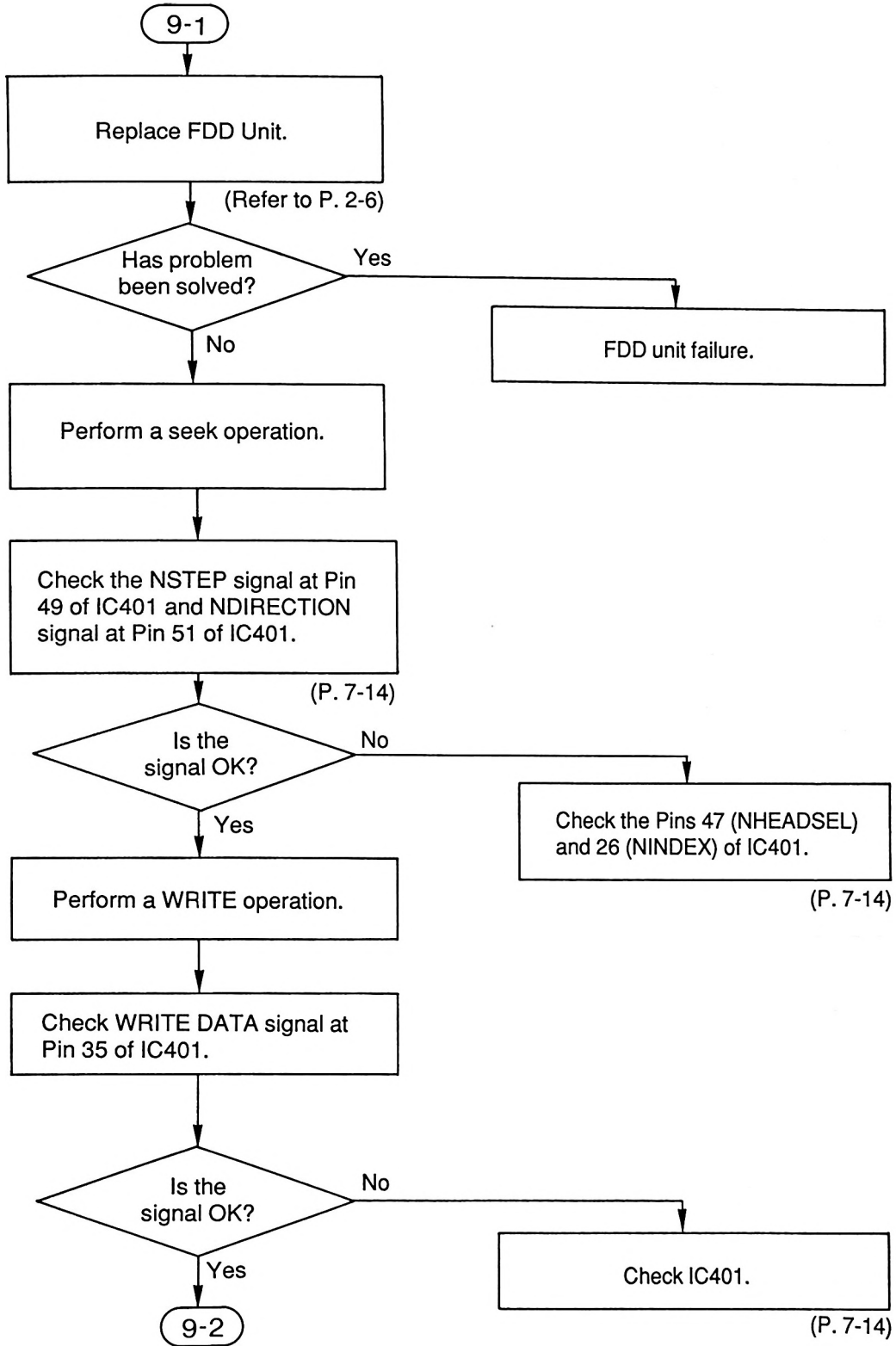
⑧ Parallel Printer Interface Check



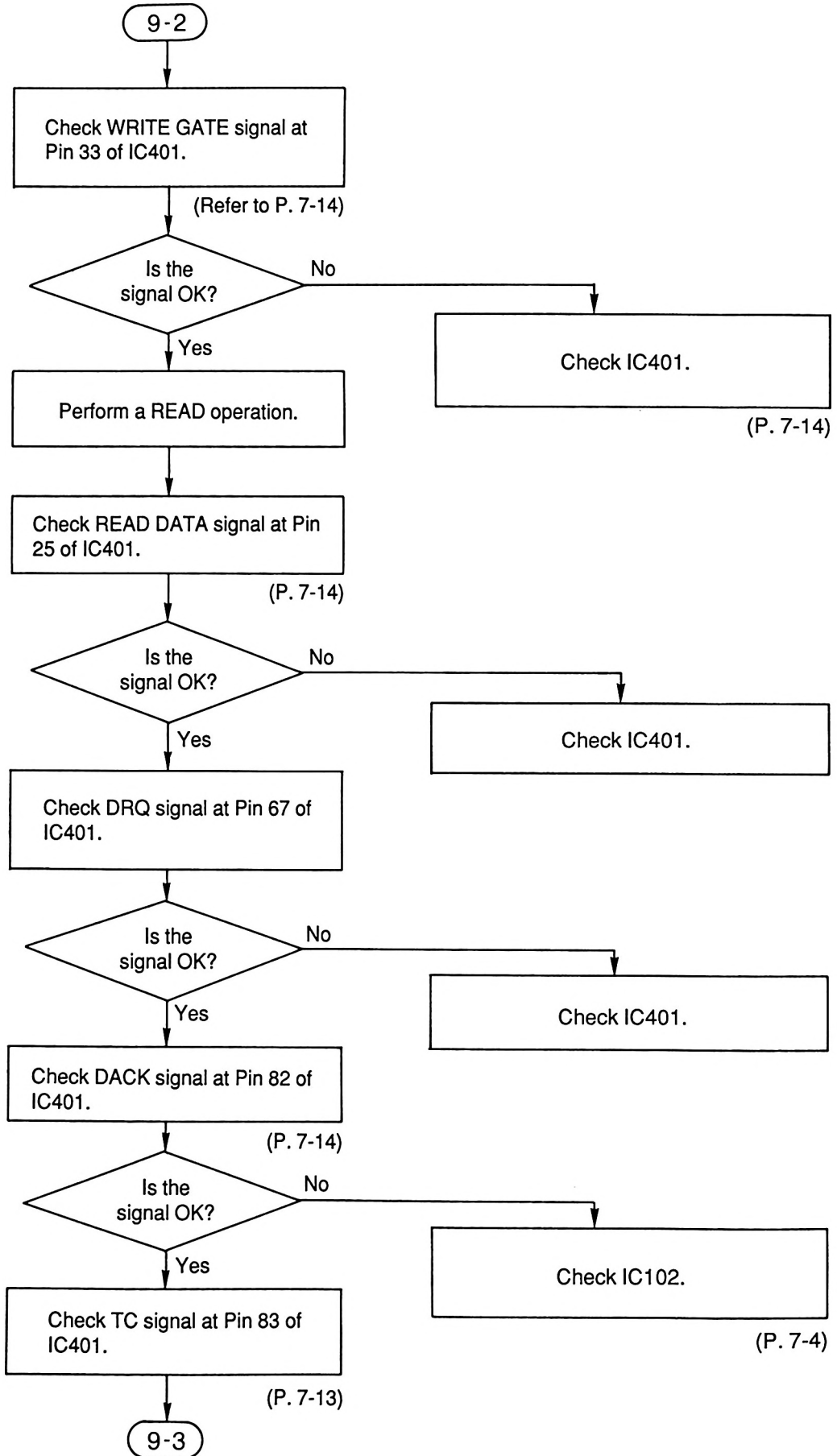
⑨ FDD Check



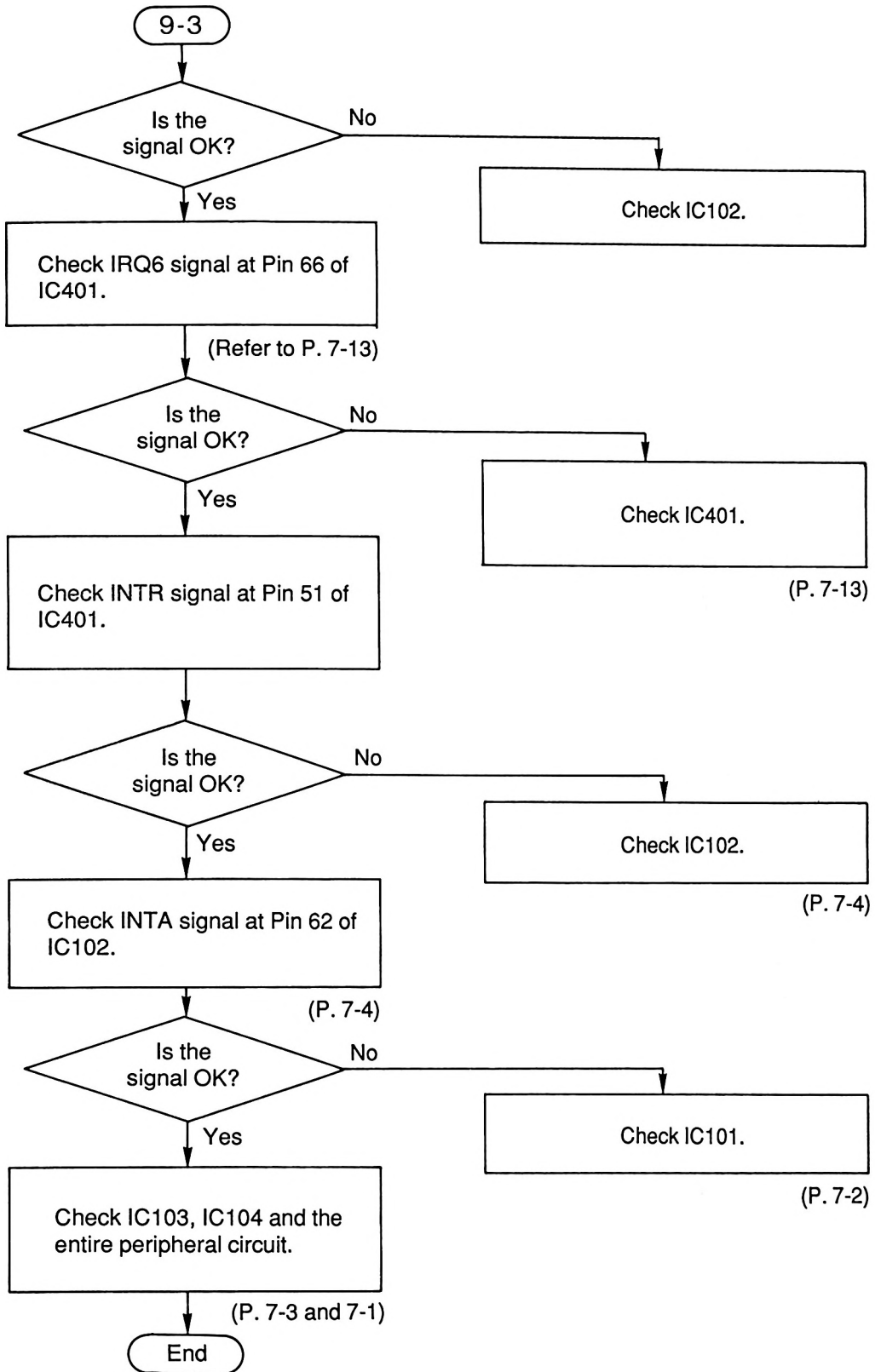
FDD Check



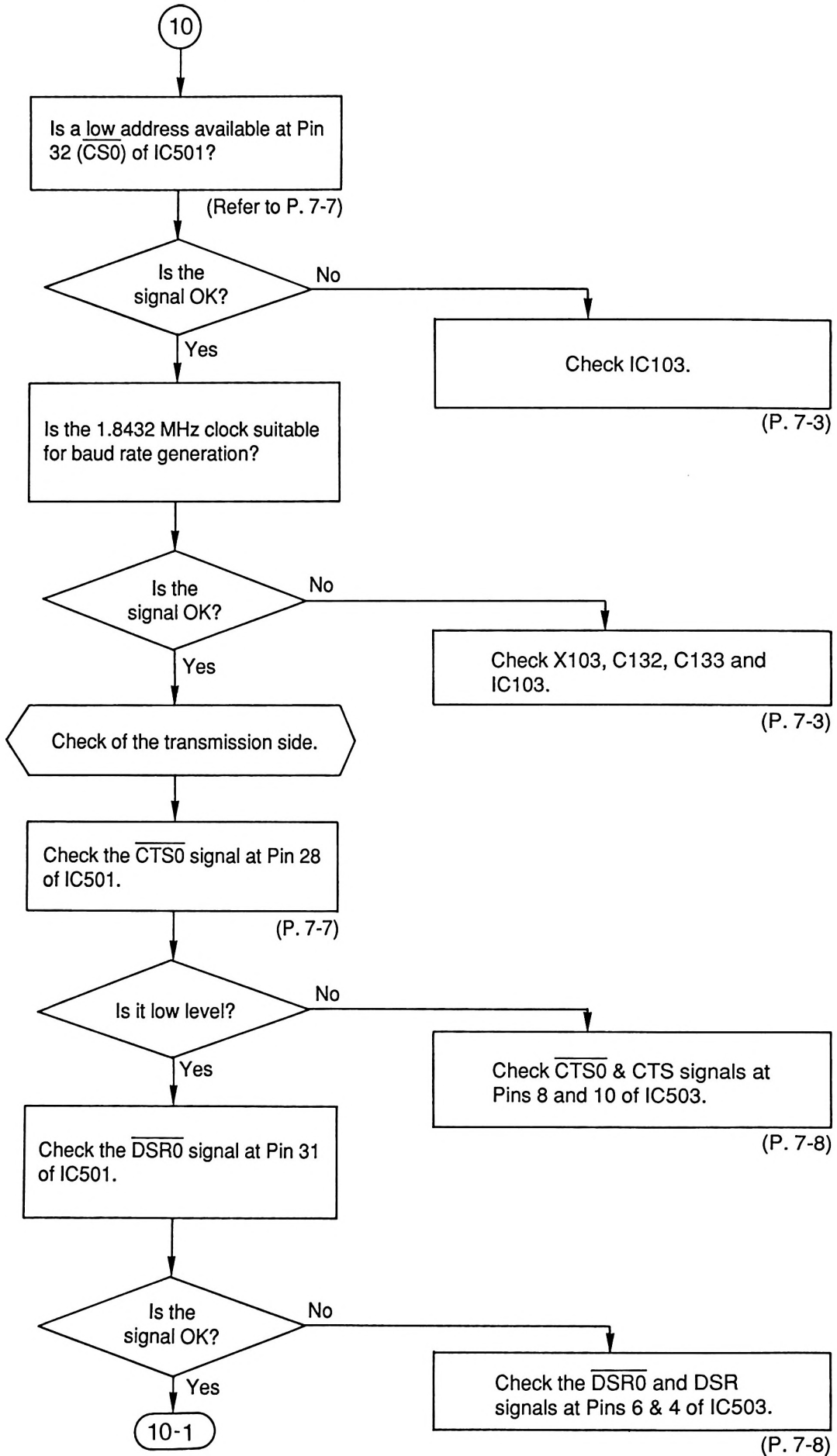
FDD Check



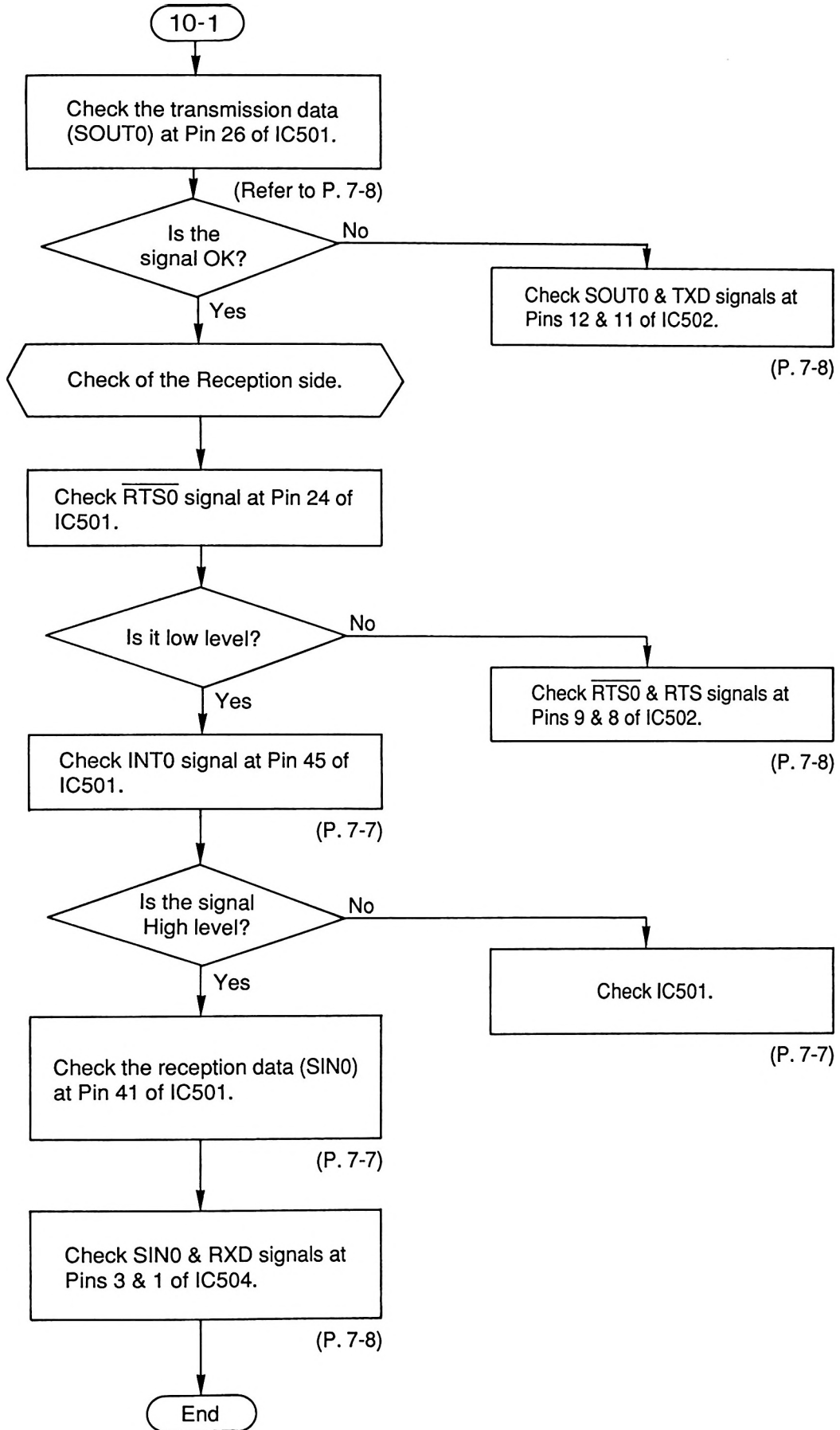
FDD Check



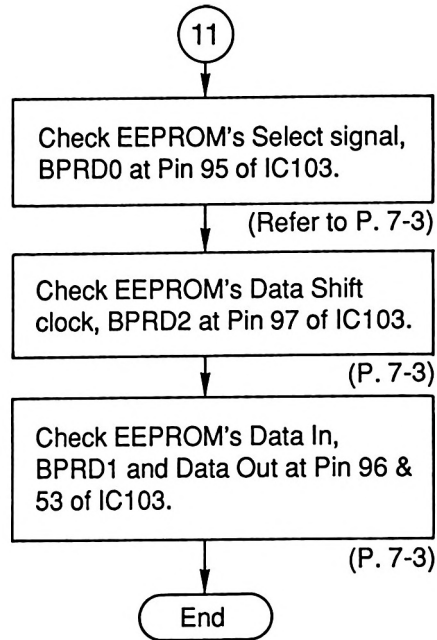
⑩ RS-232C Serial Interface Check



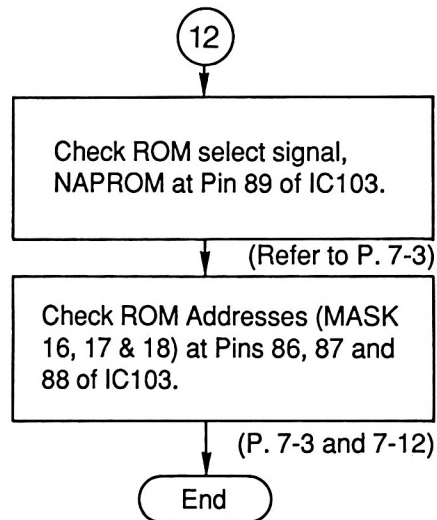
RS-232C Serial Interface Check



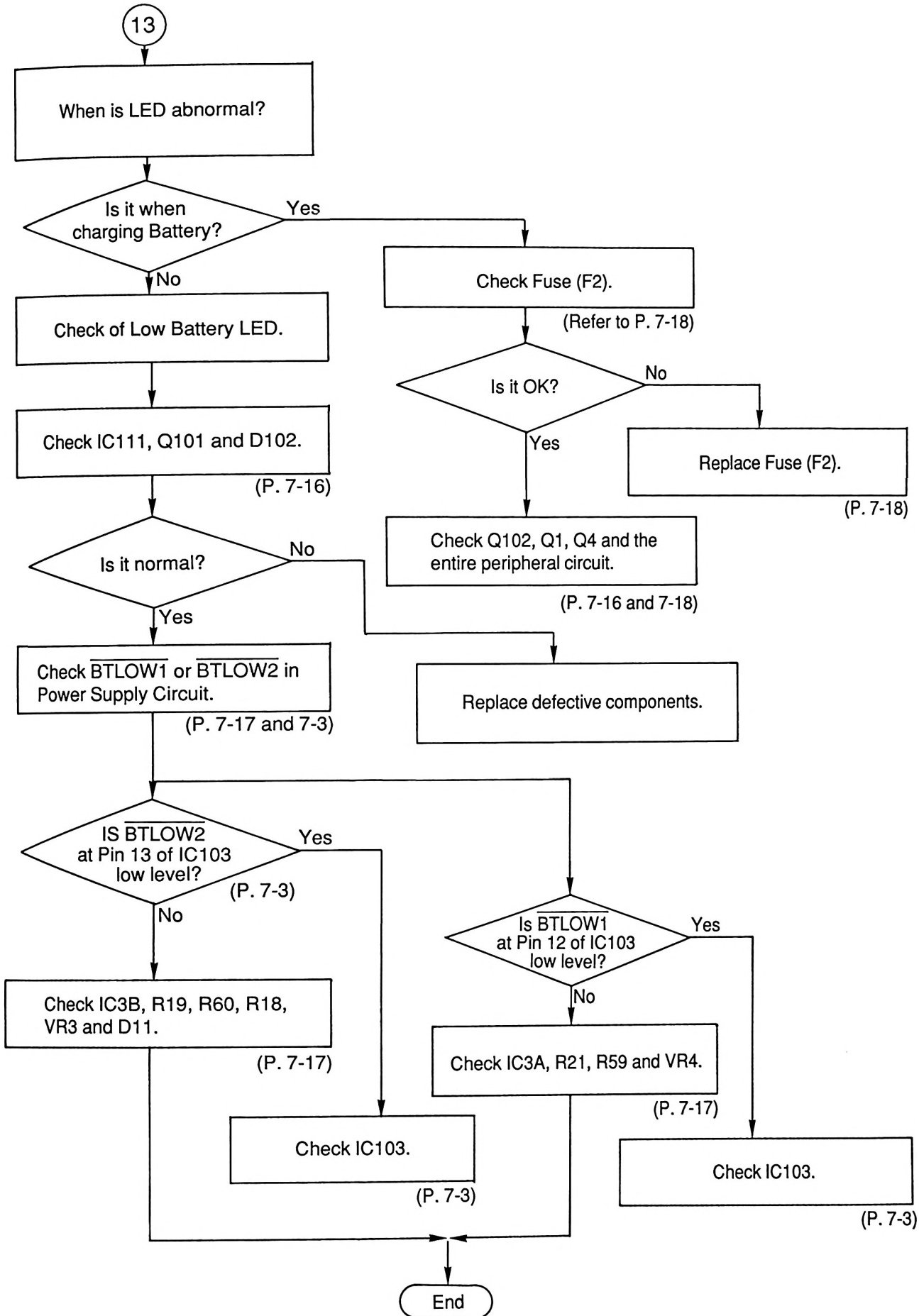
⑪ EEPROM (IC211) Check



⑫ DESKMATE/DOS ROM (IC210) Check



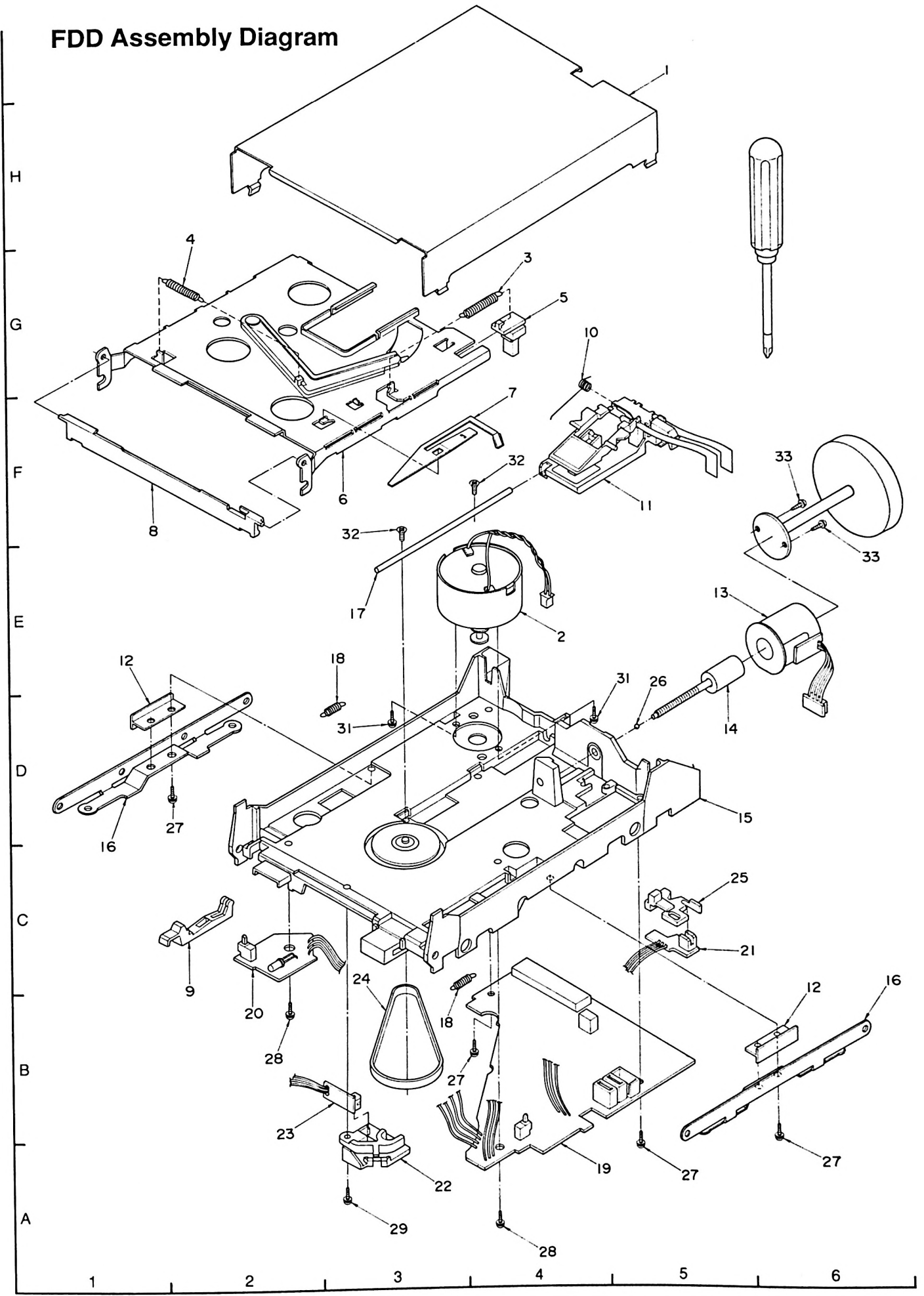
⑬ CHARGE/LOW Battery LED Check



6

12

FDD Assembly Diagram



Main PCB Assembly Parts List

REF. NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
E1	Ass'y, PCB, Main	1		DFWV48C143ZA
BATTERY				
VB601	Battery, Lithium, 3 Vdc, 1000 mA	1		CR2477-1VC
BUZZER				
BZ101	Buzzer, Piezo, 75 dB min.	1		DFAFPKM174EP
CAPACITOR				
C1	Electrolytic, 1000 μ F, \pm 20%, 10 V	1		ECEA1AU102
C2	Electrolytic, 1000 μ F, \pm 20%, 10 V	1		ECEA1AU102
C3	Electrolytic, 10 μ F, \pm 20%, 16 V	1		ECEA1CU100
C4	Electrolytic, 10 μ F, \pm 20%, 16 V	1		ECEA1CU100
C5	Electrolytic, 4.7 μ F, \pm 20%, 50 V	1		ECEA1HU4R7
C6	Electrolytic, 4.7 μ F, \pm 20%, 50 V	1		ECEA1HU4R7
C7	Electrolytic, 4.7 μ F, \pm 20%, 50 V	1		ECEA1HU4R7
C8	Electrolytic, 47 μ F, \pm 20%, 10 V	1		ECEA1AU470
C9	Electrolytic, 10 μ F, \pm 20%, 16 V	1		ECEA1CU100
C10	Electrolytic, 470 μ F, \pm 20%, 16 V	1		ECEA1CU471
C11	Electrolytic, 470 μ F, \pm 20%, 16 V	1		ECEA1CU471
C12	Electrolytic, 100 μ F, \pm 20%, 25V	1		ECEA1EU101
C13	Not used			
C14	Electrolytic, 10 μ F, \pm 20%, 16 V	1		ECEA1CU100
C15	Electrolytic, 47 μ F, \pm 20%, 16 V	1		ECEA1CU470
C16	Electrolytic, 1000 μ F, \pm 20%, 10 V	1		ECEA1AU102
C17	Electrolytic, 1000 μ F, \pm 20%, 10 V	1		ECEA1AU102
C18	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C19	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C20	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C21	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C22	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C23	Ceramic, Chip, 0.01 μ F, +80%, -20%, 50 V	1		ECUX1H103ZFG
C24	Ceramic, Chip, 2200 pF, \pm 10%, 50V	1		ECUX1H222KBN
C25	Ceramic, Chip, 0.01 μ F, +80%, -20%, 50 V	1		ECUX1H103ZFG
C26	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C27	Ceramic, Chip, 470 pF, \pm 5%, 50 V	1		ECUX1H471JCG
C28	Not used			
C29	Not used			
C30	Electrolytic, 1 μ F, \pm 20%, 50 V	1		ECEA1HU010
C31	Electrolytic, 1 μ F, \pm 20%, 50 V	1		ECEA1HU010
C32	Ceramic, Chip, 1500 pF, \pm 10%, 50 V	1		ECUX1H152KBN
C33	Electrolytic, 1 μ F, \pm 20%, 50 V	1		ECEA1HU010
C34-100	Not used			
C101	Electrolytic, 47 μ F, \pm 20%, 6.3 V	1		ECEA0JKA470
C102-104	Not used			
C105	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C106	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C107	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C108	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C109	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C110	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG

REF. NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
C111	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C112	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C113	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C114	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C115	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C116	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C117	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C118	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C119	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C120	Not used			
C121	Ceramic, 0.01 μ F, +80%, -20%, 50 V, Chip	1		ECUX1H103ZFG
C122	Ceramic, 0.01 μ F, +80%, -20%, 50 V, Chip	1		ECUX1H103ZFG
C123	Ceramic, 0.01 μ F, +80%, -20%, 50 V, Chip	1		ECUX1H103ZFG
C124	Ceramic, Chip, 100 pF, \pm 5%, 50 V	1		ECUX1H101JCG
C125	Ceramic, Chip, 100 pF, \pm 5%, 50 V	1		ECUX1H101JCG
C126	Ceramic, Chip, 100 pF, \pm 5%, 50 V	1		ECUX1H101JCG
C127	Ceramic, Chip, 100 pF, \pm 5%, 50 V	1		ECUX1H101JCG
C128	Ceramic, Chip, 33 pF, \pm 5%, 50 V	1		ECUX1H330JCN
C129	Ceramic, Chip, 33 pF, \pm 5%, 50 V	1		ECUX1H330JCN
C130	Ceramic, Chip, 22 pF, \pm 5%, 50 V	1		ECUX1H220JCN
C131	Ceramic, Chip, 22 pF, \pm 5%, 50 V	1		ECUX1H220JCN
C132	Ceramic, Chip, 15 pF, \pm 5%, 50 V	1		ECUX1H150JCN
C133	Ceramic, Chip, 15 pF, \pm 5%, 50 V	1		ECUX1H150JCN
C134	Not used			
C135	Electrolytic, 47 μ F, \pm 20%, 6.3 V	1		ECEA0JKA470
C136	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C137	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C138-200	Not used			
C201	Electrolytic, 220 μ F, \pm 20%, 6.3 V	1		ECEA0JKA221
C202	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C203	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C204	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C205	Electrolytic, 220 μ F, \pm 20%, 6.3 V	1		ECEA0JKA221
C206	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C207	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C208	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C209	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C210	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C211	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C212-301	Not used			
C302	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C303	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C304	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C305	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C306	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C307	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C308	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C309	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C310	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG

REF. NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
C311	Ceramic, Chip, 22 pF, $\pm 5\%$, 50 V	1		ECUX1H220JCN
C312	Ceramic, Chip, 22 pF, $\pm 5\%$, 50 V	1		ECUX1H220JCN
C313-400	Not used			
C401	Electrolytic, 100 μ F, $\pm 20\%$, 6.3 V	1		ECEA0JKA101
C402	Ceramic, Chip, 0.1 μ F, +80%, -20%, 50 V	1		ECUX1E104ZFG
C403	Electrolytic, 10 μ F, $\pm 20\%$, 16 V	1		ECEA1CKA100
C404	Ceramic, Chip, 0.1 μ F, +80%, -20%, 50 V	1		ECUX1E104ZFG
C405	Electrolytic, 220 μ F, $\pm 20\%$, 6.3 V	1		ECEA0JKA221
C406	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C407	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C408	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C409	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C410-500	Not used			
C501	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C502	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C503	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C504	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C505	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C506-600	Not used			
C601	Ceramic, Chip, 100 pF, $\pm 5\%$, 50 V	1		ECUX1H101JCG
C602-700	Not used			
C701	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C702	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C703	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C704	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C705	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUX1E104ZFG
C706	Ceramic, Chip, 0.01 μ F, +80%, -20%, 50 V	1		ECUX1H103ZFG
C707	Ceramic, Chip, 1000 pF, +80%, -20%, 50 V	1		ECUX1H102ZFN
C708	Ceramic, Chip, 1000 pF, +80%, -20%, 50 V	1		ECUX1H102ZFN
C709	Ceramic, Chip, 1000 pF, +80%, -20%, 50 V	1		ECUX1H102ZFN
C710	Ceramic, Chip, 1000 pF, +80%, -20%, 50 V	1		ECUX1H102ZFN
C711	Ceramic, Chip, 1000 pF, +80%, -20%, 50 V	1		ECUX1H102ZFN
C712	Ceramic, Chip, 1000 pF, +80%, -20%, 50 V	1		ECUX1H102ZFN
C713	Ceramic, Chip, 1000 pF, +80%, -20%, 50 V	1		ECUX1H102ZFN
C714	Ceramic, Chip, 1000 pF, +80%, -20%, 50 V	1		ECUX1H102ZFN
C715	Ceramic, Chip, 1000 pF, +80%, -20%, 50 V	1		ECUX1H102ZFN
C716	Ceramic, Chip, 1000 pF, +80%, -20%, 50 V	1		ECUX1H102ZFN
C717	Ceramic, Chip, 1000 pF, +80%, -20%, 50 V	1		ECUX1H102ZFN
C718	Ceramic, Chip, 1000 pF, +80%, -20%, 50 V	1		ECUX1H102ZFN
CAPACITOR TRIMMER				
TC1-600	Not used			
TC601	Trimmer, Chip, 20 pF, +50%, -0%, 100 V	1		ECRJA020E12W
COIL INDUCTOR				
L1	100 ohm, (10-300 MHz), 3 A	1		DDB6Z057
L2	100 ohm, (10-300 MHz), 3 A	1		DDB6Z057
L3	33 μ H, 2.9 A	1		DDAWZ330KV
L4	30 ohm, (10-300 MHz), 3 A	1		DDB6Z003T
L5	220 μ H, 0.64 A	1		DDA895Z221K
L6	1.1 μ H, 1 MHz, 6 A	1		DDB1Z084T
L7	33 μ H, 2.9 A	1		DDAWZ330KV

REF. NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
L8	1.1 μ H, 1 MHz, 6 A	1		DDB1Z084T
L9	150 μ H, 1.4 A	1		DDAWZ151KV
L10	0.6 mH, 3 A	1		DDB8Z008
L11	100 ohm, (10-300 MHz), 3 A	1		DDB6Z057
L12-300	Not used			
L301	3-turn, 0.8 A	1		DDB1Z029
L302	60 μ H, 500 mA	1		DDB7Z003T
L303	60 μ H, 500 mA	1		DDB7Z003T
L304	60 μ H, 500 mA	1		DDB7Z003T
L305	60 μ H, 500 mA	1		DDB7Z003T
L306	60 μ H, 500 mA	1		DDB7Z003T
L307	60 μ H, 500 mA	1		DDB7Z003T
L308-311	Not used			
L312	60 μ H, 500 mA	1		DDB7Z003T
L313-404	Not used			
L405	100 μ H, 90 mA	1		ELEPL101KA
CONNECTOR				
CN1	Female, Rechargeable Battery, 2-pin	1		DFJP02C32Z
CN2	Board-in, 2-pin	1		DFJS02C30Z
CN3	DC In Jack	1		RJJ97Y
CN4	Board-in, 2-pin	1		DFJS02C30Z
CN5	Male, Test, 8-pin	1		DFJP08C13Z
CN6-100	Not used			
CN101	Female, LED Board, 2-pin	1		RJP2G4Y
CN102	Board-in, 2-pin	1		DFJS02C30Z
CN103-300	Not used			
CN301	Male, LCD, 16-pin	1		DFJP16C54Z
CN302-400	Not used			
CN401	Female, FDD, 24-pin	1		DFJS24N13Z
CN402	Female, Parallel, 25-pin	1		DFJS25E05Z
CN403-500	Not used			
CN501	Male, RS-232C, 9-pin	1		DFJP09E14Z
CN502-700	Not used			
CN701	Female, Keyboard, 8-pin	1		DFJS08N19Z
CN702	Female, Keyboard, 14-pin	1		DFJS14N19Z
CN703-800	Not used			
CN801	Female, MODEM, 18-pin	1		DFJS18N13Z
CONNECTOR ASS'Y				
K1-36	Used for Mechanical and Assembly Parts			
K37	LCD, 16-pin	1		DFJS00Z92Z
K38	FDD, 24-pin	1		DFJE24A105AS
K39	Rechargeable Battery, 2-pin	1		DFJP00Z55Z
DIODE				
D1	Schottky Barrier, High Speed Power, Switching, ERC81	1		DEDRC81004L9

REF. NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
D2	Schottky Barrier, High Speed Power, Switching, ERC81	1		DEDRC81004L9
D3	Zener, SI Planar, Stabilized Power Supply, Chip, MA3051M	1		MA3051MTW MA3051HTW
D4	Zener, SI Planar, Chip, MA3082M	1		MA3082MTW MA3082HTW
D5	Switching, SI Epitaxial Planar, Chip, MA151A	1		MA151ATW
D6	Schottky Barrier, High Frequency Rectifier, Chip, MA701A	1		MA701TW MA701ATW
D7	Schottky Barrier, High Frequency Rectifier, Chip, MA701	1		MA701TW MA701ATW
D8	Schottky Barrier, High Frequency Rectifier, Chip, MA701A	1		MA701ATW
D9	Schottky Barrier, High Frequency Rectifier, Chip, MA701	1		MA701TW MA701ATW
D10	Schottky Barrier, High Frequency Rectifier, Chip, MA701	1		MA701TW MA701ATW
D11	Switching, SI Epitaxial Planar, Chip, MA151A	1		MA151ATW
D12	Not used			
D13	Schottky Barrier, High Frequency Rectifier, Chip, MA701	1		MA701TW MA701ATW
D14	Zener, Chip, MA3033M	1		MA3033HTW
D15	Not used			
D16	Not used			
D17	Not used			
D18	Zener, MA3240	1		MA3240MTW MA3240HTW
D19	Stabilized Power Supply, SI Planar MA1075M	1		MA1075M
D20-100	Not used			
D101	Switching, SI Epitaxial Planar, Chip, MA151A	1		MA151ATW
D102	Switching, SI Epitaxial Planar, Chip, MA151A	1		MA151ATW
D103	Switching, SI Epitaxial Planar, Chip, MA151A	1		MA151ATW
D104-600	Not used			
D601	Switching, SI Epitaxial Planar, Chip, MA151A	1		MA151ATW
D602	Zener, Chip, MA3039L	1		MA3039LTW MA3039MTW
FILTER				
LC1-312	Not used			
LC313	EMI, 22000 pF, 3-pin	1		DEA306F223TL
LC314	EMI, 22000 pF, 3-pin	1		DEA306F223TL
LC315	EMI, 22000 pF, 3-pin	1		DEA306F223TL
LC316	EMI, 22000 pF, 3-pin	1		DEA306F223TL

REF. NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
LC317	EMI, 22000 pF, 3-pin	1		DEA306F223TL
LC318-400	Not used			
LC401	EMI, 2200 pF, 3-pin	1		DEA306E222TL
LC402	EMI, 2200 pF, 3-pin	1		DEA306E222TL
LC403	EMI, 2200 pF, 3-pin	1		DEA306E222TL
LC404	EMI, 2200 pF, 3-pin	1		DEA306E222TL
LC405	EMI, 2200 pF, 3-pin	1		DEA306E222TL
LC406	EMI, 2200 pF, 3-pin	1		DEA306E222TL
LC407	EMI, 2200 pF, 3-pin	1		DEA306E222TL
LC408	EMI, 2200 pF, 3-pin	1		DEA306E222TL
LC409	EMI, 2200 pF, 3-pin	1		DEA306E222TL
LC410	EMI, 2200 pF, 3-pin	1		DEA306E222TL
LC411	EMI, 2200 pF, 3-pin	1		DEA306E222TL
LC412	EMI, 2200 pF, 3-pin	1		DEA306E222TL
LC413	EMI, 2200 pF, 3-pin	1		DEA306E222TL
LC414	EMI, 2200 pF, 3-pin	1		DEA306E222TL
LC415	EMI, 2200 pF, 3-pin	1		DEA306E222TL
LC416	EMI, 2200 pF, 3-pin	1		DEA306E222TL
LC417	EMI, 2200 pF, 3-pin	1		DEA306E222TL
LC418	EMI, 2200 pF, 3-pin	1		DEA306E222TL
LC419	EMI, 2200 pF, 3-pin	1		DEA306E222TL
FUSE				
IP1	Fast Blow, 1.6 A, 125 V, 7.5 mm (L)x2.6 mm (H), with Pigtail	1		XBADPR1R60F5
F2	Fast Blow, 0.8 A, 125 V 7.5 mm (L)x2.6 mm (H), with Pigtail	1		XBAD0800VFS
F3	Fast Blow, 2.5 A, 125 V 7.5 mm (L)x2.6 mm (H), with Pigtail	1		XBAD2500VFS
IC and Gate Array				
IC1	M5237L, Regulator, 3-terminal	1		DAM5237LTAM
IC2	LM393ML, Comparator, Dual, 8-pin	1		DALM393ML DABA10393FTE
IC3	LM393ML, Comparator, Dual, 8-pin	1		DALM393ML DABA10393FTE
IC4	AN8002, Regulator, 3-terminal, For +12 V	1		AN8002
IC5	MB3775, Converter, DC-DC, 16-pin	1		DA3775PF-GTJ
IC6	Not used			
IC7	MC79L12ACPRA, Regulator, 3-terminals, For -12 V	1		DA79L12ACPRQ
IC8	Not used			
IC9	34063HAU, Converter, DC-DC, 8-pin	1		DAMC34063MLQ
IC10	5247, Reset, 8-pin	1		DAM5247FPT
IC11-100	Not used			
IC101	D70108GC-8, CPU, C-MOS, V20, 8 MHz	1		DA70108G-8D
IC102	MN12862, Multiple Peripheral, C-MOS, 100-pin	1		MN12862
IC103	MN53030RFP, Gate Array, C-MOS, 124-pin	1		MN53030RFP
IC104	MN53020RFQ, Gate Array, C-MOS, 100-pin	1		MN53020RFQ
IC105	74HC245A, C-MOS, High Speed, 20-pin	1		MN74HC245S DA74HC245FT0

REF. NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
IC106	74HC245A, C-MOS, High Speed, 20-pin	1		MN74HC245S DA74HC245FT0
IC107	74HC244A, C-MOS, High Speed, 20-pin	1		MN74HC244S DA74HC244FT0
IC108	74HC244A, C-MOS, High Speed, 20-pin	1		MN74HC244S DA74HC244FT0
IC109	Not used			
IC110	74HCU04S, C-MOS, High Speed, 14-pin	1		DA74HCU04AF0 MN74HCU04S
IC111	74HCU04S, C-MOS, High Speed, 14-pin	1		DA74HCU04AF0 MN74HCU04S
IC112-200	Not used			
IC201	M5M44256AL10, DRAM, C-MOS, 1M bit	1		MN41C4256L08 DA44256AL10M
IC202	M5M44256AL10, DRAM, C-MOS, 1M bit	1		MN41C4256L08 DA44256AL10M
IC203	M5M44256AL10, DRAM, C-MOS, 1M bit	1		MN41C4256L08 DA44256AL10M
IC204	M5M44256AL10, DRAM, C-MOS, 1M bit	1		MN41C4256L08 DA44256AL10M
IC205	M5M4464AP, DRAM, C-MOS, 256K bit	1		MN41464A-08 DAM4464AP10M
IC206	M5M4464AP, DRAM, C-MOS, 256K bit	1		MN41464A-08 DAM4464AP10M
IC207	M5M4464AP, DRAM, C-MOS, 256K bit	1		MN41464A-08 DAM4464AP10M
IC208	M5M4464AP, DRAM, C-MOS, 256K bit	1		MN41464A-08 DAM4464AP10M
IC209	M5M27C256K-15, EPROM, C-MOS, 256K bit	1		DAFT1A3
IC210	MASK ROM, C-MOS, 4M bit, 32-pin	1		DAFT1C1
IC211	AK93C46, EEPROM, C-MOS, 128K bit	1		DA93C46001XQ
IC212-300	Not used			
IC301	MN5502, LCDC, C-MOS, 124-pin	1		MN5502
IC302	RP2364E, MASK ROM, 64K bit, N-MOS	1		DAFT1B1
IC303	M5M5165FP-10L, SRAM, 64K bit, 28-pin	1		DA8464-10LTJ DA5165F10L1M
IC304	M5M5165FP-10L, SRAM, 64K bit, 28-pin	1		DA8464-10LTJ DA5165F10L1M
IC305	74HCU04S, C-MOS, High Speed, 14-pin	1		DA74HCU04AF0 MN74HCU04S
IC306-400	Not used			
IC401	SPC2050F0A, FDC, C-MOS, 100-pin	1		DA2050F0AW
IC402-500	Not used			
IC501	MX16C452, UART/PARA, C-MOS, 68-pin	1		DA16C452XV DA16C452XW
IC502	DS14C88M, Driver, RS-232C, C-MOS	1		DA14C88AMTEN
IC503	DS14C89M, Receiver, RS-232C, C-MOS	1		DA14C89AMTEN
IC504	DS14C89M, Receiver, RS-232C, C-MOS	1		DA14C89ATEN
IC505-600	Not used			
IC601	RF5C15, RTC, 18-pin	1		DARF5C15

REF. NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
IC602-700	Not used			
IC701	49HG528, Controller, Keyboard	1		DA49HG-528
IC702	HC125A, C-MOS, 14-pin	1		MN74HC125S
IC703	HC09, C-MOS, 14-pin	1		DA74HC125FT0 DA74HC09AFT0 DASN74HC09ST
IC704	LM339ML, Comparator, 14-pin	1		DALM339ML DALM339MT
IC705	LM339ML, Comparator, 14-pin	1		DALM339ML DALM339MT
JUMPER				
J1-200	Not used			
J201	Jumper, Chip	1		ERJ6GMYJ0R00
J203	Jumper, Chip	1		ERJ6GMYJ0R00
J204	Not used			
J205	Jumper, Chip	1		ERJ6GMYJ0R00
J206-300	Not used			
J301	Jumper, Chip	1		ERJ6GMYJ0R00
OSCILLATOR				
X1-100	Not used			
X101	Ceramics, 16 MHz	1		DEBM16R0N2LX DEBM16R0N1WX
X102	Crystal, 14.31818 MHz	1		DECX14318H2H
X103	Ceramics, 1.843 MHz	1		DEBM1R843N1L
X104-300	Not used			
X301	Ceramics, 9.22 MHz	1		DEBM9R22N1L
X302-400	Not used			
X401	Crystal, 24.00 MHz	1		DECX24000H1H
X402-600	Not used			
X601	Crystal, RTC, 32.768 KHz	1		DECQ00032H3W
POTENTIONMETER				
VR1	Semi-fix, 3.3 Kohm, B-curve	1		DENAE1B332TL
VR2	Semi-fix, 10 Kohm, B-curve	1		DENAE1B103TL
VR3	Semi-fix, 10 Kohm, B-curve	1		DENAE1B103TL
VR4	Semi-fix, 10 Kohm, B-curve	1		DENAE1B103TL
VR5	Semi-fix, 10 Kohm, B-curve	1		DENAE1B103TL
RESISTOR				
R1	Metal Oxide, Chip, 1 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMJ102 DBJ6GMJ102
R2	Metal Oxide, Chip, 1.5 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMJ152 DBJ6GMJ152
R3	Metal Oxide, Chip, 220 ohm, 1/10 W, $\pm 5\%$	1		ERJ6GMJ221 DBJ6GMJ221

REF. NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
R4	Metal Oxide, Chip, 100 ohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ101 DBJ6GMJ101
R5	Metal Oxide, Chip, 1 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ102 DBJ6GMJ102
R6	Metal Oxide, Chip, 820 ohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ821 DBJ6GMJ821
R7	Metal Oxide, Chip, 200 ohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ201 DBJ6GMJ201
R8	Metal Oxide, Chip, 200 ohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ201 DBJ6GMJ201
R9	Metal Oxide, Chip, 7.5 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ752 DBJ6GMJ752
R10	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R11	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R12	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R13	Metal Oxide, Chip, 39 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ393 DBJ6GMJ393
R14	Metal Oxide, Chip, 4.02 Kohm, 1/10W, $\pm 1\%$	1		ERJ6ENF4021 DBJ6GF4021
R15	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R16	Metal Oxide, Chip, 4.03 Kohm, 1/10 W, $\pm 1\%$	1		ERJ6ENF4301 DBJ6GF4301
R17	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R18	Metal Oxide, Chip, 15 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ153 DBJ6GMJ153
R19	Metal Oxide, Chip, 180 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ184 DBJ6GMJ184
R20	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R21	Metal Oxide, Chip, 15 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ153 DBJ6GMJ153
R22	Not used			
R23	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R24	Not used			
R25	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R26	Not used			
R27	Metal Oxide, Chip, 330 ohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ331 DBJ6GMJ331
R28	Metal Oxide, Chip, 2.2 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ222 DBJ6GMJ222
R29	Metal Oxide, Chip, 2 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ202 DBJ6GMJ202
R30	Metal Oxide, Chip, 150 ohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ151 DBJ6GMJ151

REF. NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
R31	Metal Oxide, Chip, 150 ohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ151 DBJ6GMJ151
R32	Metal Oxide, Chip, 47 ohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ470 DBJ6GMJ470
R33	Metal Oxide, Chip, 100 ohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ101 DBJ6GMJ101
R34	Metal Oxide, Chip, 4.03 Kohm, 1/10 W, $\pm 1\%$	1		ERJ6ENF4301 DBJ6GF4301
R35	Metal Oxide, Chip, 36 Kohm, 1/10 W, $\pm 1\%$	1		ERJ6ENF3602 DBJ6GF3602
R36	Not used			
R37	Not used			
R38	Metal Oxide, Chip, 100 ohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ101 DBJ6GMJ101
R39	Metal Oxide, Chip, 620 ohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ621 DBJ6GMJ621
R40	Metal Oxide, Chip, 620 ohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ621 DBJ6GMJ621
R41	Metal Oxide, Chip, 1 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ102 DBJ6GMJ102
R42	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R44	Metal Oxide, Chip, 3 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6ENF3001 DBJ6GF3001
R45	Metal Oxide, Chip, 20 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6ENF2002 DBJ6GF2002
R46	Metal Oxide, Chip, 7.5 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6ENF7501 DBJ6GF7501
R47	Metal Oxide, Chip, 51 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ513 DBJ6GMJ513
R48	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R49	Metal Oxide, Chip, 82 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ823 DBJ6GMJ823
R50	Metal Oxide, Chip, 4.03 Kohm, 1/10 W, $\pm 1\%$	1		ERJ6ENF4301 DBJ6GF4301
R51	Metal Oxide, Chip, 12 Kohm, 1/10 W, $\pm 1\%$	1		ERJ6ENF1202 DBJ6GF1202
R52	Not used			
R53	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R54	Metal Oxide, 33 ohm, 3 W, $\pm 5\%$	1		ERG3SJ330
R55	Metal Oxide, Chip, 2.2 Kohm, 1/10 W, $\pm 1\%$	1		ERJ6ENF2201 DBJ6GF2201
R56	Metal Oxide, Chip, 6.8 Kohm, 1/10 W, $\pm 1\%$	1		ERJ6ENF6801 DBJ6GF6801
R57	Metal Oxide, 1.8 ohm, 1 W, $\pm 5\%$	1		ERX1SJ1R8
R58	Metal Oxide, Chip, 4.3 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ432 DBJ6GMJ432
R59	Metal Oxide, Chip, 12 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ123 DBJ6GMJ123

REF. NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
R60	Metal Oxide, Chip, 12 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMJ123 DBJ6GMJ123
R61	Metal Oxide, Chip, 1 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMJ102 DBJ6GMJ102
R62	Metal Oxide, Chip, 47 ohm, 1/10 W, $\pm 5\%$	1		ERJ6GMJ470 DBJ6GMJ470
R63	Metal Oxide, Chip, 20 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMJ203 DBJ6GMJ203
R64	Metal Oxide, Chip, 12 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMJ123 DBJ6GMJ123
R65	Not used			
R66	Not used			
R67	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMJ103 DBJ6GMJ103
R68	Metal Oxide, Chip, 20 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMJ203 DBJ6GMJ203
R69	Metal Oxide, Chip, 12 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMJ123 DBJ6GMJ123
R70-72	Not used			
R73	Metal Oxide, 100 ohm, 1/2 W, $\pm 5\%$	1		ERG12SJ101
R74-100	Not used			
R101	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMJ103 DBJ6GMJ103
R102	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMJ103 DBJ6GMJ103
R103	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMJ103 DBJ6GMJ103
R104	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMJ103 DBJ6GMJ103
R105	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMJ103 DBJ6GMJ103
R106	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMJ103 DBJ6GMJ103
R107	Metal Oxide, Chip, 100 ohm, 1/10 W, $\pm 5\%$	1		ERJ6GMJ101 DBJ6GMJ101
R108	Metal Oxide, Chip, 100 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMJ105 DBJ6GMJ105
R109	Metal Oxide, Chip, 4.7 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMJ472 DBJ6GMJ472
R110	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMJ103 DBJ6GMJ103
R111	Metal Oxide, Chip, 33 ohm, 1/10 W, $\pm 5\%$	1		ERJ6GMJ330 DBJ6GMJ330
R112	Metal Oxide, Chip, 33 ohm, 1/10 W, $\pm 5\%$	1		ERJ6GMJ330 DBJ6GMJ330
R113	Metal Oxide, Chip, 33 ohm, 1/10 W, $\pm 5\%$	1		ERJ6GMJ330 DBJ6GMJ330
R114	Metal Oxide, Chip, 33 ohm, 1/10 W, $\pm 5\%$	1		ERJ6GMJ330 DBJ6GMJ330
R115	Metal Oxide, Chip, 33 ohm, 1/10 W, $\pm 5\%$	1		ERJ6GMJ330 DBJ6GMJ330

REF. NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
R116	Metal Oxide, Chip, 33 ohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ330 DBJ6GMJ330
R117	Metal Oxide, Chip, 33 ohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ330 DBJ6GMJ330
R118	Metal Oxide, Chip, 33 ohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ330 DBJ6GMJ330
R119	Metal Oxide, Chip, 33 ohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ330 DBJ6GMJ330
R120	Metal Oxide, Chip, 33 ohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ330 DBJ6GMJ330
R121	Metal Oxide, Chip, 33 ohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ330 DBJ6GMJ330
R122	Metal Oxide, Chip, 33 ohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ330 DBJ6GMJ330
R123	Metal Oxide, Chip, 33 ohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ330 DBJ6GMJ330
R124	Metal Oxide, Chip, 33 ohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ330 DBJ6GMJ330
R125	Metal Oxide, Chip, 33 ohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ330 DBJ6GMJ330
R126	Metal Oxide, Chip, 240 ohm, 1/4 W, $\pm 5\%$	1		ERJ14YJ241
R127	Metal Oxide, Chip, 56 ohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ560 DBJ6GMJ560
R128	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R129	Metal Oxide, Chip, 240 ohm, 1/4 W, $\pm 5\%$	1		ERJ14YJ241
R130	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R131	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R132	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R133	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R134	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R135	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R136	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R137	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R138	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R139	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R140	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R141	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R142	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103

REF. NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
R143	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R144	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R145	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R146	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R147	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R148	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R149	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R150	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R151	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R152	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R153	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R154	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R155	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R156	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R157-200	Not used			
R201	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R202	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R203	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R204	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R205	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R206	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R207	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R208	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R209-300	Not used			
R301	Metal Oxide, Chip, 4.7 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ472 DBJ6GMJ472
R302	Metal Oxide, Chip, 100 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ105 DBJ6GMJ105
R303	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103

REF. NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
R304	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103
R305	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		DBJ6GMJ103
R306	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103
R307	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		DBJ6GMJ103
R308	Not used			
R309	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103
R310	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		DBJ6GMJ103
R311	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103
R312	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		DBJ6GMJ103
R313	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103
R314-400	Not used			
R401	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		DBJ6GMJ103
R402	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103
R403	Not used			
R404	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		DBJ6GMJ103
R405	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103
R406	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		DBJ6GMJ103
R407	Metal Oxide, Chip, 10Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103
R408	Not used			
R409	Metal Oxide, Chip, 1 Kohm, 1/10 W, $\pm 5\%$	1		DBJ6GMJ102
R410	Metal Oxide, Chip, 1 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ102
R411	Metal Oxide, Chip, 1 Kohm, 1/10 W, $\pm 5\%$	1		DBJ6GMJ102
R412	Metal Oxide, Chip, 1 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ102
R413	Metal Oxide, Chip, 1 Kohm, 1/10 W, $\pm 5\%$	1		DBJ6GMJ102
R414	Metal Oxide, Chip, 4.7 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ472
R415	Carbon, 330 ohm, 1/4 W, $\pm 5\%$	1		DBJ6GMJ472
R416-500	Not used			ERDS2TJ331
R501	Metal Oxide, Chip, 4.7 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ472
R502-600	Not used			DBJ6GMJ472

REF. NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
R601	Metal Oxide, Chip, 10 ohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R602	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R603	Metal Oxide, Chip, 1 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ102 DBJ6GMJ102
R604	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R605-700	Not used			
R701	Metal Oxide, Chip, 3.6 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ362 DBJ6GMJ362
R702-717	Not used			
R718	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R719	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R720-726	Not used			
R727	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R728	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
R729	Metal Oxide, Chip, 56 ohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ560 DBJ6GMJ560
R730-900	Not used			
R901	Metal Oxide, Chip, 10 Kohm, 1/10 W, $\pm 5\%$	1		ERJ6GMYJ103 DBJ6GMJ103
RESISTOR ARRAY				
RA1-400	Not used			
RA401	Resistor Array, Metal Oxide, 4.7 Kohm \times 4	1		DEANR4J5J472
RA402	Resistor Array, Metal Oxide, 4.7 Kohm \times 4	1		DEANR4J5J472
RA403	Resistor Array, Metal Oxide, 4.7 Kohm \times 4	1		DEANR4J5J472
RA404	Resistor Array, Metal Oxide, 4.7 Kohm \times 4	1		DEANR4J5J472
RA405-700	Not used			
RA701	Resistor Array, Metal Oxide, 4.7 Kohm \times 4	1		DEANR4J5J103
RA702	Resistor Array, Metal Oxide, 4.7 Kohm \times 4	1		DEANR4J5J103
RA703	Resistor Array, Metal Oxide, 4.7 Kohm \times 4	1		DEANR4J5J103
RA704	Resistor Array, Metal Oxide, 4.7 Kohm \times 4	1		DEANR4J5J103
RA705-900	Not used			
RA901	Resistor Array, Metal Oxide, 4.7 Kohm \times 4	1		DEANR4J5J103
RA902	Resistor Array, Metal Oxide, 4.7 Kohm \times 4	1		DEANR4J5J103
RA903	Resistor Array, Metal Oxide, 4.7 Kohm \times 4	1		DEANR4J5J103
RA904	Resistor Array, Metal Oxide, 4.7 Kohm \times 4	1		DEANR4J5J103
RA905	Resistor Array, Metal Oxide, 4.7 Kohm \times 4	1		DEANR4J5J103
RA906	Resistor Array, Metal Oxide, 4.7 Kohm \times 4	1		DEANR4J5J103
SOCKET				
E1-1	IC, BIOS ROM, 28-pin	1		DFJS28R20Z

REF. NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
SWITCH				
SW1	Power, Push, DC 16 V, 5 A	1		DFSH1A14W
THERMISTOR				
TH1	10 Kohm, 0.3 mA at 25°C	1		DBT103J
THYRISTOR				
SC1	470 mA (RMS), 200 V	1		DED03P2JT1
TRANSISTOR				
Q1	2SB1073R, PNP type	1		2SB1073QTW 2SB1073PTW 2SB1073RTW
Q2	Resistor built-in, UN2111, PNP type	1		UN2111TW DETA114EKT97
Q3	2SB709R, PNP type, Chip	1		2SB709RTW 2SA1037KT97R
Q4	2SB1073R, PNP type	1		2SB1073QTW 2SB1073PTW 2SB1073RTW
Q5	Not used			
Q6	2SB709R, PNP type, Chip	1		2SB709RTW 2SA1037KT97R
Q7	Resistor built-in, UN2119, PNP type	1		UN2119TW DETA113ZKT97
Q8	Resistor built-in, UN2211, NPN type	1		UN2211TW DETC114EKT97
Q9	2SB1073R, PNP type	1		2SB1073QTW 2SB1073PTW 2SB1073RTW
Q10	Resistor built-in, UN2211, NPN type	1		UN2211TW DETC114EKT97
Q11	2SD1257P, NPN type	1		2SD1257P
Q12	2SA1534AR, PNP type	1		2SA1534ARTA
Q13	2SD601AR, NPN type, Chip	1		2SD601ARTW 2SC2412KT97R
Q14	2SB952P, PNP type	1		2SB952P
Q15	Resistor built-in, UN2111, PNP type	1		UN2111TW DETA114EKT97
Q16	Resistor built-in, UN2211, NPN type	1		UN2211TW DETC114EKT97
Q17	Resistor built-in, UN2111, PNP type	1		UN2111TW DETA114EKT97
Q18	Resistor built-in, UN2211, NPN type	1		UN2211TW DETC114EKT97
Q19	Resistor built-in, UN2111, PNP type	1		UN2111TW DETA114EKT97

REF. NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
Q20	2SB952P, PNP type	1		2SB952P
Q21	Not used			
Q22	Resistor built-in, UN2119, PNP type	1		UN2119TW DETA113ZKT97
Q23	2SD1257P, NPN type	1		2SD1257P
Q24-100	Not used			
Q101	Resistor built-in, UN2119, PNP type	1		UN2119TW DETA113ZKT97
Q102	Resistor built-in, UN2119, PNP type	1		UN2119TW DETA113ZKT97
Q103-600	Not used			
Q601	Resistor built-in, UN211F, PNP type	1		UN211FTW DETA143XKT97
Q602	2SB710AR, PNP type	1		2SB710ARTW 2SA1036KF TAE
Q603	Resistor built-in, UN221E, NPN type	1		UN221ETW DETC144WKT97

LED PCB Assembly Parts List

REF. NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
E2	Ass'y, PCB, LED	1		DFWV48C144ZA
LED				
LD1	LED, Amber	1		DEDAY5551KS

LCD Contrast Control PCB Assembly Parts List

REF. NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
E3	Ass'y, PCB, LCD Contrast	1		DFWV48C145ZA
CONNECTOR				
CN1-4 CN5	Not used Male, 2-pin	1		DFJP02C63Z
PONTETIONMETER				
VR1-5 VR6 VR7-69 VR70	Not used 5 Kohm, B-curve Not used 10 Kohm, B-curve	1 1		DEVAI3B502 EVNA1AA00B14
RESISTOR				
R1-70 R71 R72 R73 R74	Not used Metal Oxide, 10.5 Kohm, 1/4 W, ±5% Not used Not used Carbon, 30 Kohm, 1/4 W, ±5%	1 1		ER0S2TKF1052 ERDS2TJ303
THERMISTOR				
TH1 TH2	Not used 10 Kohm, 0.3 mA at 25°C	1		DBT103J

LCD Unit Assembly Parts List

REF. NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
E4	Ass'y, LCD Unit, 640x200 dots (Non-repairable)	1		DFWV08A004ZA

Floppy Disk Drive Parts List

REF. NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
E5	Ass'y, Floppy Disk Drive	1		EME-213AMC
1	Cover, Shield, Metal	1		EME0SCE1
2	Ass'y, Motor, Spindle	1		EME0MMF2
3	Spring, Disk Holder Latch	1		EME0BNH1
4	Spring, Disk Holder Lever	1		EME0BNT1
5	Latch, Disk Holder	1		EME0SPB1
6	Ass'y, Disk Holder	1		EME0LUE1
7	Spring, Flat	1		EME0SBC1
8	Lid, Disk Insertion	1		EME0CVB1
9	Actuator	1		EME0ATB1
10	Spring, Helical Torsion	1		EME0BHF1
11	Ass'y, Read/Write Head	1		DFWV27A0004
12	Spacer, Retainer	2		EME0SSB1
13	Stator, Head Spacing Motor	1		EME0STE2
14	Spiral Shaft, Head Spacing Motor	1		EME0SHD1
15	Ass'y, Chassis	1		EME0CHH1
16	Retainer, FDD Unit	2		EME0TKC1
17	Shaft, Read/Write Head	1		EME0GJB1
18	Spring, Disk Holder	2		EME0BNE1
19	Ass'y, PCB, Main	1		EME0PBF9
CAPACITOR				
C1	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUM1E104ZFG
C2	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUM1E104ZFG
C3	Ceramic, Chip, 680 pF, \pm 5%, 50 V	1		ECUM1H681JCG
C4	Ceramic, Chip, 1000 pF, \pm 5%, 50 V	1		ECUM1H102JCG
C5	Ceramic, Chip, 2700 pF, \pm 10%, 50 V	1		ECUM1H272KBN
C6	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUM1E104ZFG
C7	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUM1E104ZFG
C8	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUM1E104ZFG
C9	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUM1E104ZFG
C10	Ceramic, Chip, 470 pF, \pm 5%, 50 V	1		ECUM1H471JCG
C11	Ceramic, Chip, 470 pF, \pm 5%, 50 V	1		ECUM1H471JCG
C12	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUM1E104ZFG
C13-15	Not used			
C16	Ceramic, Chip, 0.1 μ F, +80%, -20%, 25 V	1		ECUM1E104ZFG
C17	Ceramic, Chip, 0.022 μ F, \pm 10%, 50 V	1		ECUM1H223KBN
C18	Ceramic, Chip, 0.022 μ F, \pm 10%, 50 V	1		ECUM1H223KBN
C19	Electrolytic, 1 μ F, \pm 20%, 50 V	1		ECEA1HKS010I
C20	Electrolytic, 47 μ F, \pm 20%, 6.3 V	1		ECEA0JK470I
C21	Ceramic, Chip, 0.1 μ F, +80%, -20%, Chip	1		ECUM1E104ZFG
C22	Electrolytic, 220 μ F, \pm 10%, 6.3 V	1		ECEA0JK221I
C23-25	Not used			
C26	Ceramic, Chip, 0.1 μ F, +80%, -20%, Chip	1		ECUM1E104ZFG
COIL INDUCTOR				
L1	820 μ H	1		ELEBT821JA
L2	820 μ H	1		ELEBT821JA

REF. NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
CONNECTOR				
CN1	Female, Head, 4-pin	1		008370041
CN2	Female, Head, 4-pin	1		008370041
CN3	Female, Stepper, 4-pin	1		EMCS0450Z
CN4	Female, Spindle Motor, 2-pin	1		52B-PHKS
J1	Female, Interface, 24-pin	1		FH324S1-25DS
IC				
IC1	M52819FP, FDD Read/Write Amp, 28-pin, SOP	1		M52819FP
IC2	MH008, Gate Array, 44-pin	1		MH008
IC3	μPC358G2, Dual Operational Amp, 8-pin, SOP	1		μPC358G2
IC4	TA7774E, Bipolar, Stepping Motor, 16-pin, DIP	1		TA7774E
JUMPER				
JPD0	Chip	1		ERJ6GMY0R00W
JPSH	Chip	1		ERJ6GMY0R00W
OSCILLATOR				
XT1	Ceramic, 460 KHz	1		EF0A460K06B
RESISTOR				
R1	Metal Oxide, Chip, 680 ohms, 1/16 W, ±5%	1		ERJ6GMYJ681W
R2	Metal Oxide, Chip, 680 ohms, 1/16 W, ±5%	1		ERJ6GMYJ681W
R3	Metal Oxide, Chip, 1.3 Kohms, 1/16 W, ±5%	1		ERJ6GMYJ132W
R4	Metal Oxide, Chip, 91 ohms, 1/16 W, ±5%	1		ERJ6GMYJ910W
R5	Metal Oxide, Chip, 4.7 Kohms, 1/16 W, ±5%	1		ERJ6GMYJ472W
R6	Metal Oxide, Chip, 4.7 Kohms, 1/16 W, ±5%	1		ERJ6GMYJ472W
R7	Metal Oxide, Chip, 560 ohms, 1/16 W, ±5%	1		ERJ6GMYJ561W
R8	Metal Oxide, Chip, 560 ohms, 1/16 W, ±5%	1		ERJ6GMYJ561W
R9	Metal Oxide, Chip, 3.6 Kohms, 1/16 W, ±5%	1		ERJ6GMYJ362W
R10	Metal Oxide, Chip, 33 Kohms, 1/16 W, ±5%	1		ERJ6GMYJ333W
R11	Metal Oxide, Chip, 4.7 Kohms, 1/16 W, ±5%	1		ERJ6GMYJ472W
R12	Metal Oxide, Chip, 750 ohms, 1/16 W, ±5%	1		ERJ6GMYJ751W
R13	Metal Oxide, Chip, 18 Kohms, 1/16 W, ±5%	1		ERJ6GMYJ683W
R14	Metal Oxide, Chip, 1.5 Kohms, 1/16 W, ±5%	1		ERJ6GMYJ152W
R15	Metal Oxide, Chip, 1.5 Kohms, 1/16 W, ±5%	1		ERJ6GMYJ152W
R16	Metal Oxide, Chip, 390 ohms, 1/16 W, ±5%	1		ERJ6GMYJ391W
R17	Metal Oxide, Chip, 390 ohms, 1/16 W, ±5%	1		ERJ6GMYJ391W
R18	Metal Oxide, Chip, 24 Kohms, 1/16 W, ±5%	1		ERJ6GMYJ243W
R19	Metal Oxide, Chip, 1 Kohms, 1/16 W, ±5%	1		ERJ6GMYJ102W
R20	Metal Oxide, Chip, 22 Kohms, 1/16 W, ±5%	1		ERJ6GMYJ223W
R21	Metal Oxide, Chip, 22 Kohms, 1/16 W, ±5%	1		ERJ6GMYJ223W
R22	Metal Oxide, Chip, 2.2 Kohms, 1/16 W, ±5%	1		ERJ6GMYJ222W
R23	Metal Oxide, Chip, 10 Kohms, 1/16 W, ±5%	1		ERJ6GMYJ103W
R24	Metal Oxide, Chip, 3.9 Kohms, 1/16 W, ±5%	1		ERJ6GMYJ392W
R25	Metal Oxide, Chip, 120 Kohms, 1/16 W, ±5%	1		ERJ6GMYJ124W
R26	Metal Oxide, Chip, 120 Kohms, 1/16 W, ±5%	1		ERJ6GMYJ124W
R27	Metal Oxide, Chip, 470 Kohms, 1/16 W, ±5%	1		ERJ6GMYJ474W

REF. NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
R28	Metal Oxide, Chip, 330 Kohms, 1/16 W, ±5%	1		ERJ6GMYJ334W
R29	Metal Oxide, Chip, 150 Kohms, 1/16 W, ±5%	1		ERJ6GMYJ154W
R30	Metal Oxide, Chip, 12 Kohms, 1/16 W, ±5%	1		ERJ6GMYJ123W
R31	Metal Oxide, Chip, 5.6 Kohms, 1/16 W, ±5%	1		ERJ6GMYJ562W
R32	Metal Oxide, Chip, 18 Kohms, 1/16 W, ±5%	1		ERJ6GMYJ183W
R33	Metal Oxide, Chip, 1 ohm, 1/16 W, ±10%	1		ERJ6GMYK1R0W
R34	Metal Oxide, Chip, 1 ohm, 1/16 W, ±10%	1		ERJ6GMYK1R0W
R35	Metal Oxide, Chip, 1 ohm, 1/16 W, ±10%	1		ERJ6GCYK1R0W
R36	Metal Oxide, Chip, 100 Kohms, 1/16 W, ±5%	1		ERJ6GMYJ104W
R37	Metal Oxide, Chip, 100 Kohms, 1/16 W, ±5%	1		ERJ6GMYJ104W
R38	Metal Oxide, Chip, 100 Kohms, 1/16 W, ±5%	1		ERJ6GMYJ104W
R39	Metal Oxide, Chip, 100 Kohms, 1/16 W, ±5%	1		ERJ6GMYJ104W
R40	Metal Oxide, Chip, 100 Kohms, 1/16 W, ±5%	1		ERJ6GMYJ104W
RESISTOR ARRAY				
RB1	Resistor Array, 1 Kohms, 200 mW, ±5%, 7-pin	1		EXB-F7E102J
SWITCH				
SW1	ON/OFF, Disk In	1		ESE-15307
SW2	ON/OFF, Write Protect	1		ESE-15307
TRANSISTOR				
Q1	Resistor Built-in, UN2121, PNP type	1		UN2121-PSK
Q2	Resistor Built-in, UN2111, PNP type	1		UN2111-PSK
Q3	Resistor Built-in, 2SD973, NPN type	1		2SD973
20	Ass'y, PCB, LED Indicator	1		EME0PBH6
DIODE				
LED1	LED, Sunset Orange	1		GL3HS44
21	Ass'y, PCB, Track zero, Sensor	1		EME0PBH4
PHOTO COUPLER				
PH1	Photo Coupler	1		GP1S22
22	Holder, Index Timing Sensor	1		EME0MHC1
23	Ass'y, PCB, Index Timing Sensor	1		EME0PBH5
PHOTO COUPLER				
PH2	Photo Coupler	1		GP1S22
24	Belt, Urethane Rubber, 2.8 mm (W)×0.4 mm (T)×60 mm (Dia)	1		EME0BRE1
25	Holder, Track zero Sensor	1		EME0NHB1
26	Bearing, Ball, Steel, 1.5 mm(Dia)	1		EME0SBC1
27	Screw, Pan Head with Washer and Spring Washer, M2.6×5 mm	4		XYN26+C5FU
28	Screw, Truss Head, M2.6×5 mm	2		XST26+5FU
29	Screw, Pan Head with Washer and Spring Washer, M2.6×6 mm	1		XYN26+C6FU
30	Not used			
31	Screw, Flush Head, M2.6×5 mm	2		XSS26+5FU

REF. NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
32	Screw, Pan Head with Washer and Spring Washer, M2.6x4 mm	2		XYN26+F4FU
33	Screw, Pan Head with Washer and Spring Washer, M2.6x8 mm	1		XYN26+J8FU

Keyboard Unit Assembly Parts List

REF. NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
E6	Ass'y, Keyboard, USA	1		DFSX1A02Z
KEYTOP				
1	Keytop, Esc	1		DFWV70C3206
2	Keytop, F1	1		DFWV70C3207
3	Keytop, F2	1		DFWV70C3208
4	Keytop, F3	1		DFWV70C3209
5	Keytop, F4	1		DFWV70C3210
6	Keytop, F5	1		DFWV70C3211
7	Keytop, F6	1		DFWV70C3212
8	Keytop, F7	1		DFWV70C3213
9	Keytop, F8	1		DFWV70C3214
10	Keytop, F9	1		DFWV70C3215
11	Keytop, F10	1		DFWV70C3216
12	Keytop, F11	1		DFWV70C3217
13	Keytop, F12	1		DFWV70C3218
14	Keytop, NumLk	1		DFWV70C3219
15	Keytop, ScrLk	1		DFWV70C3220
16	Keytop, PrtSc	1		DFWV70C3221
17	Keytop, KeyPad	1		DFWV70C3222
18	Keytop, ! 1	1		DFWV70C3223
19	Keytop, @ 2	1		DFWV70C3224
20	Keytop, # 3	1		DFWV70C3225
21	Keytop, \$ 4	1		DFWV70C3226
22	Keytop, % 5	1		DFWV70C3227
23	Keytop, ^ 6	1		DFWV70C3228
24	Keytop, & 7	1		DFWV70C3229
25	Keytop, * 8	1		DFWV70C3230
26	Keytop, (9	1		DFWV70C3231
27	Keytop,) 0	1		DFWV70C3232
28	Keytop, _ -	1		DFWV70C3233
29	Keytop, + =	1		DFWV70C3234
30	Keytop, ← (Back Space)	1		DFWV70C3235
31	Keytop, Home	1		DFWV70C3236
32	Keytop, ← → (Tab Key)	1		DFWV70C3237
33	Keytop, Q	1		DFWV70C3238
34	Keytop, W	1		DFWV70C3239
35	Keytop, E	1		DFWV70C3240
36	Keytop, R	1		DFWV70C3241
37	Keytop, T	1		DFWV70C3242
38	Keytop, Y	1		DFWV70C3243
39	Keytop, U	1		DFWV70C3244
40	Keytop, I	1		DFWV70C3245
41	Keytop, O	1		DFWV70C3246
42	Keytop, P	1		DFWV70C3247
43	Keytop, { [1		DFWV70C3248
44	Keytop, }]	1		DFWV70C3249
45	Keytop, \	1		DFWV70C3250
46	Keytop, PgUp	1		DFWV70C3251
47	Keytop, CapsLock	1		DFWV70C3252
48	Keytop, A	1		DFWV70C3253

REF. NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
49	Keytop, S	1		DFWV70C3254
50	Keytop, D	1		DFWV70C3255
51	Keytop, F	1		DFWV70C3256
52	Keytop, G	1		DFWV70C3257
53	Keytop, H	1		DFWV70C3258
54	Keytop, J	1		DFWV70C3259
55	Keytop, K	1		DFWV70C3260
56	Keytop, L	1		DFWV70C3261
57	Keytop, ; :	1		DFWV70C3262
58	Keytop, " ' "	1		DFWV70C3263
59	Keytop, Enter	1		DFWV70C3264
60	Keytop, PgDn	1		DFWV70C3265
61	Keytop, Shift (Left)	1		DFWV70C3266
62	Keytop, Z	1		DFWV70C3267
63	Keytop, X	1		DFWV70C3268
64	Keytop, C	1		DFWV70C3269
65	Keytop, V	1		DFWV70C3270
66	Keytop, B	1		DFWV70C3271
67	Keytop, N	1		DFWV70C3272
68	Keytop, M	1		DFWV70C3273
69	Keytop, < ,	1		DFWV70C3274
70	Keytop, > .	1		DFWV70C3275
71	Keytop, ? /	1		DFWV70C3276
72	Keytop, Shift (Right)	1		DFWV70C3277
73	Keytop, ↑	1		DFWV70C3278
74	Keytop, End	1		DFWV70C3279
75	Keytop, Ctrl	1		DFWV70C3280
76	Keytop, Fn	1		DFWV70C3281
77	Keytop, Alt	1		DFWV70C3282
78	Keytop, ~ `	1		DFWV70C3283
79	Keytop, Ins	1		DFWV70C3284
80	Keytop, Del	1		DFWV70C3285
81	Keytop, ←	1		DFWV70C3286
82	Keytop, ↓	1		DFWV70C3287
83	Keytop, →	1		DFWV70C3288
84	Keytop, Space	1		DFWV70C3289
E6-1	Switch, Membrane, Keyboard	1		DFWV48C146Z
E6-2	Spring, Rubber, Keytop	84		DFWV65D0022
E6-3	Rod, CapsLock, ←, Enter	3		DFWV71H0025
E6-4	Rod, Shift (Left)	1		DFWV71H0026
E6-5	Rod, SpaceBar	1		DFWV71H0027
E6-6	Screw, Cross-recessed Flush Head Tapping, Keyboard, M2x5 mm	21		DFWV50B0006
E6-7	Spacer	1		DFWV65C0177

Mechanical and Assembly Parts List

REF. NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
K1	Case, Top, Beige	1		DFKM0092Z0
K2	Screw, Blazer Head, Tapping, M3x10 mm	1		XTV3+10GFN
K3	Cover, Hinge, Left, Beige	1		DFKE0145Z0
K4	Cover, Hinge, Right, Beige	1		DFKE0146Z0
K5	Binder, Cable	1		RHR166Z
K6	Cover, Battery, Beige	1		DFKK0014Z0
K8	Seal, Screw, Beige	2		DFHG917Z1
K9	Frame, LCD, Plastic	1		DFKF0077Y0
K10	Shield Plate, LCD	1		DFMC0224Z1
K11	Screw, Pan Head with Washer and Spring Washer, M3x8 mm	3		XYN3+J8
K12	Knob, Contrast, LCD, Beige	1		DFBD0024Z1
K13	Ass'y, Hinge, Left (Non-repairable)	1		DFWV65A0164
K14	Ass'y, Hinge, Right (Non-repairable)	1		DFWV65A0165
K16	Case, LCD, Beige	1		DFKM0094Z0
K17	Knob, Power Switch	1		DFBC0052Z2
K18	Frame, Connector, Metal	1		DFUA0092Z
K19	Cover, MODEM, Metal, Rear	1		DFGX0077Z
K20	Screw, Pan Head with Washer and Spring Washer, M3x6 mm	4		XYN3+J6
K21	Shield Plate, Main PCB, Top	1		DFMC0221Z
K22	Shield Plate, Main PCB, Bottom	1		DFMC0222Z
K23	Protector, Cable	2		DFHR5159Z
K24	Frame, FDD	1		DFMD2028Z
K25	Cushion, Battery, Black	1		DFHR8053Z
K26	Cushion, Battery, Black	1		DFHR8052Z
K27	Cushion, Core, Black	1		DFHR8053Z
K28	Shield Plate, MODEM, Top	1		DFMC0223Z
K29	Cover, Parallel & Serial Connectors, Rear, Beige	1		DFGX0076Z0
K30	Ass'y, Case, Bottom, Beige	1		DFWV80C0121
	•Case, Bottom, Beige	1		DFKF0080Z0
	•Knob, Lock, Beige	1		DFBD0026Z1
	•Hook, Display, Beige	1		DFHR5154Z1
	•Spring, Coil, Hook	1		DFUW0032Z
	•Foot, Rubber, 5mm (Dia), Black	2		RHG338Z0
	•Window, LED, Floppy Disk Drive Sunset Orange	1		ME13TB53A
K31	Screw, Blazer Head, Tapping, M3x8 mm	1		XTV3+8G
K32	Shield Plate, FDD	1		DFMC0239Z
K33	Sheet, Insulation, FDD	1		DFMX0154Z
K34	Screw, Pan Head with Washer and Spring Washer, M3x6 mm	2		XYN3+C6FN
K36	Spring Washer	2		XWA3B

Accessories

REF. NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
E7	Battery, Rechargeable, Lead-acid 6 V, 1.8 AH (with Fuse)	1		UP6V1R8AJH
E7-1	Fuse, Battery, Rechargeable, Fast Blow, with Pigtail, 4 A, 125 V 2.5 mm (Dia)×10 mm (L)	1		DFWV38A0031
E8	AC Adapter, 85–132 Vac (INPUT) 9.5 Vdc (OUTPUT), Max 2.1 A	1		FT-AA96M1
	Floppy Disk, System, MS-DOS	1		DFJN168ZA
	Floppy Disk, DESKMATE (1 of 2)	1		DFJN169ZA
	Floppy Disk, DESKMATE (2 of 2)	1		DFJN170ZA

Hardware Kit

REF. NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
	Hardware Kit	1		DFWV95C0058
K2	Screw, Blazer Head, Tapping, M3×10 mm	2		XTV3+10GFN
K7	Screw, Binding Head, M3×8 mm	4		XSB3+8FN
K15	Screw, Pan Head with Washer and Spring Washer, M2.6×6 mm	4		XYN26+C6
K20	Screw, Pan Head with Washer and Spring Washer, M3×6 mm	5		XYN3+J6
K31	Screw, Blazer Head, Tapping, M3×8 mm	11		XTV3+8G
K35	Screw, Pan Head with Washer and Spring Washer, M3×8 mm	1		XYN3+J8

3. Mechanical Specifications

Item	Dimensions	Unit
Module size	9.4 (W)×5.8 (H)×0.2 (D) max.	inches
	238 (W)×147 (H)×6.0 (D) max.	mm
Effective Viewing Area	7.8 (W)×4.8 (H)	inches
	197 (W)×121 (H)	mm
Weight	Approx. 0.42	lbs
	Approx. 190	grams

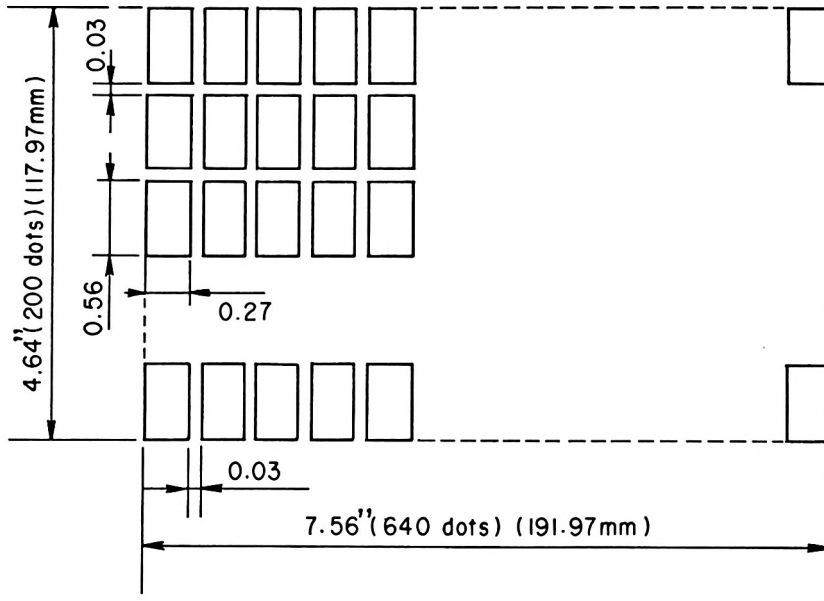


Figure A-2. Dot Dimensional Drawing

4. Electrical Specifications

4-1 Absolute Maximum Rating

Item	Symbol	Minimum	Maximum	Unit
Supply voltage for logic circuit	VDD-VSS	0	+6.0	V
Supply voltage for LCD driving	VDD-VEE	0	+28.0	V
Input Voltage	VIN	0	VDD	V
Storage temperature	Tstg	-13	140	°F
		-25	+60	°C
Operating temperature	Topr	32	113	°F
		0	+45	°C

4-2 Electrical Characteristics

Item	Symbol	Test Condition	Minimum	Typical	Maximum	Unit
Supply voltage for logic circuit	VDD-VSS					
Supply voltage for LCD driving	VDD-VEE					
Input voltage H level	VIH	VDD=5.0 V±5%	0.8 VDD	—	VDD	V
Input voltage L level	VIL	VDD=5.0 V±5%	0	—	0.2 VDD	V
Current drain for logic circuit	IDD	VDD=5.0V	—	20.0	28.0	mA
		VDD-V0=22.7 V VEE=-21 V Ta=25°C F=75 Hz High Freq.- Patter	—	16.0	22.0	mA
Current drain for LCD driving circuit	IEE	(Same above)	—	16.0	22.0	mA
Supply voltage for LCD driving	VDD-V0	(See Note)	19.6	22.7	25.3	V

Note: The viewing angle for the maximum contrast can be set by changing the driving voltage (VDD-V0) for the LCD.

4-3 V0 Adjusting Circuit

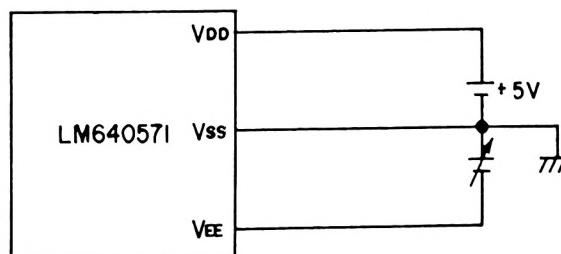


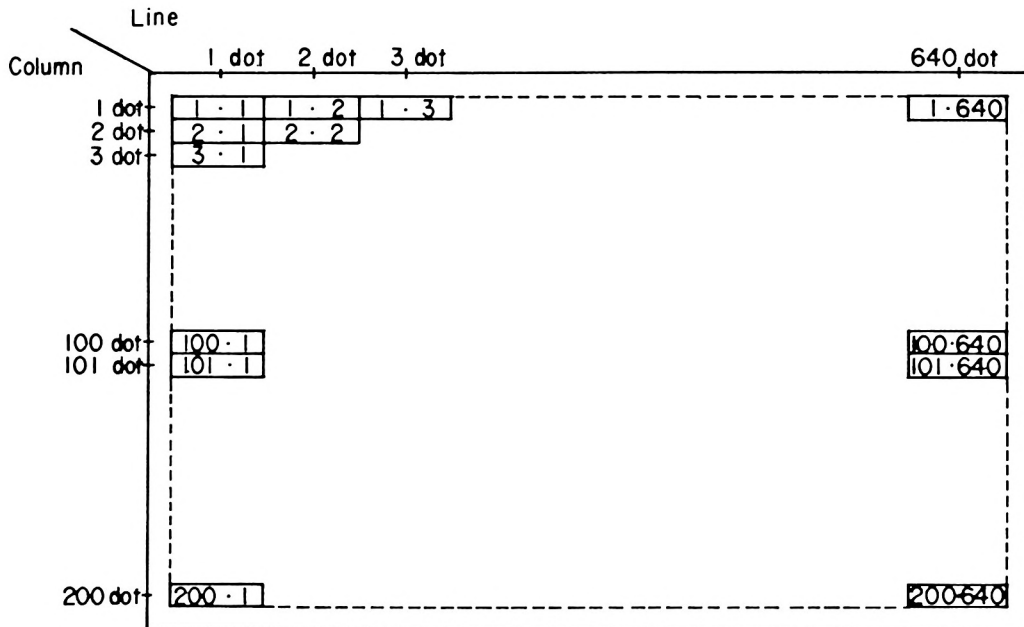
Figure A-3. V0 Adjusting Circuit

5. Interface Specifications

5-1 Terminal Pin Assignment

Pin No.	Symbol	Description	Effective Data Signal
1	S	Start signal for scan	H
2	CP1	Latch signal for input data	H→L
3	CP2	Clock signal for data input	H→L
4	NC	Not connected	—
5	VDD	+5 V (Supply voltage for logic circuit)	—
6	VSS	GND	—
7	VEE	Supply voltage for LCD driving circuit	—
8	D0	Display data signal (for upper screen)	H (ON) L (OFF)
9	D1	Display data signal (for upper screen)	H (ON) L (OFF)
10	D2	Display data signal (for upper screen)	H (ON) L (OFF)
11	D3	Display data signal (for upper screen)	H (ON) L (OFF)

5-2 Relationships of Display Data Signal and LCD Screen Division



Note: "1-2" denotes the location of display dot at 1st dot of column and 2nd dot of line.

Figure A-4. LCD Screen

5-3 Data Input Timing Chart

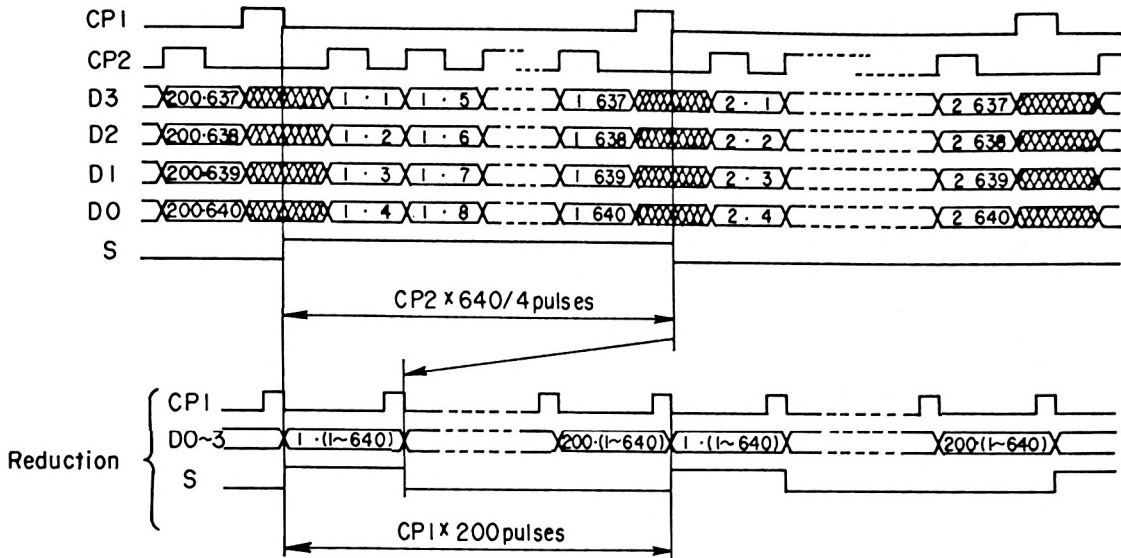


Figure A-5. Data Input Timing Chart

5-4 Interface Timing Chart

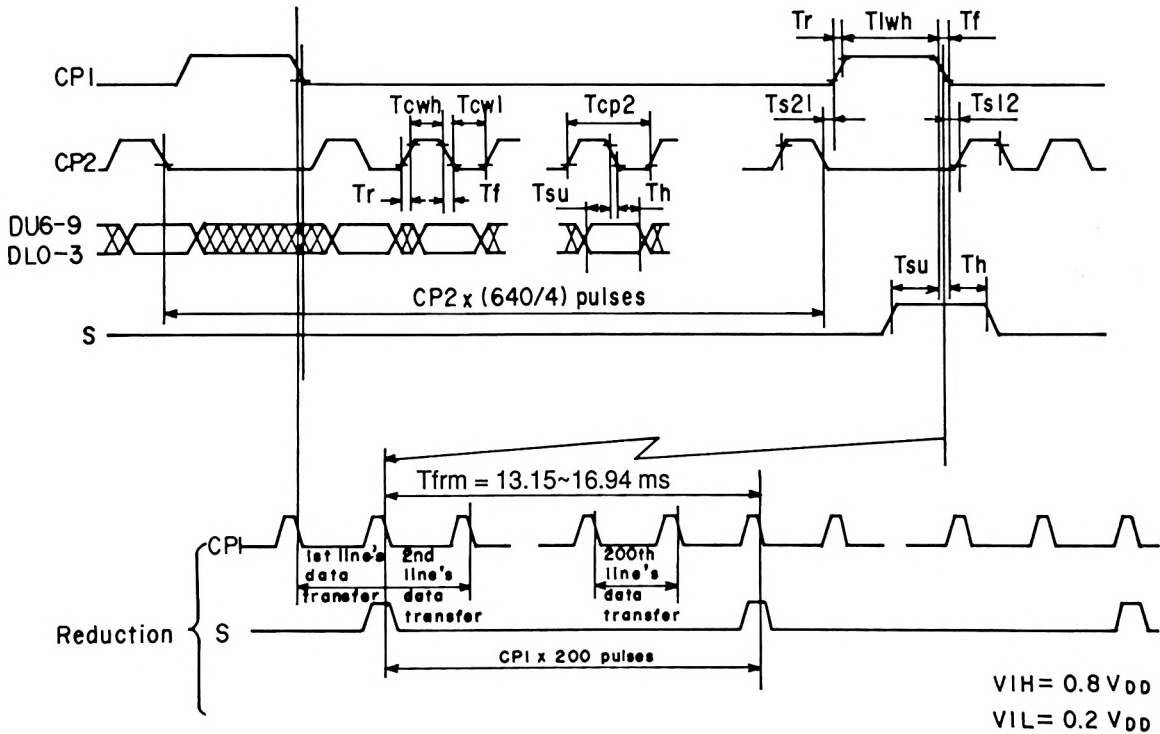


Figure A-6. Interface Timing Chart

5-5 Interface Timing Table

Interface Timing

Item	Symbol	Min.	Typ.	Max.	Unit
Frame cycle	Tfrm	13.1	—	16.94	ms
Clock cycle	Tcp2	342	—	—	ns
"H" level clock width	Tcwh	145	—	—	ns
"L" level clock width	Tcwl	145	—	—	ns
"H" level latch clock width	Tlwh	130	—	—	ns
Data set up time	Tsu	70	—	—	ns
Data hold time	Th	60	—	—	ns
Clock margin time (between CP2 fall & CP1 rise)	Ts21	0	—	—	ns
Clock margin time (between CP1 fall & CP2 rise)	Ts12	0	—	—	ns
Clock rise & fall time	Tr, Tf	—	—	50	ns

6. Precautions in Use

6-1 Precautions for handling

- (1) The polarizer is quite susceptible to scratches. Handle it very carefully. Do not handle it with metallic tweezers nor press nor rub it.
- (2) Do not get the display face stained.
If the surface is dirty, wipe it off lightly with a cotton swab or a piece of soft cloth. Never use organic solvents including acetone, toluene, ethanol, and isopropyl alcohol; they would damage the surface.
- (3) Do not allow saliva or water to remain on the surface for long; it might cause a local deformation or discoloration.
- (4) If the LCD breaks and the liquid crystal comes out, never get the liquid crystal in your mouth. If it sticks to your skin or clothing, wash it off immediately with soap and water.

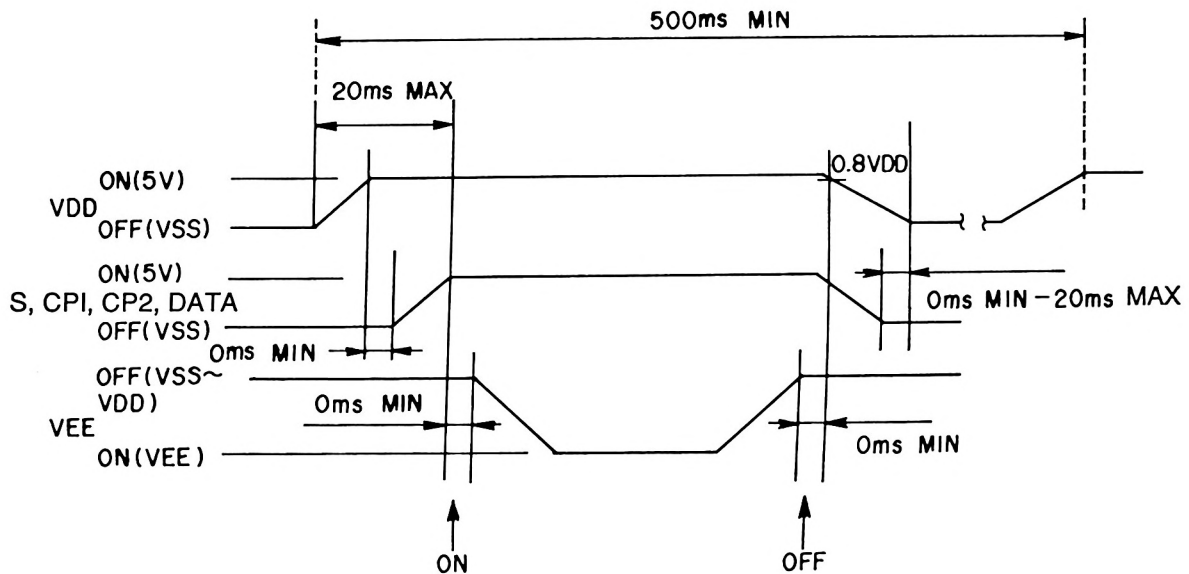
6-2 Installation

- (1) The C-MOS LSIs mounted on the PCB are very susceptible to static electricity. To protect them from static electricity which your body and clothing collect, connect your body to ground via a resistor of a few Mohms so that the electricity can be discharged. Connect the resistor close to your body in the grounding line and protect yourself from any electric shock hazards.

- (2) Neither bend nor twist the module excessively when installing it. Otherwise the device might break or the circuits may fail.

6-3 Operational precautions

- (1) The ICs will break down if the drive voltage exceeds the limit. Make sure of electrical specifications, particularly the supply voltage.
- (2) The contrast of the LCD varies with the viewing angle, ambient temperature and drive voltage. Adjust the drive voltage for the best contrast with the LCD Contrast Adjustment Knob.
- (3) In order to prevent IC latch-up and DC voltage on the LCD Panel when turning power ON or OFF, following the power sequence timing chart as shown in Figure A-7 is recommended.



ON: When power is turned "ON".
 OFF: When power is turned "OFF".

Figure A-7. Recommended Power Sequence

6-4 Storage

- (1) Avoid high temperature and high humidity. The temperature should be -13 through 140°F (-25°C through $+60^{\circ}\text{C}$) and the humidity under 95%RH (at $T_a \leq 40^{\circ}\text{C}$).
- (2) Store the module in a dark place, away from direct sunlight and fluorescent lighting, etc.
- (3) Store the module in its original carton or in a similar container that provides the same kind of protection.

Appendix B. 3.5-inch FDD Specifications

FDD Specifications

1.0 Outline of the Product

The EME-213 series (double-sided 3.5-inch floppy-disk drive) is a high-performance floppy-disk drive which has been developed with main design for low profile, light weight, high reliability and low price.

Features of this product:

- (1) Low profile 1-inch (25.4 mm) thickness and light weight 0.71 lbs (320 g).
- (2) Low power consumption
1.5 W or less at standard operation with a single power source of +5V ($\pm 10\%$), and 30 mW or less at stand-by, so that battery driving is possible.
- (3) High reliability
 - Simple and strong mechanism with the company's original front-fulcrum-turning-type loading unit and aluminum die-cast construction.
 - Belt drive system by a high-performance DC power motor (2000 hours or longer life guaranteed)
 - No adjustment required of the number of revolutions and remarkable upgrading of the load variation and chronological change characteristics by the PLL quartz lock type spindle motor control.
 - Big reduction in the number of circuit components by the employment of a newly developed LSI.

2.0 Product Specifications

2.1 Performance

ITEMS		FM	MFM	
Storage Capacity	Per disk	Unformat (KB)	500	1000
		Format (KB) *1	368	737
	Per track	Unformat (Bytes)	3125	6250
		Format (Bytes) *1	2304	4608
Recording density	Innermost track recording density (BPI)		4358	8717
	Data transfer rate (Kbit/sec)		125	250
	Number of heads		2	
	Number of tracks		160	
	Track density (TPI)		135	
Access time	Track-to-track access time (msec)		6 (min)	
	Settling time (msec)	*2	15 (min)	
	Mean access time (msec)		173	
Motor characteristics	Number of revolutions (rpm)		300	
	LSV (long-period speed variation) (%)		±1.5 (max)	
	ISV (instantaneous speed variation) (%)		±1.5 (max)	
	Motor starting time (sec)		0.4 (max)	
Ready time (sec)		1.0 (max)		

Note:

*1 This applies to 9 sectors/track. The relative position of the index signal of this drive and the head is adjusted to ±1.7 ms (max) with respect to the reference disk by converting to time. Therefore, the IBM format with long preamble portion is recommended. (An inquiry is requested when using the ISO format.)

*2 The settling time denotes the time required to be at the final stable output level ±15% after the passage of track-to-track transfer at the final step. Therefore, the time when read/write become possible (6+15 = 21 ms) from the final step pulse.

2.2 Conditions for Installation

2.2.1 Power Source Specifications

ITEMS		SPECIFICATIONS	
Voltage	Allowable voltage (at the connector on the PC board on the drive side)	+5 V±10%	
	Allowable ripple voltage	100 mVp-p	
Current drain	① At power on (stepping motor calibration)		0.74 (Peak)
	② Stand-by mode (MOTOR ON=High)	6 mA (Typ)	10 mA (Max)
	③ Read/write mode (Panasonic medium outermost track)	0.31A (Typ)	0.37A (Max)
	④ Seek mode (under motor rotation)	0.62A (Max)	1.1A (Peak)
	⑤ At motor starting (maximum value in 400 msec)		0.9A (Max)
Power consumption	Stand-by mode	30 mW (Typ)	50 mW (Max)
	Read/write mode	1.5W (Typ)	
	Seek mode	3.1W (Max)	
	At motor starting		4.5W (Max)

In order to reduce the power source load, it is recommended not to perform the step operation within 400 msec after starting the motor. It is also recommended not to start the motor within 21 ms after the step operation.

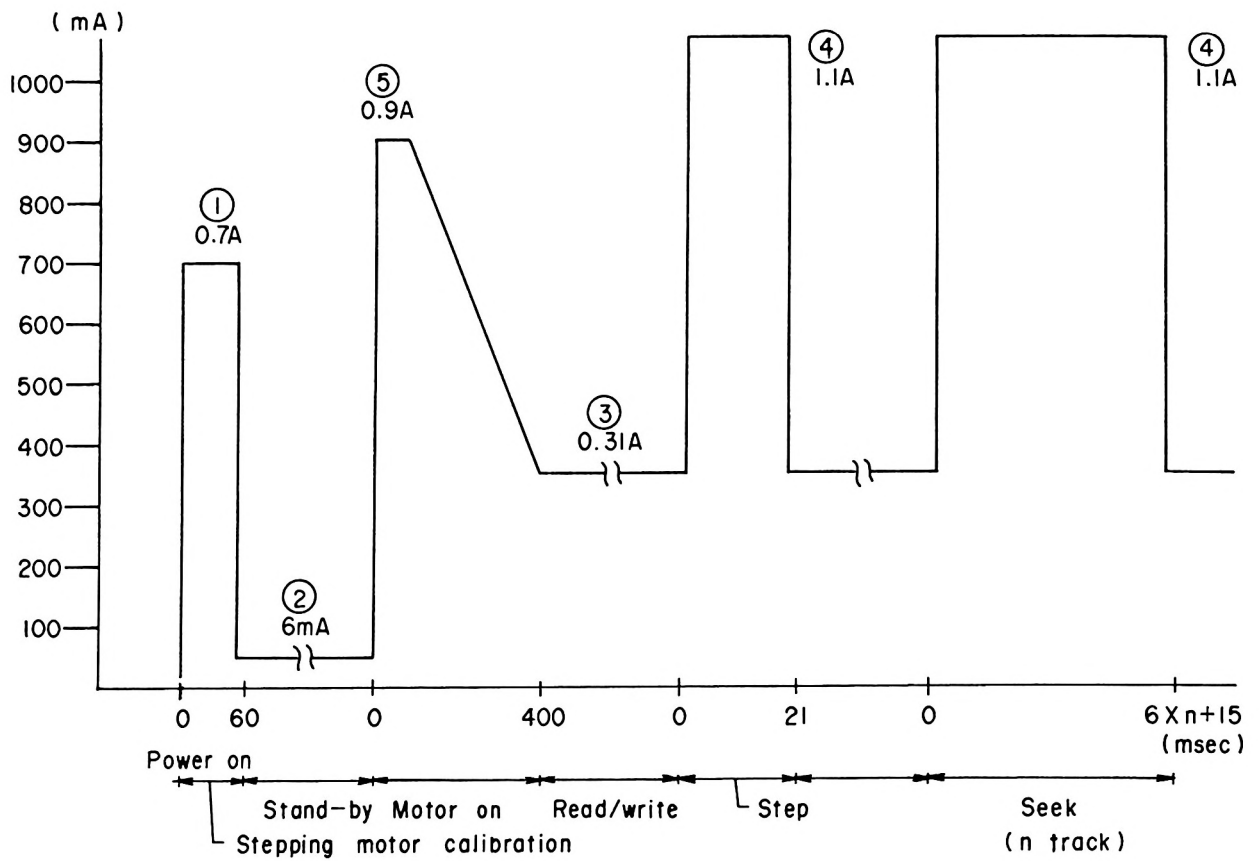


Figure 2.1 Current Drain Diagram (+5 V)

2.2.2 Environmental Conditions

ITEMS		SPECIFICATIONS		
Temperature	Under operation	41°F~115°F (5°C~46°C)		
	Under storage	-13°F~140°F (-25°C~60°C) 96 hr min.		
	Under transport	-40°F~140°F (-40°C~60°C) 96 hr min.		
	Temperature gradient	68°F/hr (20°C/hr)		
Relative humidity	Under operation	20~80% RH (No condensation)		
	Under storage/transport	5~95%RH (no condensation) 96 hr min.		
	Maximum wet-bulb temperature	29°C		
Vibration	Under operation	Acceleration	(a) 0.5G (b) 1.0G	3 mutually perpendicular directions Operation: During test, normal read/write shall be possible. No operation: after test, the specification performance shall be satisfied.
		Number of vibration	(a) 10~500 Hz (b) 10~100 Hz	
	Under storage/transport (No operation)	Acceleration	2.0G	
		Number of vibration	10~500 Hz	
Impact	Under operation	Acceleration	3.0G	3 mutually perpendicular directions Operation: During test, normal read/write shall be possible. No operation: after test, the specification performance shall be satisfied.
		Time	11 msec (Half sine wave)	
	Under storage/transport (No operation)	Acceleration	70G	
		Time	11 msec (Half sine wave)	
Packaging specification	Drop height	23 19/32 inches (60 cm), 6 faces 19 21/32 inches (50 cm), 1 corner, 3 edges	After a total of 10 drops, the specification performance shall be satisfied.	
Mounting direction/angle		3 horizontal directions, 0~+30° (See Fig. 2.2)		

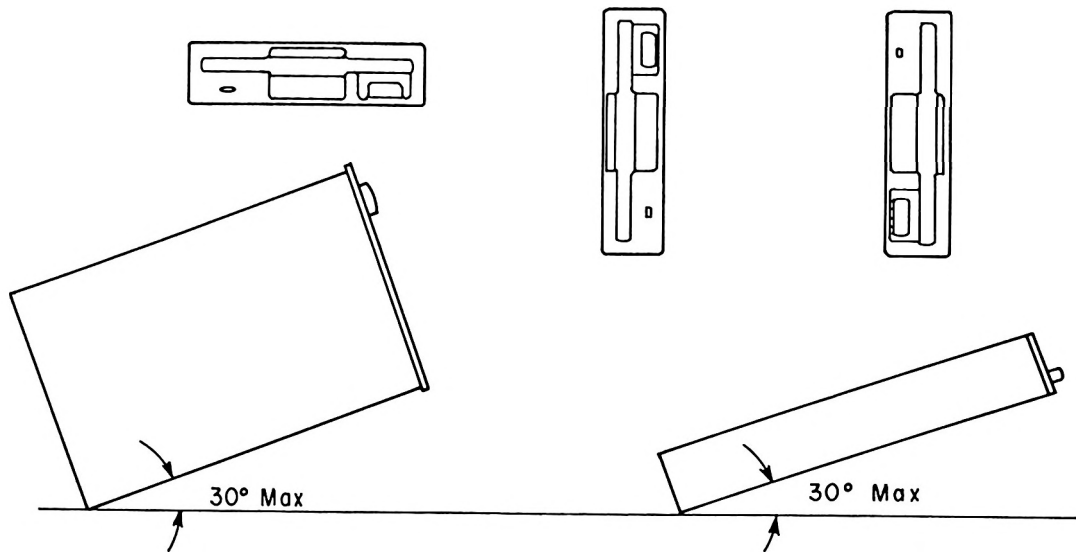


Figure 2.2 Mounting Direction and Angle

2.2.3 Others

ITEMS		SPECIFICATIONS
Shape and dimensions	Width	4 inches (101.6 mm)
	Height	1 inch (25.4 mm)
	Depth	5 23/32 inches (146 mm)
Weight		0.7 lbs. (320 g)
Disk operating force	Insertion	1.2±0.4 lbs. (550±200 g)
	Ejection	2.2±0.9 lbs. (1000±400 g)
Noise		40 dBA [at a position of 19 21/32 inches (50 cm) from the drive]
Disk projecting amount		*25/32~2 25/32 inches (20~70 mm) (at normal temperature and normal humidity in vertical direction by using Panasonic medium)
Insulation resistance		10 MΩ min. at 250V DC between power source and chassis with FG and SG open.
Dielectric withstanding voltage		DC 250V for 1 minute between power source and chassis with FG and SG open.
Temperature rise		5 degrees max. (in the condition of continuous use of the system)
Abnormal power source		In a mode other than the write mode, the record on the medium shall not be damaged when the power source is cut off.
Direction switching time		21 ms min.
Positioning accuracy (average value)		within ±20 μm, TR40, Side 0, 1, 70°F±37°F (21°C±3°C), 40~70% RH

ITEMS		SPECIFICATIONS
Electromagnetic conversion performance	Average signal output Track 00 1F (Side 0) Track 79 2F (Side 1)	2500 mV max. Differential output of self read/write TP1 and 2. 180 mV min. (TP1-GND: 50%)
	Resolution Track 79 (Side 0, 1)	55% min.
	Asymmetry Track 79 (Side 0, 1)	700 ns max. ITI-T21
	Azimuth angle	within ± 20 minutes, $70^{\circ}\text{F} \pm 37^{\circ}\text{F}$ ($21^{\circ}\text{C} \pm 3^{\circ}\text{C}$), 40-70% RH
Overall Characteristics	Time margin Self Interchange	700 ns min. 500 ns min.
	Temperature time margin Temperature interchangeability time margin at 115°F (46°C) 50%RH (or 41°F , 5°C , 50%RH) and 41°F , 5°F , 50%RH (or 115°F , 46°C , 50%RH) *with the same drive	500 ns min.
	Off-track time margin Time margin at $60\text{-}\mu\text{m}$ off-track (with the same drive)	400 ns min.

2.3 Reliability

ITEMS		SPECIFICATIONS
Mean time between failure (MTBF)		10,000 POH
Mean time to repair (MTTR)		0.5H
Drive designed life		5 years or 20,000 POH
Error rate	Soft read error *1	10^{-9} /bits
	Hard read error *2	10^{-12} /bits
	Seek error *3	10^{-6} /seeks

*1 Error that becomes readable within two retries.

*2 Error that does not become readable within two retries.

*3 Error that makes it impossible to seek the target track.

2.4 Life

ITEMS		SPECIFICATIONS
Head		10,000 hr min.
Medium (single track wear)		3,000,000 passes min.
Number of disk loading	Disk	10,000 times min.
	Drive	100,000 times min.
Seek (go/back)		3,000,000 times min.
Motor and belt		*4 2,000 hr min.

Note: *4 Environmental conditions: Normal temperature, 41°F (5°C), 40% 115°F (46°C) 80%
Operating mode: Continuous and intermittent
(10-second ON, 2-second OFF)

3.0 Interface

3.1 Signal Names and Voltage Levels

3.1.1 Input Signals

- DRIVE SELECT 0-1
- MOTOR ON
- DIRECTION SELECT
- STEP
- WRITE DATA
- WRITE GATE
- SIDE 1 SELECT

Low (true)	0.8V max.
High (false)	2.2V min.

FDD side terminator: 1 K Ω fixed.

3.1.2 Output Signals

	LOW (true)	High (false) DSEL="L"	High (false) DSEL="H"
DISK CHANGE (tri-state output)	0.4V (IOL=12 mA)	3.9V (IOH=12 mA)	High impedance
READY (tri-state output)	"	"	"
INDEX (tri-state output)	"	"	"
TRACK 00 (tri-state output)	"	"	"
WRITE PROTECT (tri-state output)	"	"	"
READ DATA (Open train output)	0.4V (IOL=6 mA)	High impedance	

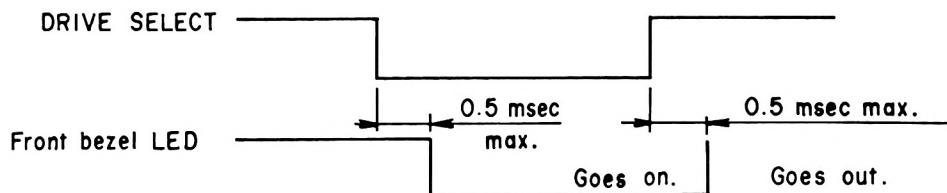
Note: The terminator on the host system side shall be 1 to 3.3 kohms.
 For the IC 74LS14 equivalent is recommended.
 The cable length shall be within 23 19/32 inches (60 cm).

3.2 Functions of the Signals

3.2.1 Input Signals

(1) DRIVE SELECT 0-1

This signal can prohibit input and output of signals other than the MOTOR ON signal. DRIVE SELECT can be set by soldering the chip jumper position on the main PC board either to JPD0 or JPD1. This setting allows selection ("LOW" true) of the drive on the host system side, so that up to 2 drives can be used by daisy chain connection. (At shipment, DS0 is selected.) By the selection of the drive, the LED on the front bezel will go on.



(2) MOTOR ON

Regardless of DRIVE SELECT, at "LOW" level of this signal, the spindle motor will start when a disk is loaded. When this signal is turned to "High" level or the disk is unloaded, the motor will stop. At "LOW" level of this signal, the ordinary mode is in effect, and at "High" level, the stand-by mode is in effect, suppressing the power consumption to about 30 mW. In the stand-by mode, the TRACK 00 output signal is effective by DRIVE SELECT.

The time from the motor on to the readable and writable state (ready state) is a maximum of 1 second.

(3) DIRECTION SELECT

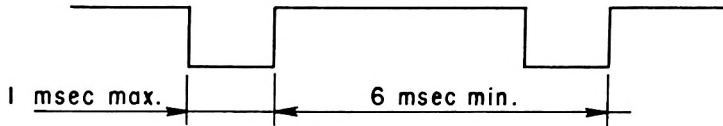
This signal designates the head moving direction when STEP signal is input.

"Low" level: Inner direction (Disk inner circumference direction)

"High" level: Outer direction (Disk outer circumference direction)

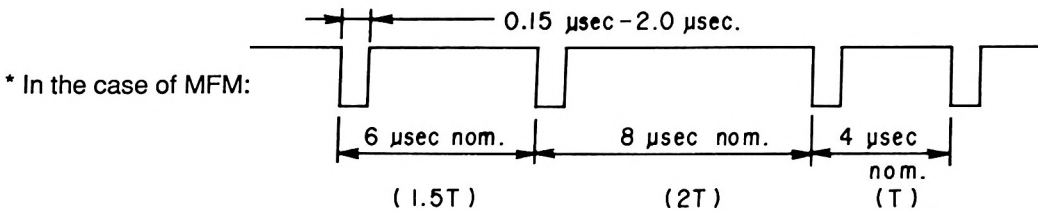
(4) STEP

This signal moves the head to the direction specified by DIRECTION SELECT signal. For the operation, the head is moved by 1 track by the pulse rise edge. The head is stabilized 21 msec after the last step pulse, and read/write operation becomes possible. This signal is ineffective when the drive is under writing operation.



(5) WRITE DATA

While WRITE GATE signal is at "Low" level, the fall edge of this signal changes the direction of the head current, causing change in the magnetizing direction of the disk face to record data.



(6) WRITE GATE

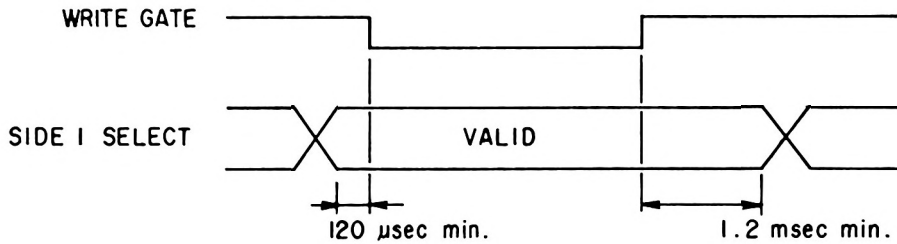
At "Low" level of this signal, writing in the disk is possible by WRITE DATA signal. Also at "High" level, read operation and step operation are possible.

(7) SIDE 1 SELECT

Head selection is performed by this signal.

"Low" level: Head 1 is selected.

"High" level: Head 0 is selected.

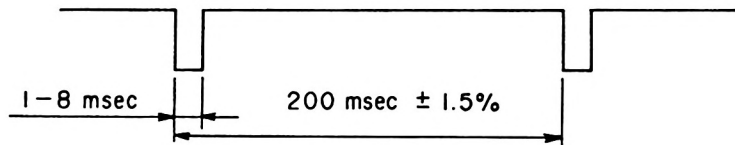


3.2.2 Output Signals

All output signals are effective at DRIVE SELECT. In case of no DRIVE SELECT, C-MOS high impedance state will result.

(1) INDEX

This signal indicates the starting of the track, and 1 pulse is output with every 1 rotation. No output is obtained when no disk is loaded. For this signal, the fall edge of the pulse shall be used.



(2) TRACK 00

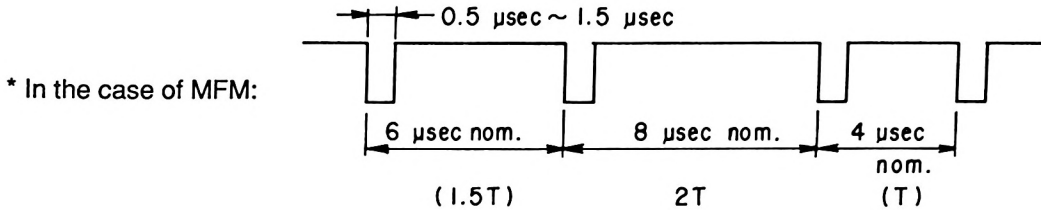
When this signal is at "Low" level, it indicates that the head is in the track 00 position (outermost track). Other than track 00, the signal is at "High" level.

(3) WRITE PROTECT

When this signal is at "Low" level, it indicates that no disk is loaded or a write-protected disk is loaded.

(4) READ DATA

This signal is the data of the inversion of the disk magnetization read out by the head. The fall edge of the pulse shall be used.



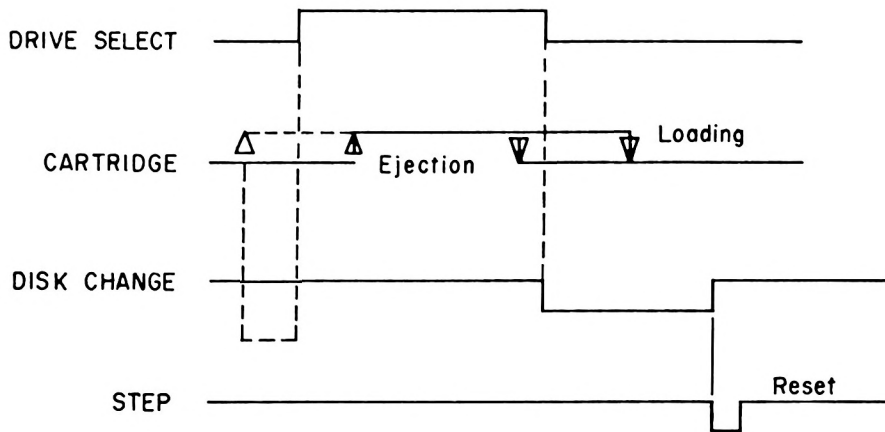
(5) READY

At "Low" level of this signal, read/write of the disk is possible. For the conditions at this time, the output is obtained within 1 second after the motor is started, when a disk has been loaded and DRIVE SELECT is in effect.

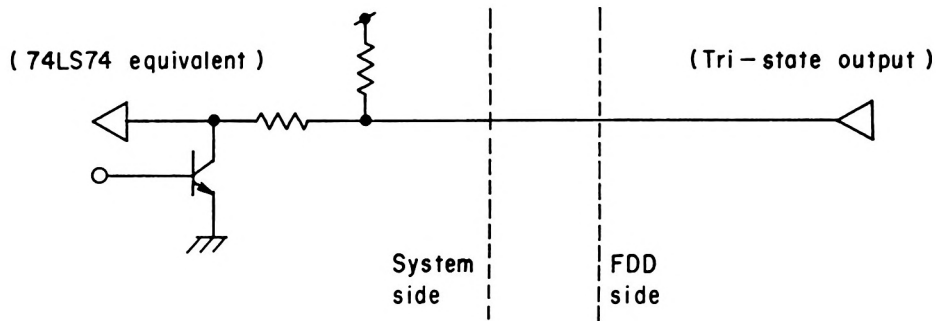
(6) DISK CHANGE

At "Low" level of this signal, it indicates that the disk is unloaded.

After a disk is loaded again, in the state of DRIVE SELECT, it is changed to "High" level by the first STEP signal.



(7) When DRIVE SELECT is at "LOW", in order to set DISK change, ready index, track 00, WRITE PROTECT output (tri-state output) is forcibly set to "LOW", the circuit setup as shown in the figure below is recommended.



3.3 Connector Pin Layout

3.3.1 Signal Connector Pin Layout

NO.	SIGNAL NAME	NO.	SIGNAL NAME
1	+5V (LOGIC C)	2	+5V (LOGIC C)
3	N.C.	4	+5V (MOTOR)
5	+5V (MOTOR)	6	READY
7	GND	8	GND
9	SIDE SELECT	10	GND
11	READ DATA	12	WRITE PROTECT
13	TRACK 00	14	WRITE GATE
15	GND	16	WRITE DATA
17	GND	18	STEP
19	DIRECTION SELECT	20	MOTOR ON
21	NC (DS1)	22	DRIVE SELECT 0
23	INDEX	24	DISK CHANGE

Applicable connector: CL586-0060-0 (Hirose)

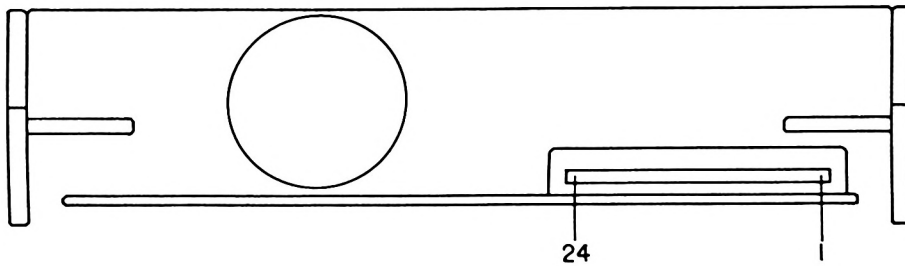
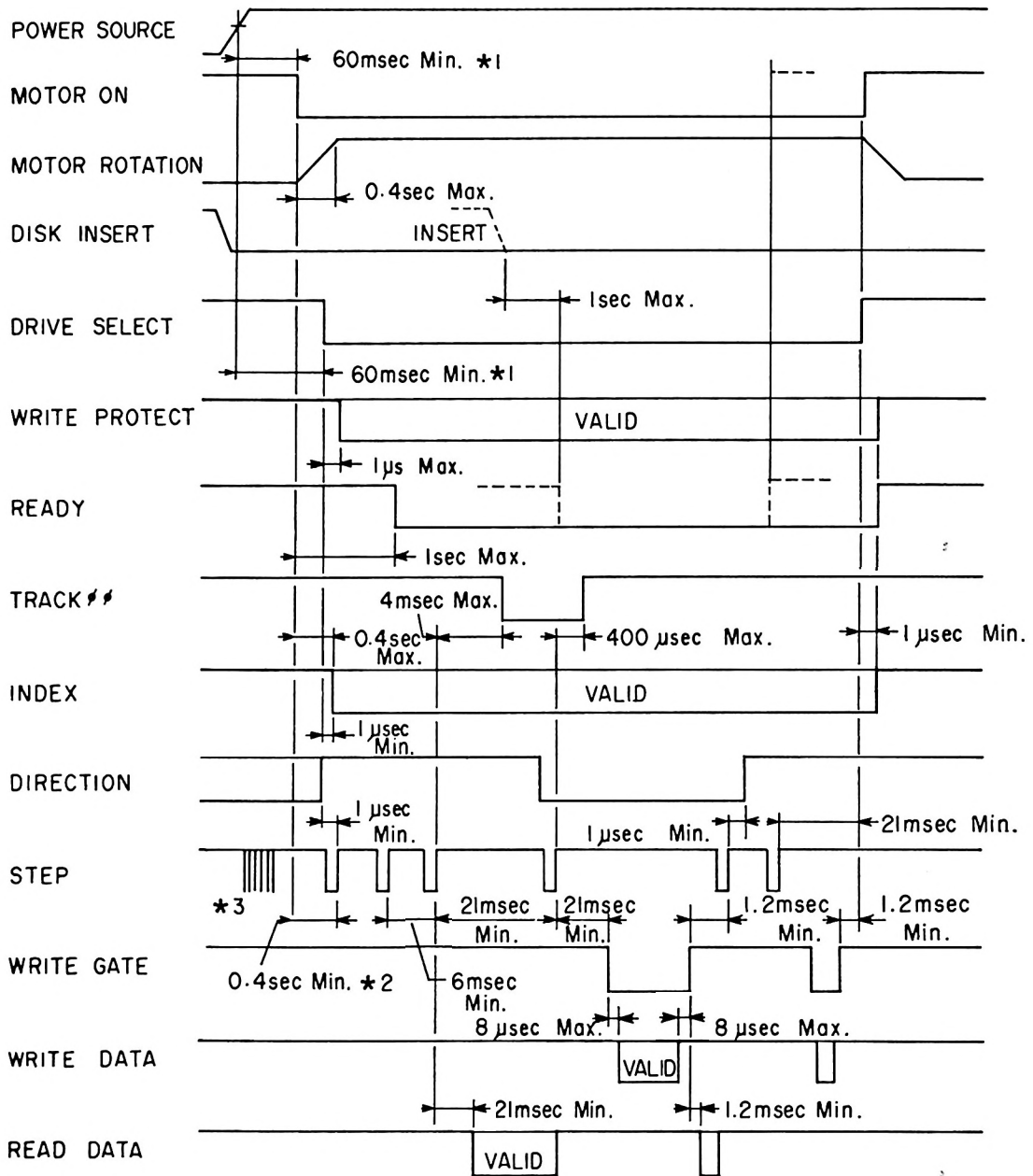


Figure 3.1 Connector Position

3.4 Timing



*1 Recommended value for reduction of power source load (stepping motor calibrating time)

*2 Recommended value for reduction of power source load (motor starting time)

*3 When the power source is turned on, 6 steps are taken unconditionally toward the inner circumference.

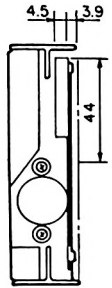
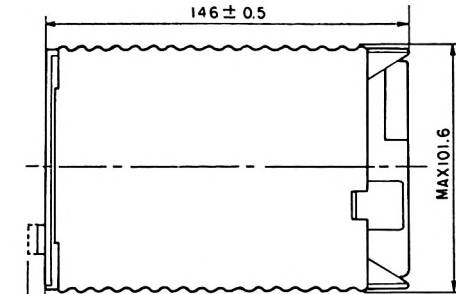
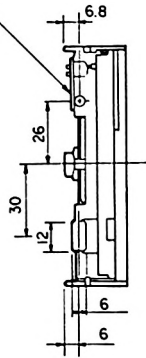
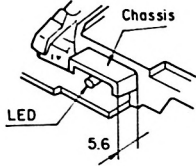
Figure 3.2 Drive Control Timing

5.0 Special Items

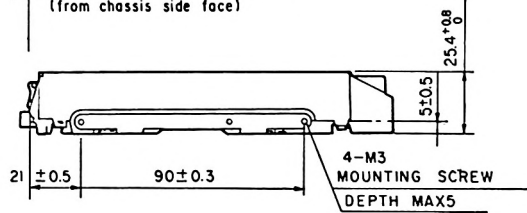
- (1) The DC power source rise shall be within 100 msec with monotonous increase.
The voltage specification shall be satisfied at the connector on the PC board when the operating current of the drive is maximum.
- (2) The signal ground and the frame ground (drive chassis) are electrically connected.
This provides the drive chassis with a shielding function.
- (3) The mounting screw length shall be a maximum of system side mounting plate thickness +5 mm. The tightening torque shall be controlled to be 4 to 6 kg-cm. When the mounting face strength is so great that flat face control is difficult, 3-point tightening is recommended (except for the stepping motor portion).
- (4) Avoid using the drive in a corrosive gas atmosphere (H_2S , SO_2 , NO_2 , Cl_2 , etc.), and in a place where there is a substance which generates a harmful gas (organic silicon system, cyanogen system, formaline system, phenol system, etc.). (This shall also apply to the case when the drive is mounted in a system.)
- (5) The delivery form of the drive is to specified separately by the packaging specification.
- (6) The components' lugs shall not protrude from the chassis bottom face.

LED: Sunset orange color when illuminated

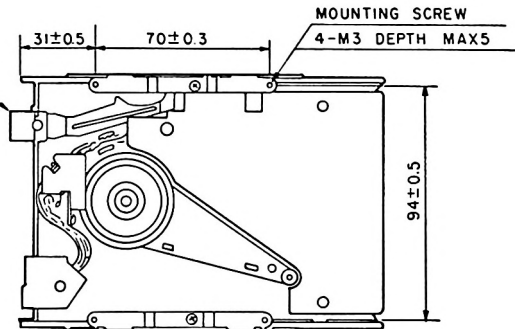
(Oblique view of main portion)



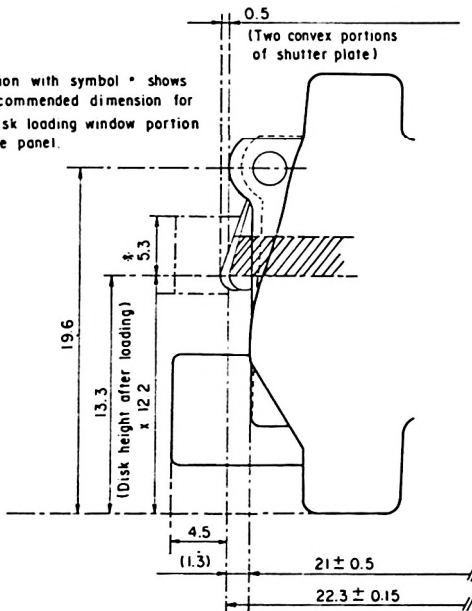
Button protruding dimension
when loaded: 9.4 max.
(from chassis side face)



COLOR: BEIGE



Dimension with symbol * shows
the recommended dimension for
the disk loading window portion
of the panel.



Circuit description of 3.5-inch FDD

General

The basic composition of the 3.5-inch floppy disk drive (EME-213AMC) is functionally divided into the spindle motor control circuit for rotating the disk at a constant speed, stepping motor control circuit for moving the R/W head to a desired track, and read/write circuit for recording onto and reproducing from the disk. The circuit composition comprises four ICs, IC1 (M52819P: R/W IC), IC2 (MH0008: gate array) and IC3 (uPC358G2, amplifier IC), IG4 (TA7774F stepper control driver), and peripheral discrete parts, and various optical and mechanical sensors.

Operation modes consist of circuit initial reset and 6-track inner seek mode when turning on the power, standby mode in waiting state, track 00 recall mode, seek mode to specified track, and data read/write mode.

The circuit is further described below in each mode while referring to the accompanying circuit diagrams.

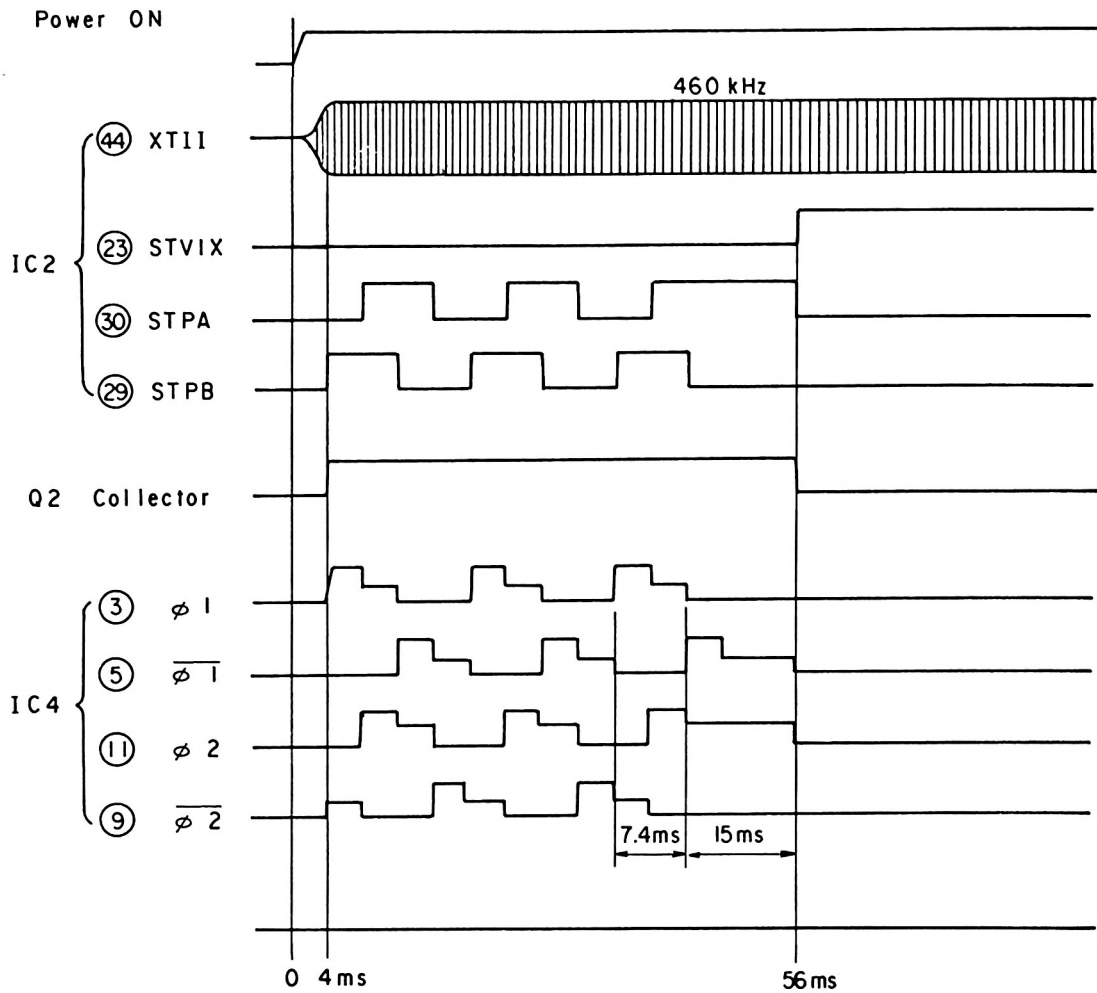
1. Circuit operation when turning on the power (6-track inner seek mode)

When the power is supplied to the 5 V terminal (pin No. 1) of power source connector J1, first in the process of voltage rise from 3.7 to 4.3 V, the voltage monitor circuit built in the IC1 operates, and "7" (XPOR) changes from Low to High. As a result, the logic circuits in IC2 are initialized (reset).

In consequence, the quartz oscillator (XT1) begins to operate, and a reference clock (460 kHz) is supplied. (At "44" at this time, this waveform can be observed, but it is recommended to use an oscilloscope of low capacity and probe of 10 Mohms or more.)

Next, automatically, step pulses are generated inside IC2, and the head moves 6 tracks in the direction of internal circumference of the disk. This process is unconditionally executed in order to avoid the problem of the head being dislocated outside of the track 00 sensor due to some cause.

This series of actions is finished in about 56 ms after turning on the power.



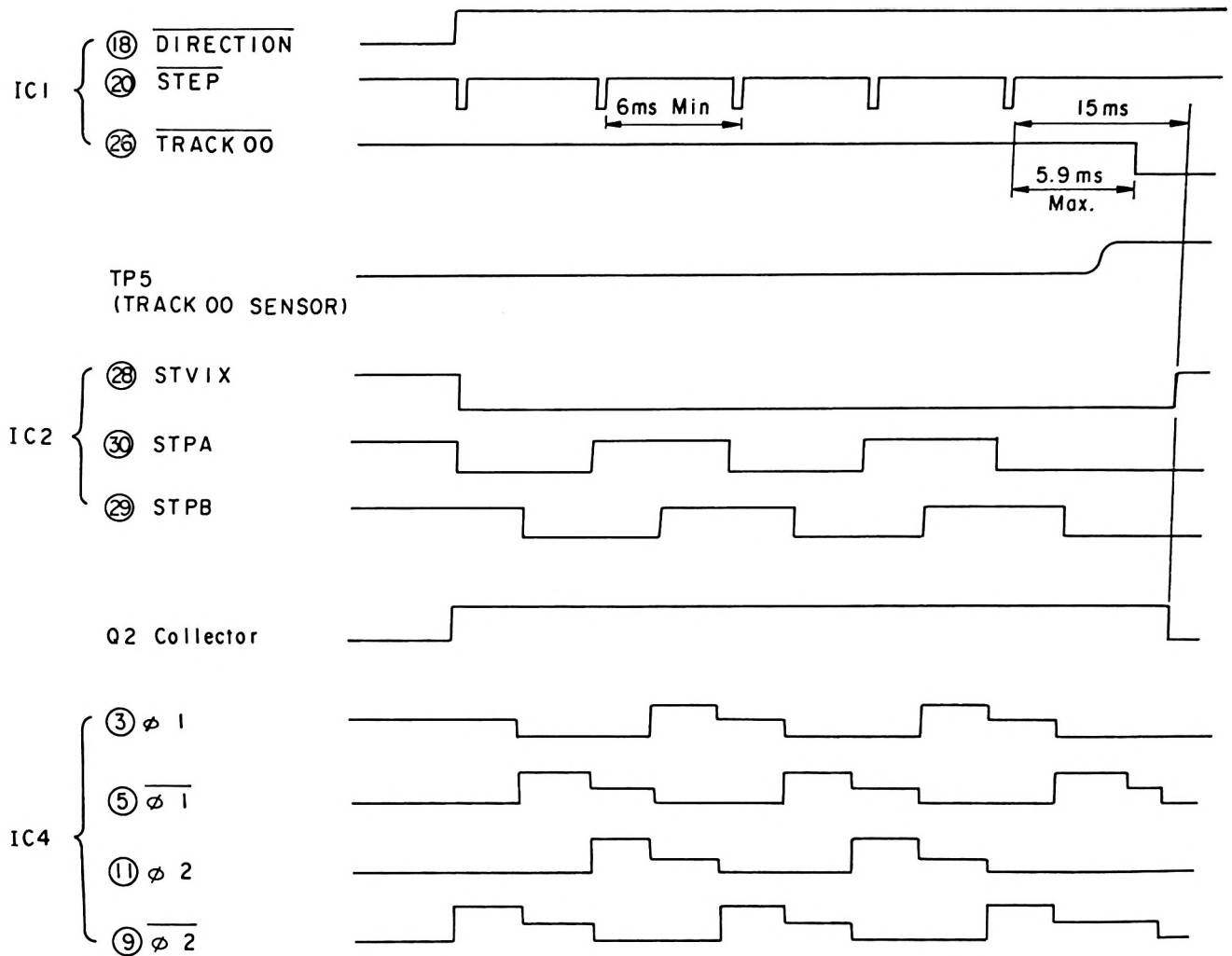
6-track Inner Seek Timing

2. Waiting state (standby mode)

When the $\overline{\text{MOTOR ON}}$ signal is High level after turning on the power, the drive is in standby state. In this state, only IC2 is operating, and all other circuits are stopped or in power-down mode (IC1). IC2 "32" becomes High level, and Q1 is turned off. Therefore, the current consumption of the entire circuit is kept under 10 mA (provided, however, all input signals of the interface line are in High logic).

3. Track 00 recall mode

For the purpose of track position initial setting after turning on the power, the host system executes the track 00 recall mode on the drive. At this time, the DIRECTION signal is set to High (outer direction), and step pulses are given at intervals of 6 ms until the TRACK 00 signal becomes Low.



Track 00 Recall Timing

4. Specified track seek mode

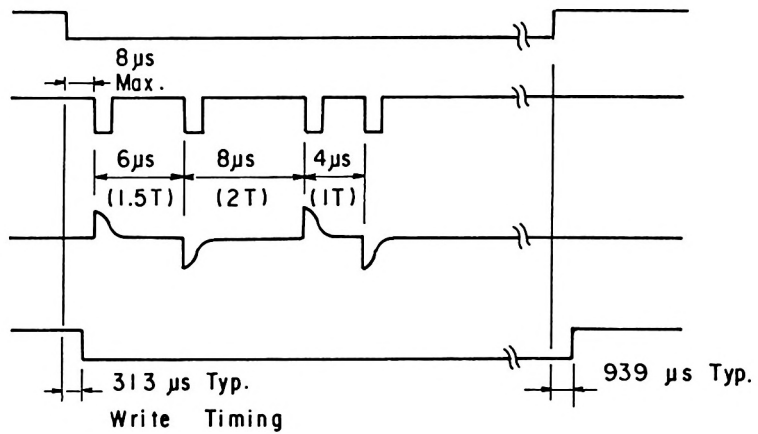
In the preceding track 00 recall mode, the head reference position of the drive and the logic of the stepping motor control register inside IC2 are established, and the subsequent specified track seek is enabled.

The seek and step action is effected by J1 DIRECTION signal and STEP signal, and the interval of step pulses is 6 ms min. When the DIRECTION signal is Low, it means the track internal circumferential direction, and when High, the external circumferential direction. At this time, the waveforms at each point are the same as in the foregoing 6-track inner seek mode and track 00 recall mode.

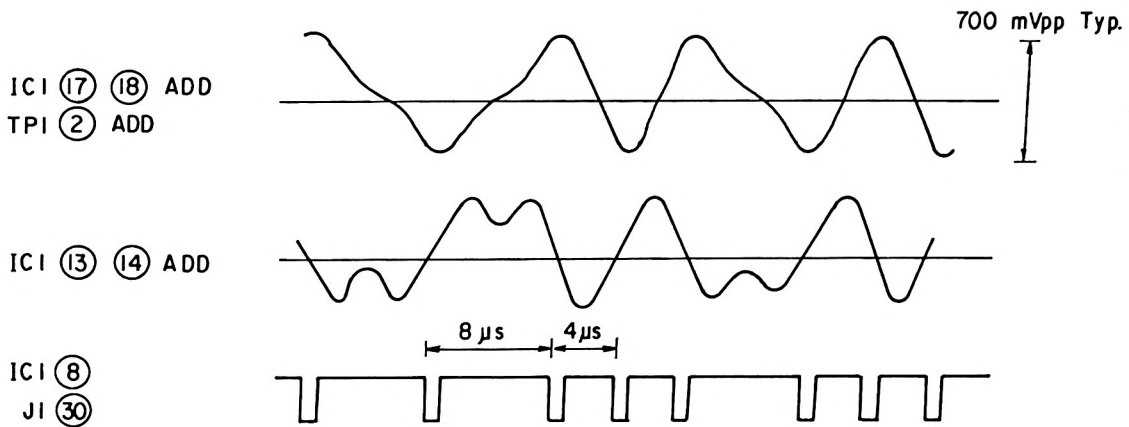
5. Data read/write mode

The write circuit for recording the data from the host system, and the read circuit for amplifying the reproduced signal from the head and delivering the read data are controlled by IC1 (M52819FP). The write condition requires that the drive is in ready state and not in seek mode, and that the supply voltage is normal (over 4.3 V).

J1 (24) WRITE GATE
 IC2 (18) (35) IC1 (3)
 J1 (22) WRITE DATA
 IC1 (2)
 IC1 (22) (23) or (24) (25)
 IC1 (27) or (26)



In the read mode, first, the head reproduced signal is amplified about 50 dB by the read AMP inside IC1, and then the signal is converted by the differential AMP so that the peak point of the waveform may be zero volt. Furthermore, by the low pass filter (cutoff frequency of about 200 kHz) composed of external R, L, C, the high frequency noise components are removed, and the waveform is shaped by a zero cross comparator, and is delivered as READ DATA.



Read Mode Waveform

In both data read and write modes, when J1 "32" $\overline{\text{SIDE SEL}}$ is High, the side 0 head is selected.

6. Mechanical and logic controller (IC2: custom gate array)

The mechanical and logic controller (IC2 MH008) is composed of a separation circuit of FG/index mixed signal, 6-track inner seek control circuit when turning on the power, erase on/off control circuit for controlling the head erasing current timing, 2-stepping delay timing control circuit for driving the 2-phase bipolar stepping motor, stepper high voltage timing control circuit, input buffers of direction control and various sensors, host system input, output signal interface, and motor control FG output circuit. This is a CMOS gate array (custom IC) of 5 V signal supply 44-pin flat type.

Pin No.	Function	Pin No.	Function
1	Oscillation output	23	Index output
2	Track 00 sensor input	24	Disk change output
3	Disk in sensor input	25	FG output
4	Write protect sensor input	26	Motor drive signal output
5	Indicator output	27	Motor start/stop output
6	FG/index mixed signal input	28	Stepper voltage output
7	Schmitt confirmation output	29	Stepper phase B output
8	Motor selection input	30	Stepper phase A output
9	2-step changeover input	31	VDD (5V)
10	Inner seek selection input	32	Power down output
11	VDD (5V)	33	Reset input
12	VSS (GND)	34	Erase gate output
13	Ready output	35	Write gate output
14	Write protect output	36	NC
15	Track 00 output	37	Ready timer output
16	VSS (GND)	38	Force ready input
17	VDD (5V)	39	VSS (GND)
18	Write gate input	40	Test input 1
19	Step input	41	Test input 2
20	Direction input	42	Test input 3
21	Motor on input	43	VSS (GND)
22	Drive select input	44	Clock input (460 kHz)

7. Read/write IC (IC1: semicustom IC)

The read/write IC (IC1: M52819FP) is a 5 V single supply 28-pin bipolar (semicustom) IC composed of read amplifier for amplifying the reproduced signal from the head, write/erase circuit for recording the data from the host system, supply voltage detection circuit for prohibiting writing in the event of abnormal voltage, and various control logic units.

Pin No.	Function	Pin No.	Function
1	GND (analog system)	15	Differentiator output
2	Write data input	16	Differentiator output
3	Write gate input	17	Differential constant setting terminal
4	Erase on input	18	Differential constant setting terminal
5	Head side select input	19	VDD (analog system)
6	Drive select input	20	Read amplifier coupling C input
7	Supply voltage detection output)	21	Read amplifier coupling C input
8	Read data output	22	Head input S0
9	VDD (digital system)	23	Head input S0
10	Power save input	24	Head input S1
11	GND (digital system)	25	Head input S1
12	Time domain filter constant	26	Erase input S1
13	Zero cross comparator input	27	Erase input S0
14	Zero cross comparator input	28	Write current setting terminal

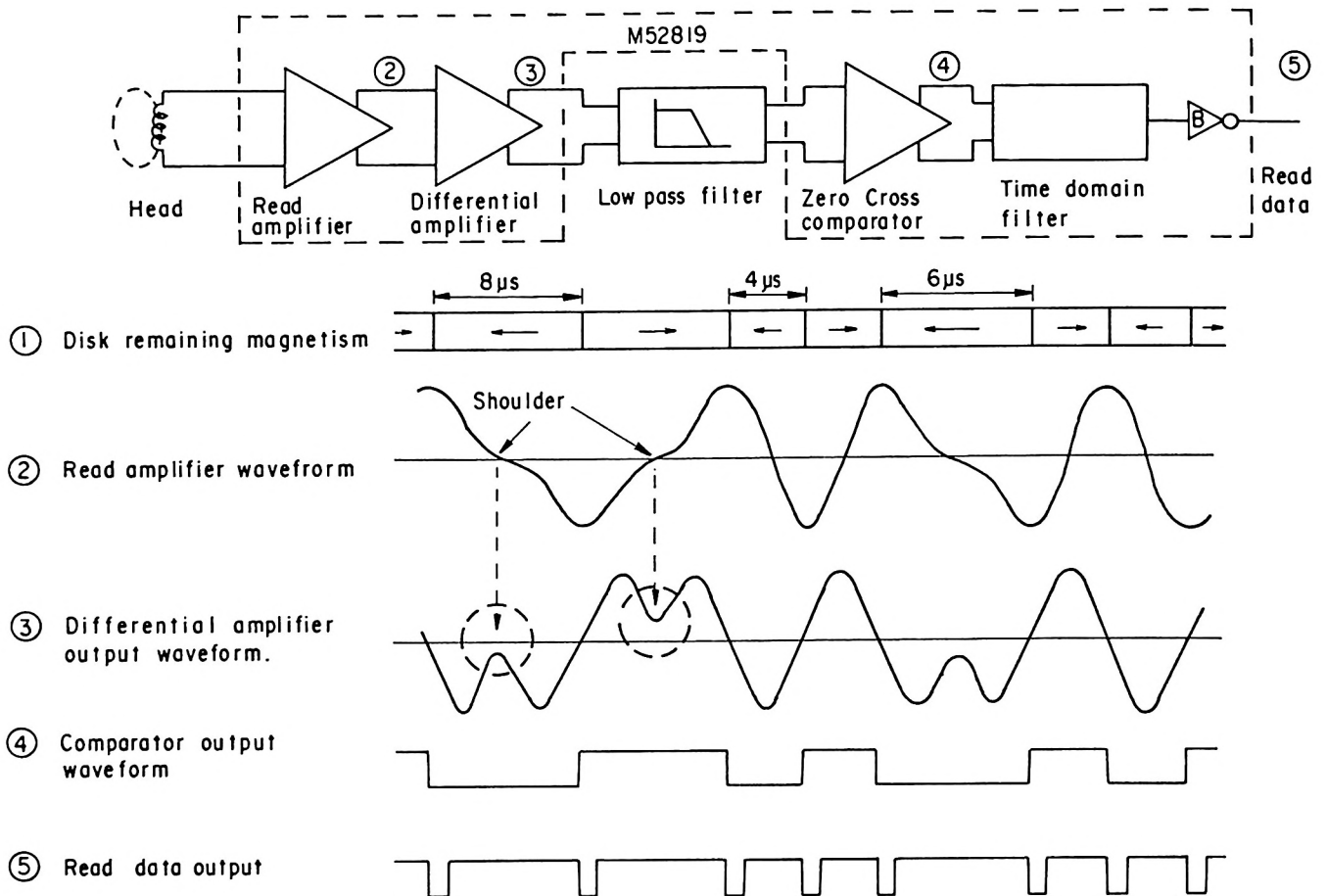
8. Stepping motor driver IC (IC4: general-purpose IC)

The stepping motor driver IC (IC4: TA7774F) is an IC for 2 phase stepping motors by bipolar driving with 5V/12V (two power supplies) and for driving the stepping motor by the stepping motor output signal from the gate array.

Pin No.	Function	Pin No.	Function
1	VCC (5V)	10	$\emptyset B$ output
2	N.C.	11	$\overline{\emptyset B}$ output
3	Vcc (5V)	12	N.C.
4	Phase A input	13	N.C.
5	Phase B input	14	$\overline{\emptyset A}$ output
6	GND	15	$\emptyset A$ output
7	N.C.	16	Vss (12V)
8	Stepper drive voltage input	Fin	GND
9	Vss (12V)		

9. Read circuit unit

The read circuit unit is composed of IC1 M52819 and various externally mounted parts.



The head reproduced signal is amplified by about 50 dB by the read amplifier, and the signal is converted by the differential amplifier so the peak point of the waveform may be zero volt (steps 2 and 3).

Next, by the low pass filter composed of externally mounted R, L, C, the noise components are eliminated, and the waveform is shaped by the zero cross comparator (step 4).

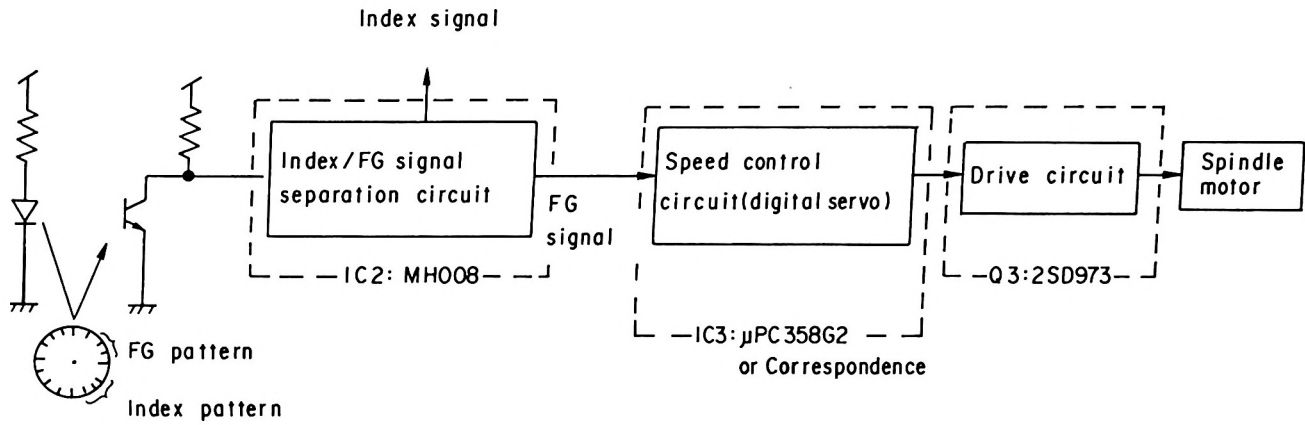
The time domain filter is a digital filter for preventing generation of zero cross due to the shoulder portion of the low frequency signal ($f=62.5$ kHz), and it is intended to prevent malfunction due to noise.

10. Supply voltage detection circuit

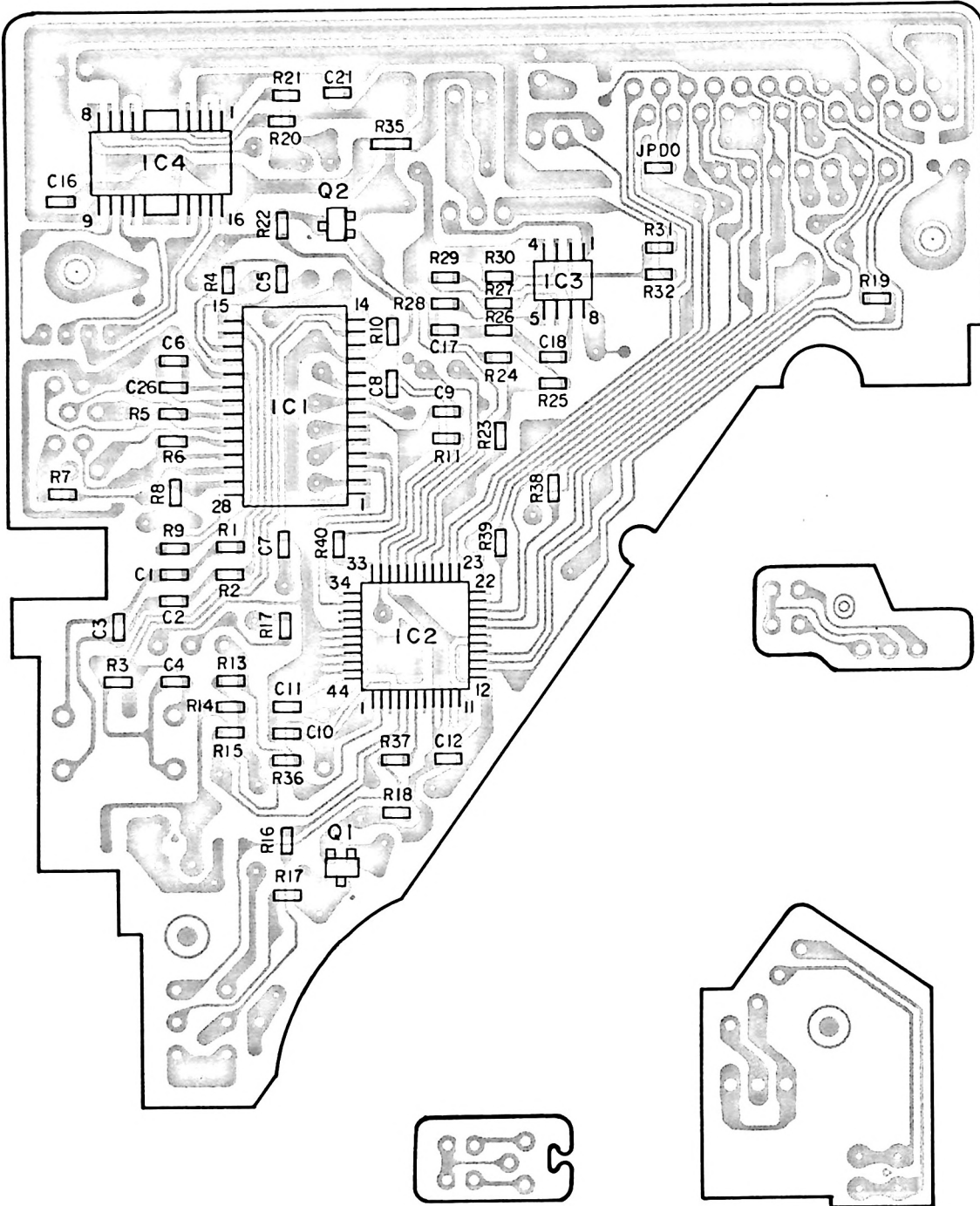
This is built in the IC1 M52819, and it is actuated at an abnormal voltage of 3.7 to 4.3V (Hysteresis 0.2V) to prohibit the write action, and at the same time the gate array logic is reset by external output, and all functions of the drive such as NOT READY output are stopped.

11. Spindle motor control circuit

The motor control circuit is composed of the photo interruptor sensor for optically detecting the signal of a slit plate directly coupled to the spindle motor (composed of FG signal part and index signal part), the circuit for separating the detected FG/index mixed signal (built in the MH008), and the circuit for comparing (digital servo) the FG signal (speed signal) and reference clock, detecting (3-phase logic) the rotating speed by using hall element output, and controlling the rotating speed of the spindle motor (incorporated in IC3 and Q3). Accordingly, there is almost no fluctuation of rotation, and adjustment of rotating speed is not necessary.



Solder Side



7

8

9

10

11

12

13

Disassembly Procedure

1) Main Board

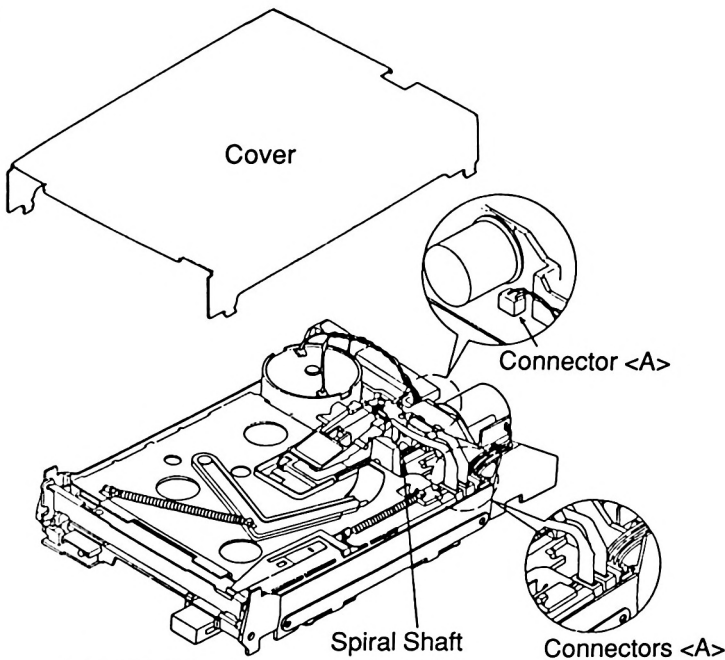


Figure 1

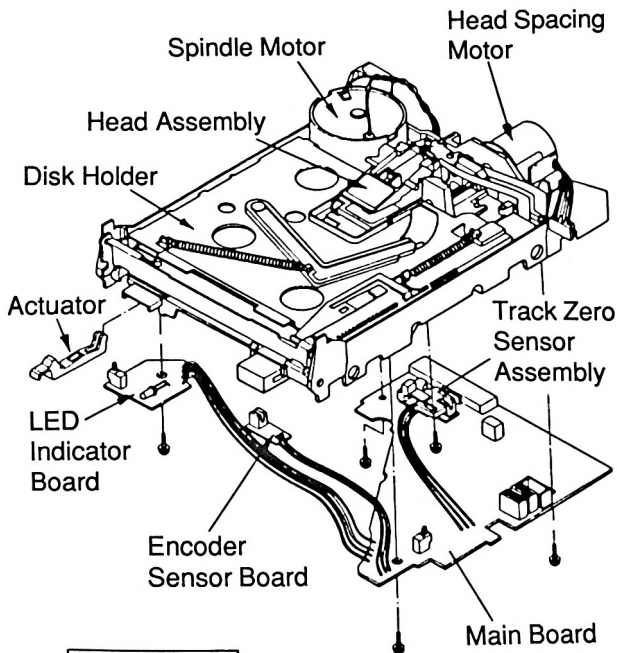
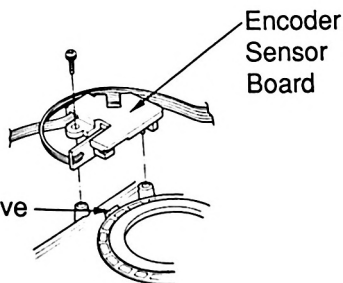


Figure 2



1) Remove the cover as shown in Figure 1.

2) Disconnect four connectors <A> from the main board as shown in Figure 1.

3) Remove one screw each from the encoder sensor board, LED indicator board and T00 track sensor assembly and three screws from the main board as shown in Figure 2.

4) Remove the main board, encoder sensor board, LED indicator board and track zero sensor assembly as shown in Figure 2.

Note:

1. The encoder sensor board is held to the chassis unit boss by an adhesive. Carefully remove it from the chassis.
2. When reinstalling the encoder sensor board, attach it to the chassis unit boss using an adhesive, then check index timing. Refer to Section "5. Adjustment".
3. When removing the track zero sensor assembly, move the R/W head assembly to the center of spiral shaft, then remove it.

5) Remove the actuator as shown in Figure 2.

2) Disk Holder

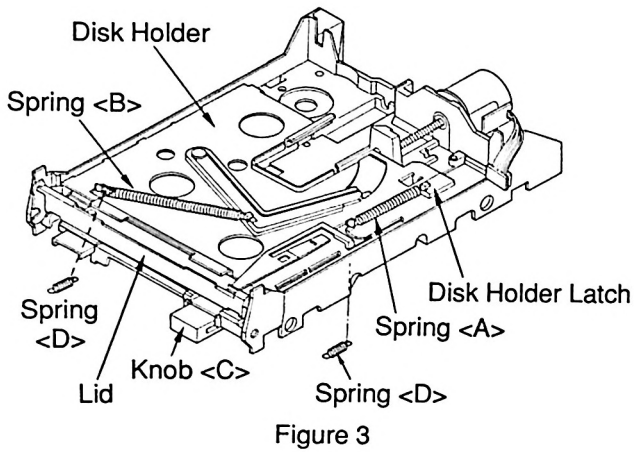


Figure 3

- 1) Remove one disk holder latch spring <A> and one holder lever spring from the chassis unit as shown in Figure 3.
- 2) Push the knob and remove the disk holder assembly as shown in Figure 3.
- 3) Remove the disk holder latch and two disk holder springs from the disk holder assembly as shown in Figure 3.
- 4) Remove the lid from the disk holder assembly in Figure 3.

3) Spindle Motor Assembly

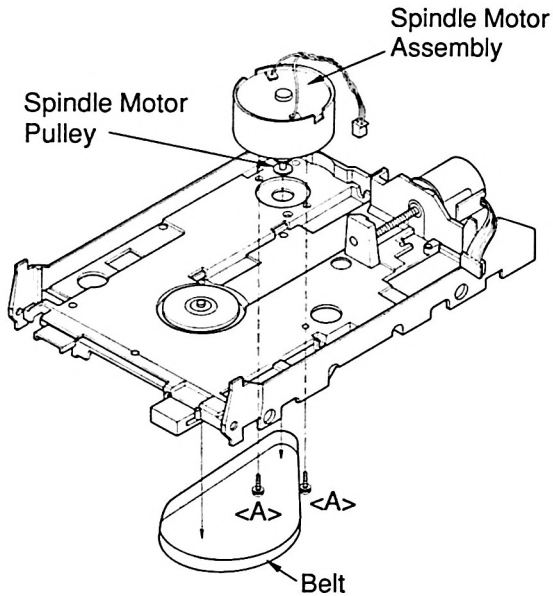


Figure 4

- 1) Remove the belt from the spindle motor pulley as shown in Figure 4.
- 2) Remove two screws <A> from the spindle motor board, then remove the spindle motor assembly as shown in Figure 4.

4) Head Spacing Motor and Head Assembly

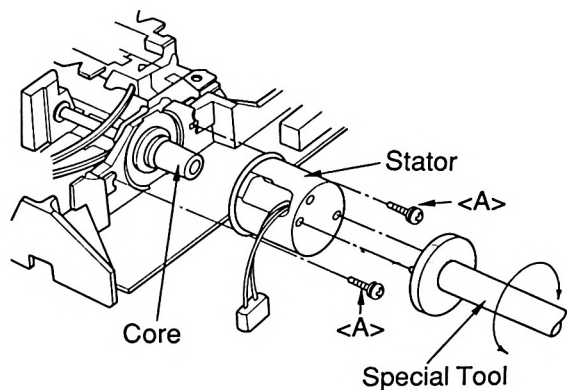


Figure 5

- 1) Remove two screws <A> from the head spacing motor stator, then remove the stator as shown in Figure 5.

Note: If necessary, remove two screws after rotating the stator by using special tool (P/N: PJZX3E31M).

- 2) Remove the core with the spiral shaft from the chassis frame while rotating it in a clockwise direction as shown in Figure 5.

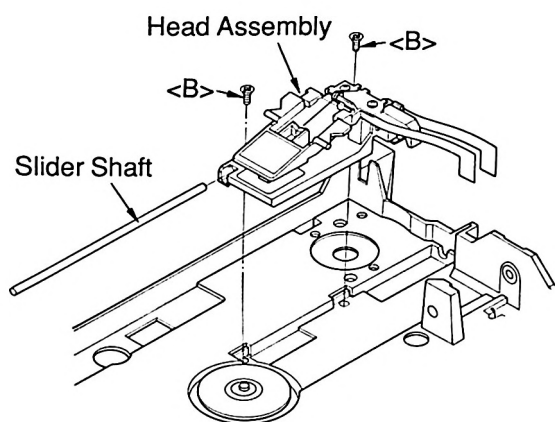


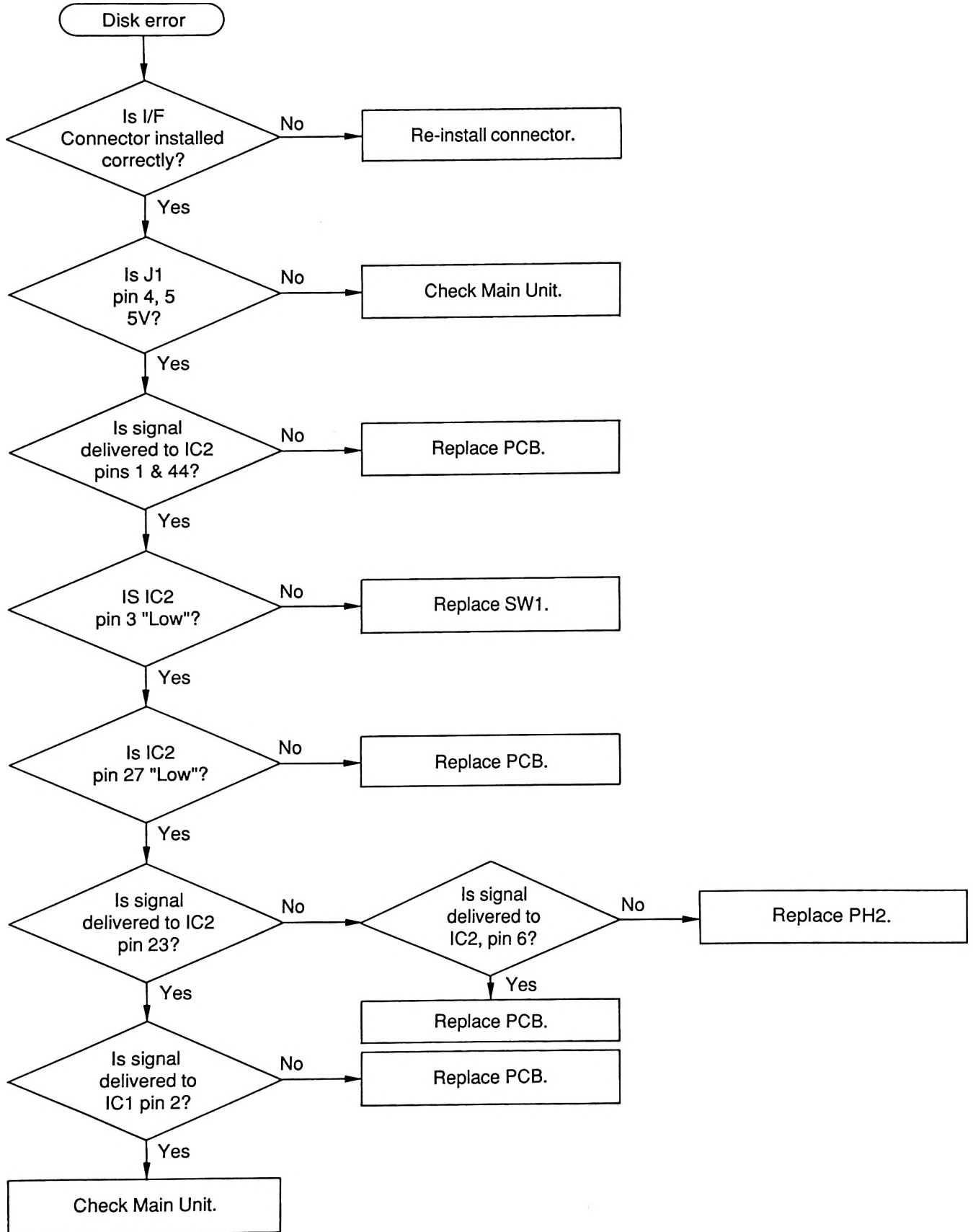
Figure 6

- 3) Remove two screws holding the head assembly shaft to the chassis unit as shown in Figure 6.
- 4) Remove the head assembly as shown in Figure 6.
- 5) Remove the slider shaft from the head assembly as shown in Figure 6.

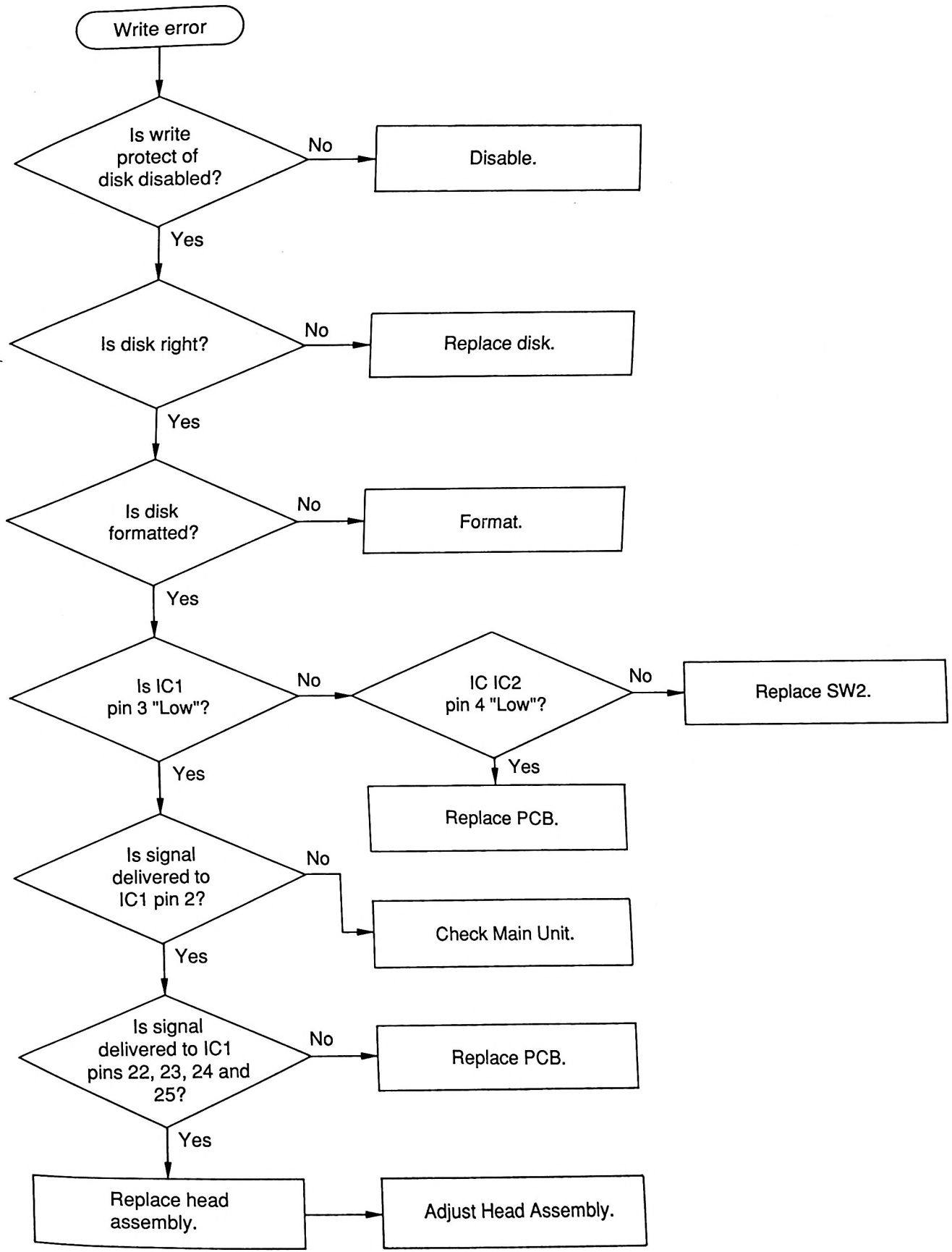
*Reassemble in the reverse order.

Troubleshooting

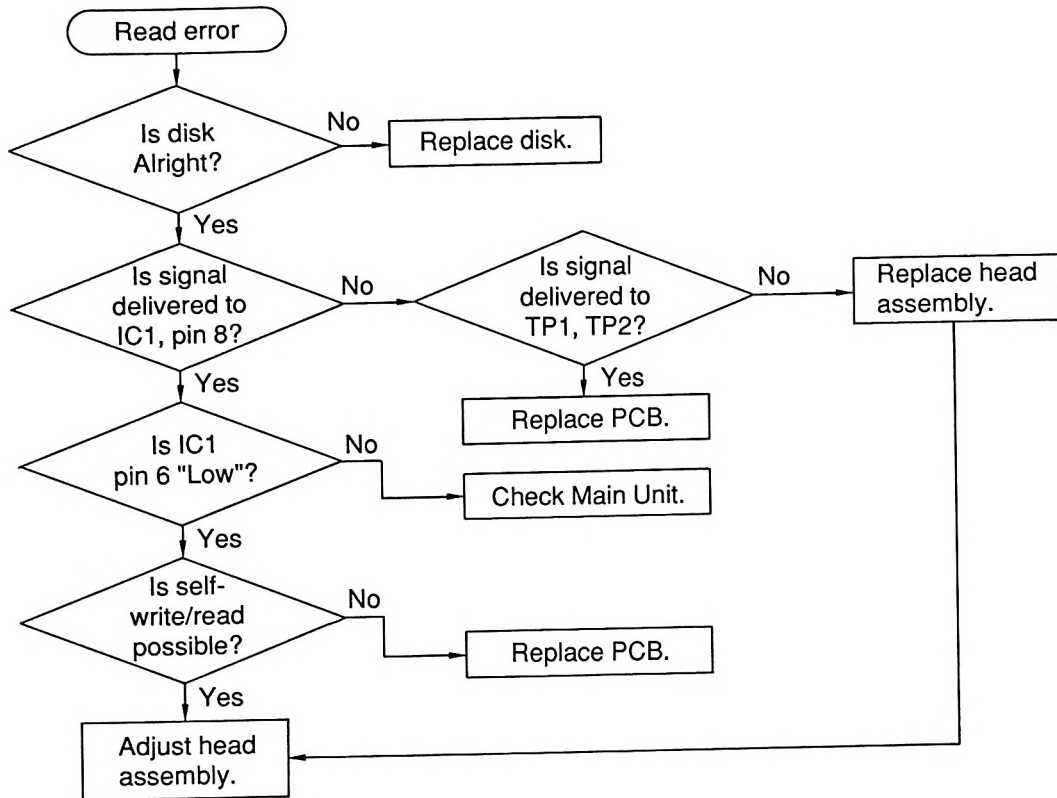
Disk Error (Initial Operation Failure)



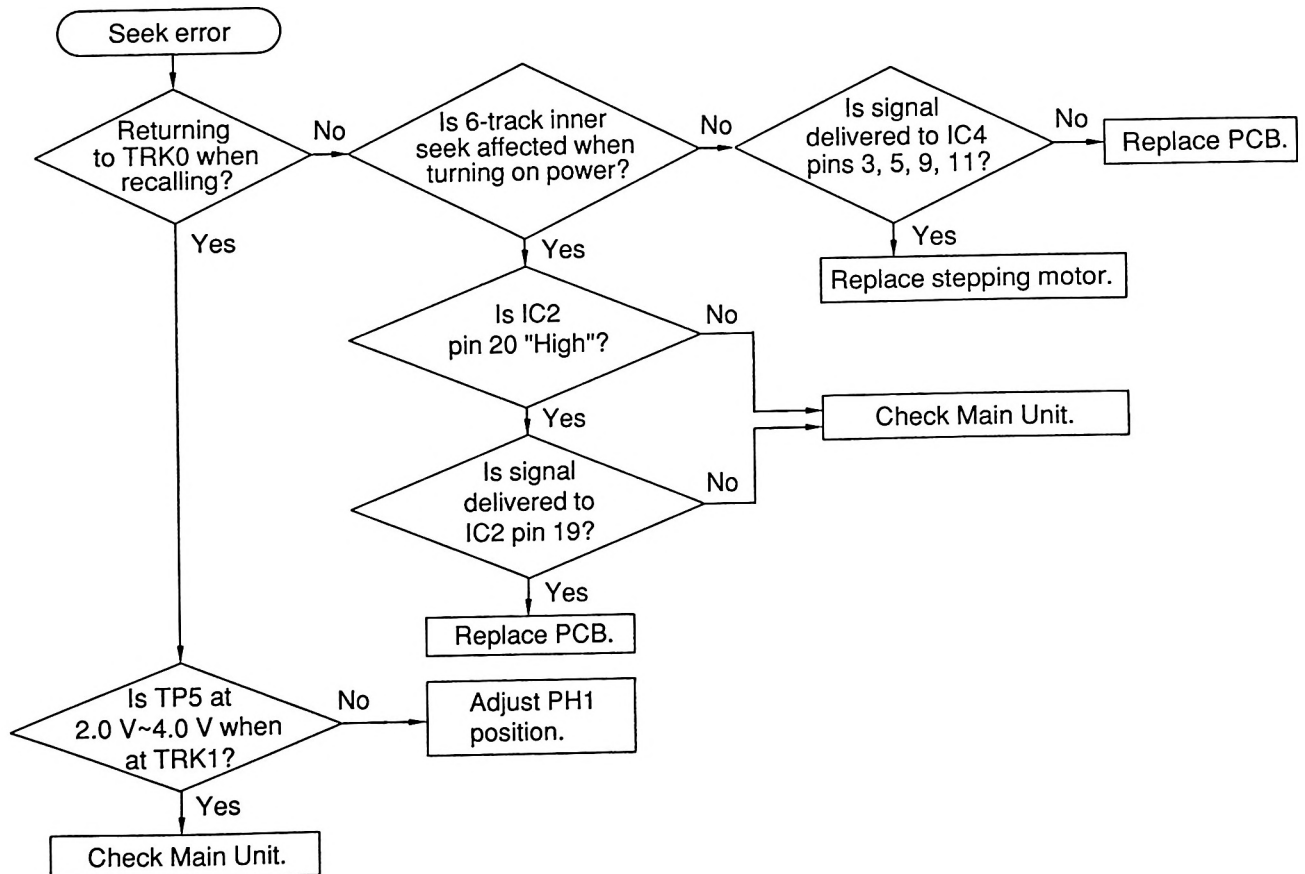
Write Error



Read Error



Seek Error



Adjustment

1. Items of adjustment

Item	Inspection standard	Adjustment standard	
Index timing	1700 μ S \pm 1700 μ S	—	3-1
Positioning	Within \pm 22 μ m	Within \pm 5 μ m	3-2
T00 sensor position	T ₀₁ : 4.5 V or less T ₀₂ : 0.5 V or more	T ₀₁ : 3.0 \pm 0.5 V DC	3-3
Alignment (azimuth angle)	\pm 12'	—	3-4

2. Instruments used

Name of instrument	Part No.	Q'ty	Remarks
Exerciser	KBC-05	1	With index sync display.
Oscilloscope		1	
Frequency counter		1	When other exerciser is used.
Torque driver		1	
Volume driver		1	
Alignment disk	EME-MF2DD	1	T40 servo pattern.
Work disk		1	Crude disk.
Positioning adjusting jig		1	

3. Checking and adjusting method

Check and adjust in the following procedure.

3.1 Checking of index timing

- (1) Insert alignment disk into the drive.
- (2) Connect the probes of the oscilloscope as follows.

CH1	Hot side	TP1 or TP2
	GND side	TP3
CH2	Hot side	Terminal 23 of 24-pin connector (J1)
	NG side	TP3

- (3) Cause a seek to TK40.
- (4) Adjust the index timing as follows.
 - 1) Set the oscilloscope to CH2.
 - 2) Turn the slope level knob, and synchronize at the fall of pulse as shown in Fig. 1.

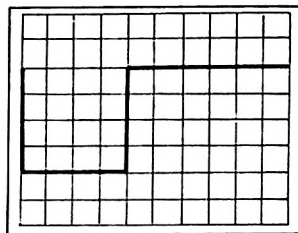


Fig. 1

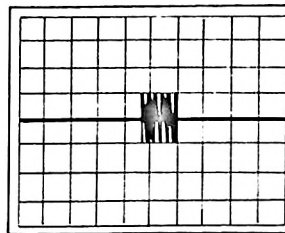


Fig. 2

- 3) Using the " $\leftarrow \rightarrow$ " knob, adjust the left end of the waveform to the left end of the graduations on the oscilloscope screen.
- 4) Change to CH1, and set TIME/DIV to 0.5 msec, and view the index timing waveform as shown in Fig. 2, and make sure it is within $1700 \mu\text{s} \pm 1700 \mu\text{s}$.

3.2 Checking and adjustment of positioning

- (1) Connect the drive to the exerciser.
- (2) Insert an alignment disk into the drive.
- (3) Connect the oscilloscope probes same as in 3.1.
- (4) Cause a seek to TK40.
- (5) Check and adjust the positioning as follows.
 - 1) Set the oscilloscope to CH2.
 - 2) Turning the slope level knob, synchronize at the fall of pulse.
 - 3) Using the " $\leftarrow \rightarrow$ " knob, adjust the left end of the waveform to the left end of the graduations on the oscilloscope screen.

- 4) Set the side selector of the exerciser to S0 and set the oscilloscope channel to S0. Set TIME/DIV at 2 msec, and view servo pattern waveform as shown in Fig. 3.

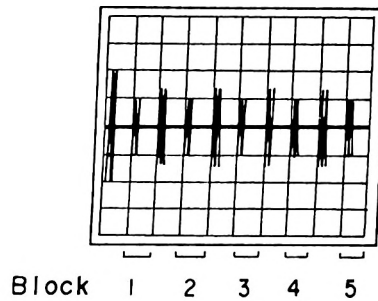


Fig. 3

(Reading head effective width: 35μ)

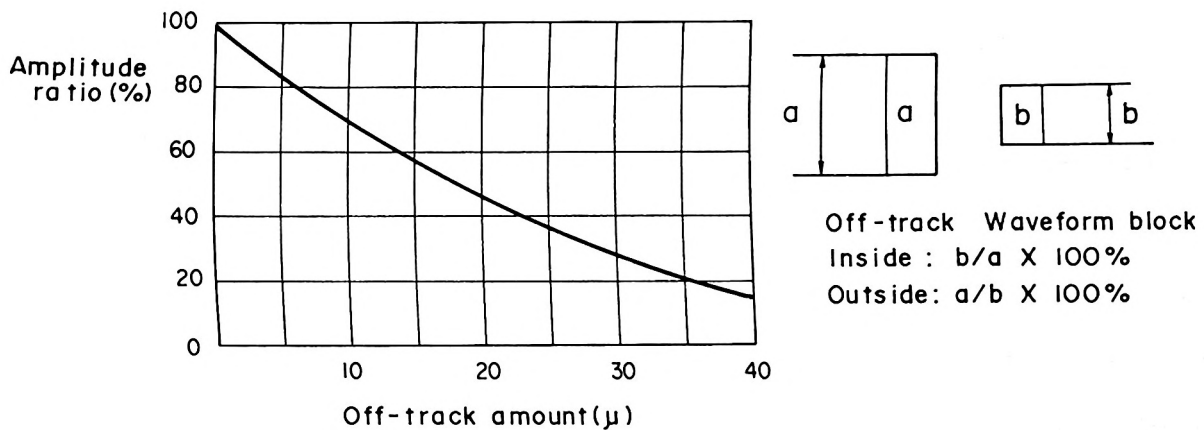


Fig. 4

- 5) Determine the output ratio in one block of the servo pattern waveform, and obtain the off-track amount from Fig. 4. At this time, make sure the off-track amount is within $2 \mu\text{m}$; otherwise, adjust as follows.
- 6) Loosen stepping motor screws, and rotate the stepping motor. Adjust to the waveform so the off-track amount is $5 \mu\text{m}$ or less.
- 7) Tighten the stepping motor screws to 3 kg-cm, and return to the original track. Make several steps inside or outside, and check the off-track amount again.

3.3 checking and adjustment of T00 sensor position

- (1) Connect the CH1 probes of the oscilloscope as shown below.

Hot side	TP5
GND side	TP3

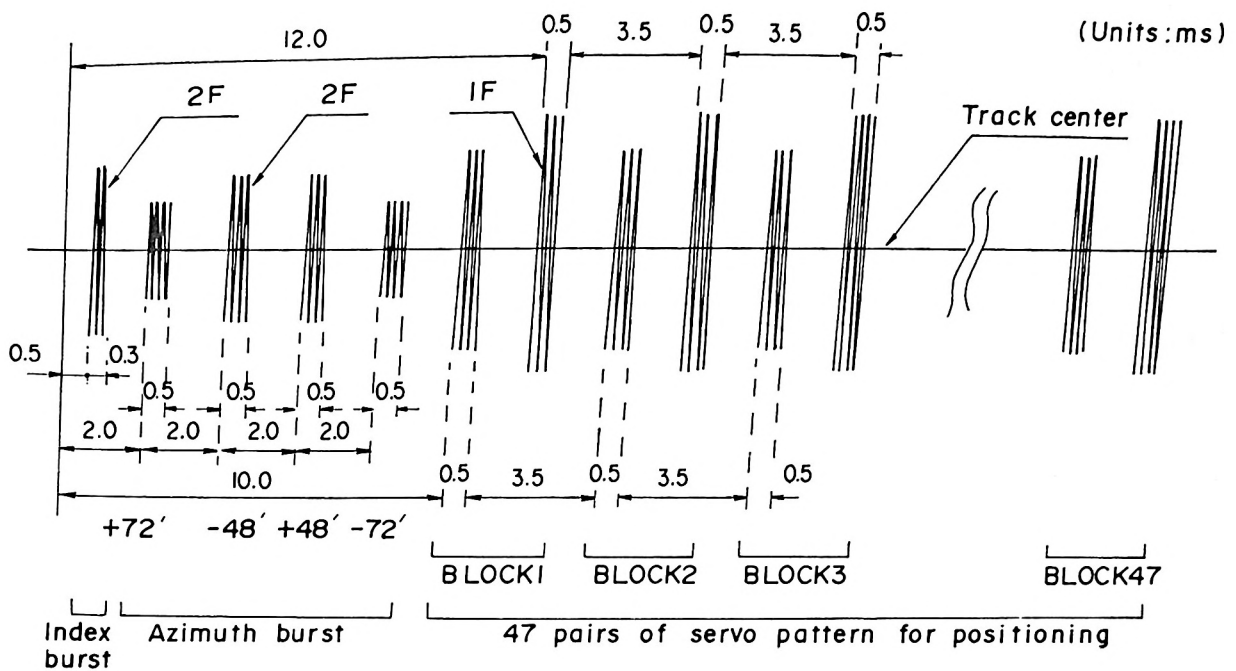
*At this time, short TP6 and GND.

- (2) Step 40 tracks toward outside from the track delivering the servo pattern in Fig. 3, and check the output of CH1 on the oscilloscope.
- (3) At this time, make sure the output is 4.5 V DC or more.
- (4) Then step 2 tracks inside, and similarly make sure the oscilloscope output is 0.5 V DC or less.
- (5) If any one of the checking items above is defective, adjust the T00 sensor position as follows.
 - a) Step 39 tracks outside from the track delivering the servo pattern, and loosen the screws of T00 sensor.
 - b) Actuate the T00 sensor so the output voltage of the oscilloscope is 2.5 V to 3.5 V DC, and tighten screws to 2 kg-cm.
 - c) Repeat steps (2) to (4) above.
 - d) Apply screw lock (Three-Bond #1401B) to the screw area.

3.4 Checking and adjustment of alignment

- (1) Insert an alignment disk into the drive.
- (2) Connect the oscilloscope probes same as in checking of index timing. (3.1)
- (3) Cause a seek to TK40.
- (4) Same as in the checking of index timing, synchronize the oscilloscope by the index pulse of CH2, and show the CH1 waveform on the oscilloscope screen.

(5) Set the TIME/DIV to 2 msec, and show the following IAP pattern on the screen.

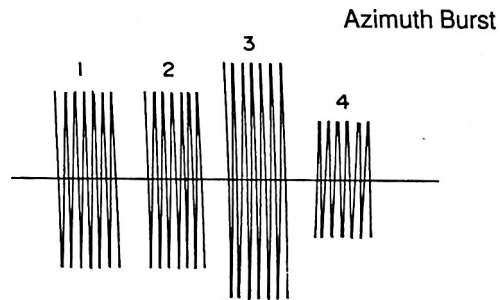


(6) Check the index timing and positioning according to the method shown in 3.1 and 3.2.

(7) Check the azimuth angle in the following waveforms.

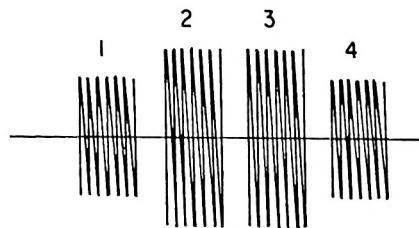
Pattern 1

Azimuth angle = $-12'$
(Levels of azimuth bursts 1, 2 are equal.)



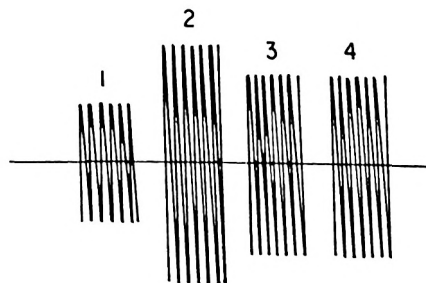
Pattern 2

Azimuth angle = $\pm 0'$
(Level of azimuth bursts 2, 3 are equal.)



Pattern 3

Azimuth angle = $+12'$
(Levels of azimuth bursts 3, 4 are equal.)



Therefore, when the level of azimuth burst 1 is smaller than that of burst 2, and the level of azimuth burst 3 is larger than that of burst 4, it may be regarded that the azimuth angle of the head being tested is within $\pm 12'$.

- (8) Inspect items (6) and (7) for both heads, and make sure the values are within the standard.
- (9) If out of the standard, adjust as follows.
 - 1) Insert a cleaning disk, and seek from T00 to T79 and vice versa, and clean the head.
 - 2) Take out the cleaning disk, and insert an alignment disk, and seek to T40.
 - 3) As shown in Fig. 5, hold the S1 head by hand, and adjust the position of S1 head by hand while observing the oscilloscope waveform.

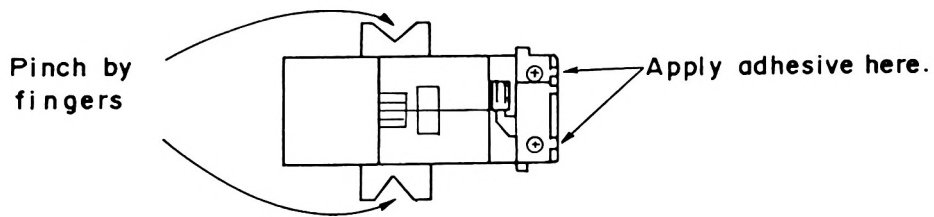


Fig. 5

- 4) Observe the oscilloscope waveform, and make sure the index, azimuth and positioning are all within the standard, and tighten the screws firmly (torque: 2 kgf-cm).
- 5) Take out the disk, and apply an instantaneous adhesive to two positions shown in Fig. 5 (use Lock-Tite #420).
- 6) Apply screw-lock (Three-Bond #1401B) to the screw tightening parts.

Appendix C. BIOS Interface

Software Contents

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Bootstrap Loader	C-10
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Additional Data Area	C-13
EEPROM definition for BIOS	C-14

BIOS Services

Device I/O Services

Following is a quick reference list of software interrupts for all device I/O and system status services.

Service	Software Interrupts
Video Display	10 hex (16 dec)
Equipment	11 hex (17 dec)
Memory Size	12 hex (18 dec)
Diskette	13 hex (19 dec)
Serial Communications	14 hex (20 dec)
System Services	15 hex (21 dec)
Keyboard	16 hex (22 dec)
Line Printer	17 hex (23 dec)
Bootstrap Loader	19 hex (25 dec)
System Clock/Real Time Clock	1A hex (26 dec)

Keyboard

16 hex (22 dec)

Function Summary

AH=0:	Read keyboard (destructive with wait)
AH=1:	Scan keyboard (nondestructive, no wait)
AH=2:	Get current shift status
AH=5:	Store ASCII character and scan code in keyboard buffer
AH=10H:	Extended keyboard read
AH=11H:	Extended ASCII status
AH=12H:	Extended shift status read

Function Descriptions

Read Keyboard

Read the next character typed at the keyboard. Return the ASCII value of the character and the keyboard scan code, removing the entry from the keyboard buffer (destructive read).

Entry Conditions

AH=0

Exit Conditions

AL=ASCII value of character
AH=keyboard scan code

Scan Keyboard

Set up the zero flag (Z flag) to indicate whether a character is available to read from the keyboard or not. If a character is available, return the ASCII value of the character and the keyboard scan code. The entry remains in the keyboard buffer (non-destructive read).

Entry Conditions

AH=1

Exit Conditions

Z=no character available

NZ=a character is available, in which case:

AL=ASCII value of character

AH=keyboard scan code

Get Shift Status

Return the current shift status.

Entry Conditions

AH=2

Exit Conditions

AL=current shift status

(bit settings: set=true, reset=false)

Bit 0=RIGHT SHIFT key depressed

Bit 1=LEFT SHIFT key depressed

Bit 2=CTRL (control) key depressed

Bit 3=ALT (alternate mode) key depressed

Bit 4=SCROLL state active

Bit 5=NUMBER lock engaged

Bit 6=CAPS lock engaged

Bit 7=INSERT state active

Store ASCII Character

Entry Conditions

AH=5

CL=ASCII character

CH=Scan Code

Exit Conditions

AL=00: Successful

AL=01: Buffer full

[C]=Operation failed

Extended Keyboard Read

Entry Conditions

AH=10H

Exit Conditions

AL=ASCII value of character

AH=keyboard scan code

Extended ASCII Status

Entry Conditions

AH=11H

Exit Conditions

Z=No character is available

NZ=A character is available, in which case:

AL=ASCII value of character

AH=keyboard scan code

Extended Shift Status Read

Entry Conditions

AH=12H

Exit Conditions

AL=shift status (bit settings: set=true, reset=false)

Bit 7=INSERT active

Bit 6=CAPS LOCK active

Bit 5=NUM LOCK active

Bit 4=SCROLL LOCK active

Bit 3=ALT pressed

Bit 2=CTRL pressed

Bit 1=LEFT SHIFT pressed

Bit 0=RIGHT SHIFT pressed

AH=extended shift status

(bit settings: set=true, reset=false)

Bit 7=SYS REQ pressed

Bit 6=CAPS LOCK active

Bit 5=NUM LOCK active

Bit 4=SCROLL LOCK active

Bit 3=RIGHT ALT active

Bit 2=RIGHT CTRL active

Bit 1=LEFT ALT active

Bit 0=LEFT CTRL active

Video Display

These routines provide an interface for the video display—the output half of the console (CON) device. MS-DOS considers the video display to be the default standard output (STDOUT) device.

Software Interrupts

10 hex (16 dec)

Function Summary Table Supported Video BIOS Calls

INT 10H

AH=00	Set Video Mode
AH=01	Set Cursor Type
AH=02	Set Cursor Position
AH=03	Read Cursor Position
AH=05	Select Active Display Page
AH=06	Scroll Active Page Up
AH=07	Scroll Active Page Down
AH=08	Read Attribute/Character at Current Cursor Position
AH=09	Write Attribute/Character at Current Cursor Position
AH=0A	Write Character Only at Current Cursor Position
AH=0B	Set Color Palette
AH=0C	Write Dot
AH=0D	Read Dot
AH=0E	Write TTY to Active Display
AH=0F	Current Video State
AH=13	Write String
AL=00	Write Character String
AL=01	Write Character String and Move Cursor
AL=02	Write Character and Attribute Strings
AL=03	Write Character and Attribute Strings and Move Cursor

Function Descriptions Set CRT Mode

Entry Conditions

AH=0

AL=*mode value*, as follows:

Alpha Modes

AL=0:	40×25 black and white
AL=1:	40×25 color
AL=2:	80×25 black and white
AL=3:	80×25 color

Graphics Modes

AL=4:	320×200 color graphics
AL=5:	320×200 black and white graphics with 4 shades
AL=6:	640×200 black and white graphics with 2 shades
AL=7:	monochrome text (1100FD Hardware does not support it)

Additional Modes

AL=8:	160×200 color graphics with 16 colors
AL=9:	320×200 color graphics with 16 colors
AL=A:	640×200 color graphics with 4 colors

Note: If the high order bit of the AL register is 1, then the video buffer is not cleared.

Set Cursor Type

Set the cursor type and attribute.

Entry Conditions

AH=1

CH=*bit values*:

Bits 5-6=*an invisible or erratically blinking cursor*

Bits 5-6=0: *produces a visible, blinking cursor*

Bits 4-0=*start line for cursor within character cell*

CL=*bit values*:

Bits 4-0=*end line for cursor within character cell*

Set Cursor Position

Write (set) cursor position.

Entry Conditions

AH=2

BH=*page number* (must be 0 for graphics modes)

DH=*row* (0=top row)

DL=*column* (0=leftmost column)

Get Cursor Position

Read (get) cursor position.

Entry Conditions

AH=3

BH=*page number* (must be 0 for graphics modes)

Exit Conditions

DH=*row of current cursor position* (0=top row)

DL=*column of current cursor position*
(0=leftmost column)

CX=*cursor type currently set* [1]:

See previous "Set Cursor Type" (AH=1).

Select Active Page

Select active display page (valid in alpha mode only).

Entry Conditions

AH=5

AL=0 through 7: *new page value for modes 0, 1*

AL=0 through 3: *new page values for modes 2, 3*

Exit Conditions

Scroll Up

Scroll active page up.

Entry Conditions

AH=6

AL=*numbers of lines to scroll*. The number of lines that will be left blank at the bottom of the window.
(0=blank entire window)

CH=*row of upper left corner of scroll window*

CL=*column of upper left corner of scroll window*

DH=*row of lower right corner of scroll window*

DL=*column of lower right corner of scroll window*

BH=*attribute* (alpha modes) or *color* (graphics modes) to be used on blank line

Attributes

Color modes.

Foreground color:

Bit 0:=blue

Bit 1:=green

Bit 2:=red

Bit 3:=intensity

All bits off=black

Background color:

Bit 4:=blue

Bit 5:=green

Bit 6:=red

Bit 7:=blink

All bits off=white

Scroll Down

Scroll active page down.

Entry Conditions

AH=7

AL=*number of lines to scroll* (0=blank entire window)

CH=*row of upper left corner of scroll window*

CL=*column of upper left corner of scroll window*

DH=*row of lower right corner of scroll window*

DL=*column of lower right corner of scroll window*

BH=*attribute* (alpha modes) or *color* (graphics modes) to be used on blank line. See "Scroll Up" (AH=6) for attribute values and "Set Color Palette" (AH=0BH) for color values.

Read Attribute or Color/Character

Read a character and its attribute or color at the current cursor position.

Entry Conditions

AH=8

BH=*display page number* (not used in graphics modes)

Exit Conditions

AL=*character read*

AH=*attribute of character* (alpha modes only)

Write Attribute or Color/Character

Write a character and its attribute or color at the current cursor position.

Entry Conditions

AH=9

BH=*display page number* (not used in graphics modes)

CX=*number of characters to write*

AL=*character to write*

BH=*attribute of character* (for alpha modes) or *color of character* (for graphics modes. If Bit 7 of BL is set, the color of the character is XOR'ed with the color value). See "Scroll Up" (AH=6) for attribute values and "Set Color Palette" (AH=0BH) for color values.

Write Character Only

Write character only at current cursor position.

Entry Conditions

AH=0AH

BH=*display page number* (valid for alpha modes only)

CX=*number of characters to write*

AL=*character to write*

BL=*color of character* (graphics mode)

Set Color Palette

Select the color palette.

Entry Conditions

AH=0BH

BH=0: Set background color (0–15) to color value in BL.

BL=*color value*:

1=blue	5=magenta	9=light blue	13=light magenta
2=green	6=yellow	10=light green	14=yellow
3=cyan	7=light grey	11=light cyan	15=white
4=red	8=dark grey	12=light red	

or

BH=1: Set default palette to the number (0 or 1) in BL.

In black and white modes:

BL=0: 1 for white

BL=1: 1 for black

In 4 color graphics modes:

BL=0: (1=green, 2=red, 3=yellow)

BL=1: (1=cyan, 2=magenta, 3=white)

In 16 color graphics modes:

1=blue	5=magenta	9=light blue	13=light magenta
2=green	6=yellow	10=light green	14=yellow
3=cyan	7=light grey	11=light cyan	15=white
4=red	8=dark grey	12=light red	

Note: For alpha modes, Palette Entry 0 indicates the border color. For graphics modes, Palette Entry 0 indicates the border and the background color.

Write Dot

Write a pixel (dot).

Entry Conditions

AH=0CH

DX=*row number*

CX=*column number*

AL=*color value* (When Bit 7 of AL is set, the resultant color value of the dot is the exclusive OR of the current dot color value and the value in AL.)

Read Dot

Read a pixel (dot).

Entry Conditions

AH=0DH

DX=*row number*

CX=*column number*

Exit Conditions

AL=*color value of dot read*

Write TTY

Write a character in teletype fashion. (Control characters are interpreted in the normal manner.)

Entry Conditions

AH=0EH

AL=*character to write*

BL=*foreground color* (graphics mode)

BH=*display page* (alpha modes)

Get CRT Mode

Get the current video mode.

Entry Conditions

AH=0FH

Exit Conditions

AL=*current video mode*. See the previous "Set CRT Mode" (AH=0) for values

AH=*number of columns on screen*

BH=*current active display page*

Set Palette Registers

Sets palette registers.

Entry Conditions

AH=10H

AL=0: Set Palette register

BL=*number of palette register* (0–15) to set

BH=*color value to store*

AL=1: Set border color register

BH=*color value to store*

AL=2: Set palette color value to store and border registers

ES:DX points to a 17-byte list.

Bytes 0–15=*values for palette registers 0–15*

Byte 16=*value for border register*

Write String

Display a string of characters on screen.

Entry Conditions

AH= 13H

ES:BP= *pointer to start of string*

CX= *length of string* (attributes do not count)

DX= *starting cursor position*

(DH=row, DL=column)

BH= *page number* (for text modes)

BL= *attribute for characters* (graphic modes)

AL= 00: Characters only string, cursor not updated

AL= 01: Characters only string, cursor updated

AL= 02: Character, attribute alternating string, cursor not updated

AL= 03: Character, attribute alternating string, cursor updated

Serial Communications

These routines provide asynchronous byte stream I/O from and to the RS-232C serial communications port. This device is labeled the auxiliary (AUX) I/O device in the device list maintained by MS-DOS.

Software Interrupts

14 hex (20 dec)

Function Summary

AH=0: Reset Comm port
 AH=1: Transmit character
 AH=2: Receive character
 AH=3: Get current Comm status
 DX= *communication port number* (0 or 1)

Function Descriptions

Reset Comm Port

Reset (or initialize) the communication port according to the parameters in AL, DL, and DH.

Entry Conditions

AH=0
 AL=*RS-232C parameters*, as follows:
 DX=*port number* (0 or 1)

7 6 5	4 3	2	1 0
<i>Baud Rate</i>	<i>Parity</i>	<i>Stop Bits</i>	<i>Word Length</i>

000= 110 baud	00=none	0=1 bit	10=7 bits
001= 150 baud	01=odd	1=2 bits	11=8 bits
010= 300 baud	11=even		
011= 600 baud			
100=1200 baud			
101=2400 baud			
110=4800 baud			
111=9600 baud			

Exit Conditions

AX=*RS-232C status*; See the following "Get Current Comm Status" (AH=3)

Transmit Character

Transmit (output) the character in AL (which is preserved).

Entry Conditions

AH=1
 AL=*character to transmit*
 DX=*port number* (0 or 1)

Exit Conditions

AH=*RS-232C status*; See the following "Get Current Comm Status" (AH=3). (If Bit 7 is set, the routine was unable to transmit the character because of a timeout error.)
 AL is preserved

Receive Character

Receive (input) a character in AL (wait for a character, if necessary). On exit, AH will contain the RS-232C status, except that only the error bits (1, 2, 3, 4, 7) can be set; the timeout bit (7), if set, indicates that data set ready was not received and the bits in AH are not meaningful. Thus, AH is non-zero only when an error occurred.

Entry Conditions

AH=2
 DX=*port number* (0 or 1)

Exit Conditions

AL=*character received*
 AH=*RS-232C status*; See the following "Get Current Comm Status" (AH=3)

Get Current Comm Status

Read the communication status into AX.

Entry Conditions

AH=3
 DX=*port number* (0 or 1)

Exit Conditions

AH=*RS-232C status*, as follows (set=true):

- Bit 0=data ready
- Bit 1=overrun error
- Bit 2=parity error
- Bit 3=framing error
- Bit 4=break detect
- Bit 5=transmitter holding register empty
- Bit 6=transmitter shift register empty
- Bit 7=timeout occurred

AL=*modem status*, as follows (set=true):

- Bit 0=delta clear to send
- Bit 1=delta data set ready
- Bit 2=trailing edge ring detector
- Bit 3=delta receive line signal detect
- Bit 4=clear to send
- Bit 5=data set ready
- Bit 6=ring indicator
- Bit 7=receive line signal detect

Line Printer

These routines provide an interface to the parallel line printer. This device is labeled "PRN" in the device list maintained by the operating system.

Software Interrupts

17 hex (23 dec)

Function Summary

AH=0: Print character
AH=1: Reset printer port
AH=2: Get current printer status

Function Descriptions

Print a Character

Entry Conditions

AH=0
AL=*character to print*
DX=*printer to be used (0-2)*

Exit Conditions

OAH=*printer status*. See the following "Get Current Printer Status" (AH=2)
(If Bit 0 is set, the character could not be printed because of a timeout error.)

Reset Printer Port

Reset (or initialize) the printer port.

Entry Conditions

AH=1
DX=*printer to be used (0-2)*

Exit Conditions

AH=*printer status*; See the following "Get Current Printer Status" (AH=2)

Get Current Printer Status

Read the printer status into AH.

Entry Conditions

AH=2

Exit Conditions

DX=*printer to be used (0-2)*
AH=*printer status as follows (set=true)*:
Bit 0=timeout occurred
Bit 1=[unused]
Bit 2=[unused]
Bit 3=I/O error
Bit 4=selected
Bit 5=out of paper
Bit 6=acknowledge
Bit 7=not busy

System Clock/Real Time Clock

These routines provide methods of reading and setting the clock maintained by the system. This device is labeled CLOCK in the device list of the operating system. An interface for setting the multiplexer for audio source is also provided.

Software Interrupts

1A hex (26 dec)

Function Summary

AH=0: Get time of day
AH=1: Set time of day
AH=2: Read real-time clock
AH=3: Set real-time clock
AH=4: Read date from real-time clock
AH=5: Set the date in the real-time clock
AH=6: Set Alarm
AH=7: Reset Alarm

The clock runs at the rate of 1,193,180/65,536 per second (about 18.2 times per second).

Function Descriptions

Get Time of Day

Get (read) the time of day in binary format.

Entry Conditions

AH=0

Exit Conditions

CX=*high (most significant) portion of the clock count*
DX=*low (least significant) portion of the clock count*
AL=0 of the clock was read or written (via AH=0,1) within the current 24-hour period; otherwise, AL=0

Set Time of Day

Set (write) the time of day using binary format.

Entry Conditions

AH=1

CX=*high* (most significant) *portion of the clock count*

DX=*low* (least significant) *portion of the clock count*

Read Clock Time of Day

Read the time fo day kept in the clock.

Entry Conditions

AH=2

Exit Conditions

CH=hours in BCD

CL=minutes in BCD

DH=seconds in BCD

Set Clock Time of Day

Set the time of day kept in the clock.

Entry Conditions

AH=3

CH=hours in BCD

CL=minutes in BCD

DH=seconds in BCD

Read Clock Date

Read the date kept in the clock.

Entry Conditions

AH=4

Exit Conditions

CH=century in BCD

CL=year in BCD

DH=month in BCD

DL=day in BCD

Set Clock Date

Set the date kept in the clock.

Entry Conditions

AH=5

CH=century in BCD

CL=year in BCD

DH=month in BCD

DL=day in BCD

Set Alarm

Entry Conditions

AH=06H

CH=hours in BCD

CL=minutes in BCD

Exit Conditions

CF=0 Alarm set

CF=1 Alarm already set

Note: Place address for alarm routine in INT4AH vector before using this service. And the alarm routine must be created by user.

Reset Alarm

Entry Conditions

AH=07H

Exit conditions

None

Disk I/O Support for Diskette Only

System Configuration

Software Interrupt

13 hex (19 dec)

Function Summary

AH=0:	Reset diskette
AH=1:	Return status of last diskette operation
AH=2:	Read sector(s) from diskette
AH=3:	Write sector(s) to diskette
AH=4:	Verify sector(s) on diskette
AH=5:	Format track on diskette
AH=08H:	Read drive parameters
AH=15H:	Read DASD type
AH=16H:	Diskette change line status

Function Descriptions

Reset Diskette

Reset the diskette system. Resets associated hardware and recalibrates all diskette drives.

Entry Conditions

AH=0

Exit Conditions

See the following "Exits From All Calls."

Return Status of Last Diskette Operation

Returns the diskette status of the last operation in AH.

Entry Conditions

AH=1

Exit Conditions

AL=*status of the last operation*. For values, see the following "Exits From All Calls."

Read Sector(s) from Diskette

Read the desired sector(s) from the diskette into RAM.

Entry Conditions

AH=2

DL=*drive number* (0)

DH=*head number* (0-1)

CH=*track number* (0-79)

CL=*sector number* (1-9)

AL=*sector count* (1-9)

ES:BX=*pointer to disk buffer*

Exit Conditions

See the following "Exits From All Calls."

AL=*number of sectors read*

Write Sector(s) to Diskette

Write the desired sector(s) from RAM to disk.

Entry Conditions

AH=3

DL=*drive number* (0)

DH=*head number* (0-1)

CH=*track number* (0-79)

CL=*sector number* (1-9)

AL=*sector count* (1-9)

ES:BX=*pointer to disk buffer*

Exit Conditions

See the following "Exits From All Calls."

AL=*number of sectors written*

Verify Sector(s) on Diskette

Verify the desired sector(s) are readable.

Entry Conditions

AH=4

DL=*drive number* (0)

DH=*head number* (0-1)

CH=*track number* (0-79)

CL=*sector number* (1-9)

AL=*sector count* (1-9)

Exit Conditions

See the following "Exits From All Calls."

AL=*number of sectors verified*

Format on Diskette

Format the desired track.

Entry Conditions

AH=5

AL=*sector count* (1-9)

DL=*drive number* (0)

DH=*head number* (0-1)

CH=*track number* (0-79)

CL=*sector number* (1-9)

ES:BX=*pointer to a group of address fields for each track*. Each address field is made up of 4 bytes.

These are C, H, R, and N, where:

C=*track number*

H=*head number*

R=*sector number*

N=*the number of bytes per sector*

(00=128, 01=256, 02=512, 03=1024)

There is one entry for every sector on a given track.

Exit Conditions

See the following "Exits From All Calls."

Read Drive Parameters

Return the drive parameters.

Entry Conditions

AH=08H

DL=*drive number* (0)

Exit Conditions

AX=0

BH=0

CH=Maximum usable track number

CL=Maximum usable sector number

DH=Maximum usable head number

DL=Number of diskette drives installed

ES:D1=Pointer to diskette drive parameter table for the maximum media type supported on the specified drive.

CF=0: No error
CF=1: Illegal parameter

Read DASD Type

Return the change line status.

Entry Conditions

AH=15H
DL=*drive number* (0-1)

Exit Conditions

CF= 1: Operation was not successful.
AH= 1: Invalid command.
CF= 0: Operation was successful.
AH= 0: Drive not present
 = 1: Diskette, no change line available
 = 2: Diskette, change line available

Diskette Change Line Status

Return the status of the diskette change line.

Entry Conditions

AH=16H
DL=*drive number* (0)

Exit Conditions

CF= 0: If AH=0
CF= 1: If AH is non 0
AH= 0: Diskette change signal not active
 = 1: Invalid diskette parameter
 = 6: Diskette change signal active
 = 80: Diskette drive not ready (drive door is open)

Exits From All Calls

AH=*Status of operation*, where set=true

Error Code	Condition
01H	Illegal Function
02H	Address Mark Not Found
03H	Write Protect Error
04H	Sector Not Found
06H	Diskette Change Line Active
08H	DMA Overrun
09H	Attempt to DMA Across a 64K Boundary
10H	Bad CRC on Disk Read
20H	Controller Failure
40H	Seek Failure
80H	Device Timeout, Device Failed to Respond

[NC]= operation successful (AH=0)

[C]= operation failed (AH=error status)

Equipment

This service returns the "equipment flag" (hardware configuration of the computer system) in the AX register.

Software Interrupts

11 hex (17 dec)

The "equipment flag" returned in the AX register has the following meanings for each bit:

Reset=the indicated equipment is not in the system

Set=the indicated equipment is in the system

Bit 0=diskette installed

(Bit 1=math coprocessor)

Bits 2, 3 always=11

Bits 4, 5 *initial video mode*

01 40×25 Color

10 80×25 Color

(11 80×25 Monochrome)

Bits 6, 7 *number of diskette drives* (only if Bit 0=1)

00 1

(01 2

10 3 (Tandy 1000 TL ONLY))

Bit 8 0=DMA present (always present)

1=no DMA present

Bits 9, 10, 11 *number of RS-232C cards*

Bit 12 game I/O adapter present (joystick)

Bit 13 not used

Bit 14, 15 *number of printers*

Memory Size

This service returns the total number of kilobytes of RAM in the computer system (contiguous starting from Address 0) in the AX register. The maximum value returned is 640.

Software Interrupts

12 hex (18 dec)

Bootstrap Loader

Track 0, Sector 1 is read into Segment 0, Offset 7C00.

Control is then transferred as follows: (CS)=0000H

(IP)=7C00H

(DL)=drive where bootstrap sector was read

Software Interrupts

19 hex (25 dec)

System Services

Software Interrupts

15 hex (21 dec)

Function Summary

AH=C0H: Machine identification
AH=15H: Read and write EEPROM data

Machine Identification

The machine identification algorithm is the same as all previous Tandy 1000's. As well, the Tandy 1000 SL and Tandy 1000 TL computers have a new BIOS call to further identify the machine.

All current and previous Tandy 1000 computers have the following machine identification:

Byte at address FFFF:E=FF hex

(compatible with IBM PC)

Byte at address FC000:0=21 hex (Tandy 1000 unique)

Entry Conditions

AH=C0H

Exit Conditions

If CF=0

ES:BX= pointer to machine identification data in ROM

DW 0003 Byte count of data that follows (always 3)

DB xx Model ID

DB xx Submodel ID

DB xx BIOS revision level

If CF=1, the call is not supported (all previous versions of the Tandy 1000)

	Tandy 1000 SL	Tandy 1000 TL	1100 FD
Model ID	FF	FF	FF
Submodel ID	00	01	30
BIOS revision level	xx	xx	xx

EEPROM/E0000 ROM

Read From EEPROM

Read the 16-bit value from the indicated EEPROM word.

Entry Conditions

AH=70H

AL=0

BL=word number to read (0-63)

Exit Conditions

DX=word value

Carry flag set indicates EEPROM call not supported.

Write to EEPROM

Write a 16-bit value to the indicated EEPROM word.

Entry Conditions

AH=70H

AL=1

BL=word number to write (0-63)

DX=word value to write

Exit Conditions

Carry Flag set indicates EEPROM call not supported.

Get E0000 ROM PAGE

Entry Conditions

AH=70H

AL=02H

Exit Conditions

AL=Page # (0-7)

Set E0000 ROM PAGE

Entry Conditions

AH=70H

AL=03H

DL=Page # (0-7)

Exit Conditions

CF=0 no error

CF=1 invalid page #.

ROM BIOS Data Area

The following table gives the starting offset, and length of each BIOS device driver. This area is located at segment 40:00.

Comm card address	0000	8 (1 word per card)
Printer addresses	0008	8 (1 word per printer)
Devices installed	0010	2 (16 bits)
Not used	0012	1
Memory size	0013	2 (1 word)
I/O channel RAM size	0015	2 (1 word)
KBD data area	0017	39
Disk data area	003E	11
Video data area	0049	30
Not used	0067	5
Clock data area	006C	5
KBD Break & Reset flags	0071	3
Not used	0074	4
Printer timeout counter	0078	4 (1 byte per printer)
Comm timeout counter	007C	4 (1 byte per card)
KBD extra data area	0080	4 (2 words)

The structure and usage of the Video driver RAM data area is as follows:

HEX Offset From Segment 0040:0000	Length and Intended Use	
49H	1 byte-	current CRT mode (0-7)
4AH	1 word-	screen column width
4CH	1 word-	byte length of screen
4EH	1 word-	address/offset of beginning of current display page
50H	8 words-	row/col coordinates of the cursor for each of up to 8 display pages
60H	1 word-	current cursor type (See "Set Cursor Type" for correct encoding)
62	1 byte-	current display page
65H	1 word-	base address+4 of the CRT controller card
66H	1 byte-	copy of value written to the Mode Select Register
66H	1 byte-	current color palette setting

The equipment check BIOS call (INT 11H) and memory size BIOS call (INT 12H) return information from the following data areas:

HEX Offset From Segment 0040:0000	Length and Intended Use	
10H	Devices installed word	
13H	Memory installed word	

The structure and usage of the diskette driver RAM data area is as follows:

HEX Offset From Segment 0040:0000	Length and Intended Use	
3EH	1 byte-	drive recalibration status—bit 3-0, if 0 then drive 3-0 needs recalibration before next Seek. Bit 7 indicates interrupt occurrence
3FH	1 byte-	motor status—Bit 3-0 drive 3-0 motor is on/off. Bit 7—current operation is write, requires delay
40H	1 byte-	motor turn off timeout counter (see Timer ISR)
41H	1 byte-	disk status—codes are defined as in this section
42H	7 bytes-	7 bytes of status returned by the controller during result phase of operation

Value	Error Condition
01H	Illegal Function
02H	Address Mark Not Found
03H	Write Protect Error
04H	Sector Not Found
06H	Diskette Change Line Active
08H	DMA Overrun
09H	Attempt to DMA Across a 64K Boundary
10H	Bad CRC on Disk Read
20H	Controller Failure
40H	Seek Failure
80H	Device Timeout, Device Failed to Respond

The structure and usage of the RS-232C driver RAM data area is as follows:

HEX Offset From Segment 0040:0000	Length and Intended Use	
00H	4 words-	Base address of each one of 4 possible comm cards
7CH	4 words-	1 word timeout count for each of 4 possible comm cards

The structure and usage of the Keyboard driver RAM data area is as follows:

HEX Offset From Segment 0040:0010	Length and Intended Use	
17	1 byte- Bits	Keyboard shift state flag returned by function 02 7-INSERT state active, 6-CAPS LOCK on/off, 5-NUM LOCK on/off, 4-SCROLL LOCK on/off, 3-ALT key pressed 2-CTRL key pressed 1-Left SHIFT key pressed, 0-Right SHIFT key pressed,
18	1 byte- Bits	Secondary shift state flag, 7-INSERT key pressed, 6-CAPS LOCK pressed, 5-NUM LOCK pressed, 4-SCROLL LOCK NUM LOCK pressed, 4-SCROLL pressed, 4-SCROLL LOCK pressed, 3-Pause on/off, pressed, 3-Pause on/off, 2, 1, 0-not used
19	1 byte-	Used to store ALT keypad entry

HEX Offset From Segment 0040:0000	Length and Intended Use	HEX Offset From Segment 0040:0000	1=External monochrome video installed
1A	1 word- Pointer to beginning of the keyboard buffer		
1C	1 word- Pointer to end of the keyboard buffer		
1E	16- Keyboard buffer (enough for words)	B6H	1 byte Bit 0:0 =Drive C is 5¼"
	15- Type ahead entries	40:C2	1 byte 1 =Drive C is 3½"
			01=ROM drive is A: 02=ROM drive is B: 03=ROM drive is C:
		C6	1 byte ROM paging port 210 image.
		C7	1 byte Initial LCD timeout value (in minutes). Initialized from EEPROM. Used by BIOS when initializing LCD— COUNTER. Value 00 means never timeout.
		C8	1 word Timeout counter (low word, ticks).
		CA	1 word Timeout counter (high word, ticks).
		CB	1 byte Miscellaneous status bits for 1100FD. Bit 7-5 Unused Bit 4 1=Low Power Beeping Enabled. Bit 3 1=NMI has occurred. Bit 2 1=FDC operation in progress. Bit 1 Back light Status (Not supported). Bit 0 FDC standby mode utilization. 0=Never use FDC standby mode. 1=Use FDC standby mode.

The structure and usage of the clock service routine is as follows:

HEX Offset
From Segment
0040:0000

HEX Offset From Segment 0040:0000	Length and Intended Use
6CH	1 word- Least significant 16 bits of clock count
6EH	1 word- Most significant 16 bits of clock count
70H	1 byte- Twentyfour hour rollover flag

Additional Data Area

HEX Offset
From Segment
0040:0000

B0H	2 words international support
B4H	1 byte 0=No monochrome monitor FFH=Monochrome monitor
B5H	1 byte Bit 0:0=Drive A is 5¼" 1=Drive A is 3½" Bit 1:0=Drive B is 5¼" 1=Drive B is 3½" Bit 2:0=Tandy 1000 keyboard layout 1=IBM keyboard layout Bit 3:0=Slow CPU speed mode 1=Fast CPU speed mode Bit 4:0=Internal color video support enabled 1=Internal color video support disabled, external color video enabled Bit 5:0=No external monochrome video installed

CC 1 word Counter used for beeping when LOW Power.

EEPROM Definition for BIOS

1100FD BIOS Use of EEPROM

Word 0

- Bit 0—Boot disk override
 - 0—No override
 - 1—Override
- Bit 1—Boot disk override drive
 - 0—Override to drive 0
 - 1—Override to drive 1 (see note 1)
- Bits 10:8—Initial LCD timeout interval
 - 000— Never timeout
 - 001— 1 minute
 - 010— 2 minutes
 - 011— 4 minutes
 - 100— 8 minutes
 - 101— 16 minutes
 - 110— 32 minutes
 - 111— 64 minutes
- Bit 11—Initial FDC standby mode use
 - 0—Never use standby mode
 - 1—Use standby mode

Not Used

- Bit 13—Initial backlight power
 - 0—Backlight off
 - 1—Backlight on

Word 1

- Bit 2—Drive swap
 - 0—Do not swap drives
 - 1—Swap drives 0 and 1 in hardware (see note 1)
- Bit 5—Memory diagnostics
 - 0—Do not test memory unless reset flag is hex 4321
 - 1—Always test memory
- Bit 7—Attached monitor
 - 0—Color
 - 1—Monochrome

BIOS uses this only when both CGA and MDA are detected.

- Bit 11—Serial port address assignment
 - 0—primary: RS-232C secondary: MODEM
 - 1—primary: MODEM secondary: RS-232C

Word 2

- Bits 1:0—Number of floppies installed
 - 00—1 drive
 - 01—2 drives
 - 10—3 drives
 - 11—reserved
- Bits 7:4—Drive 0 type
 - 0000—Not installed
 - 0001—5.25" 360 Kb
 - 0010—5.25" 1.2 Mb (not valid for this BIOS)
 - 0011—3.5" 720 Kb
 - 0100—3.5" 1.44 Mb (not valid for this BIOS)
 - else—reserved
- Bits 11:8—Drive 1 type
- Bits 15:12—Drive 2 type

Note 1)

For drive swapping there must be hardware support. The BIOS attempts to swap drives through port hex 3F1.

Port 3F1

- Bit 1
 - 0—No drive swap
 - 1—Swap drives 0 and 1

