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Hardware Reference
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Technical Reference

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Personal Computer PC*jr*
Hardware Reference
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Technical Reference

First Edition Revised (November 1983)

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Preface

The IBM PC*jr* Technical Reference manual describes the hardware design and provides interface information for the IBM PC*jr*. This publication also has information about the basic input/output system (BIOS) and programming support.

The information in this publication is both descriptive and reference oriented, and is intended for hardware and software designers, programmers, engineers, and interested persons who need to understand the design and operation of the IBM PC*jr* computer.

You should be familiar with the use of the IBM PC*jr*, and understand the concepts of computer architecture and programming.

This manual has five sections:

Section 1: "Introduction" is an overview of the basic system and available options.

Section 2: "Base System" describes each functional part of the base system. This section also has specifications for power, timing, and interfaces. Programming considerations are supported by coding tables, command codes, and registers.

Section 3: "System Options" describes each available option using the same format as Section 2: "Base System."

Section 4: "Compatibility with the IBM Personal Computer Family" describes programming concerns for maintaining compatibility between the IBM PC*jr* and the other IBM Personal Computers.

Section 5: "System BIOS and Usage" describes the basic input/output system (BIOS) and its use. This section also contains the software interrupt listing, a system memory map, descriptions of vectors with special meanings, and a set of low-storage maps. In addition, keyboard encoding and usage is discussed.

This publication has four appendixes:

Appendix A: "ROM BIOS Listing"
Appendix B: "Logic Diagrams"
Appendix C: "Characters, Keystrokes, and Color"
Appendix D: "Unit Specifications"

Prerequisite Publication:

Guide to Operations part number 1502291

Guide to Operations part number 1502292

Suggested Reading:

IBM PCjr Hands on BASIC part number 1504702
IBM PCjr BASIC Reference Manual part number 6182371
Disk Operating System (DOS) part number 6024061
Hardware Maintenance and Service Manual part number 1502294
Macro Assembler part number 6024002

Related publications are listed in "Bibliography."

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SECTION 1. INTRODUCTION

Contents

Introduction **1-3**

Notes:

Introduction

The system unit, a desk top transformer, and a cordless keyboard make up the hardware for the PC*jr* base system.

The following options are available for the base system:

- IBM PC*jr* 64KB Memory and Display Expansion
  - The 64KB Memory and Display Expansion enables the user to work with the higher density video modes while increasing the system's memory size by 64K Bytes to a total of 128K Bytes.
- IBM PC*jr* Diskette Drive Adapter
  - The IBM PC*jr* Diskette Drive Adapter permits the attachment of the IBM PC*jr* Diskette Drive to the IBM PC*jr* and resides in a dedicated connector on the IBM PC*jr* system board.
- IBM PC*jr* Diskette Drive
  - The IBM PC*jr* Diskette Drive is double-sided with 40 tracks for each side, is fully self-contained, and consists of a spindle drive system, a read positioning system, and a read/write/erase system.
- IBM PC*jr* Internal Modem
  - The IBM PC*jr* Internal Modem is an adapter that plugs into the PC*jr* system board modem connector and allows communications over standard telephone lines.

- IBM PC*jr* Parallel Printer Attachment

  - The IBM PC*jr* Parallel Printer Attachment is provided to attach various I/O devices that accept eight bits of parallel data at standard TTL logic levels. It attaches as a feature to the right side of the system unit.

- IBM Personal Computer Graphics Printer

  - IBM Graphics Printer is an 80 cps (characters-per-second), self-powered, stand-alone, tabletop unit.

- IBM PC*jr* Joystick

  - The IBM PC*jr* Joystick is an input device to provide the user with two-dimensional positioning-control. Two pushbutton switches on the joystick give the user additional input capability.

- IBM Color Display

  - The IBM Color Display is a Red/Green/Blue /Intensity (RGBI) Direct-Drive display, that is independently housed and powered.

- IBM Connector for Television

  - The IBM Connector for Television allows a TV to be connected to the IBM PC*jr* system.

- IBM PC*jr* Keyboard Cord

  - The IBM PC*jr* Keyboard Cord option is used to connect the IBM PC*jr* Cordless Keyboard to the system board.

- IBM PC*jr* Adapter Cable for Serial Devices

  – This option is an adapter cable that allows connection of serial devices to the IBM PC*jr* system board.

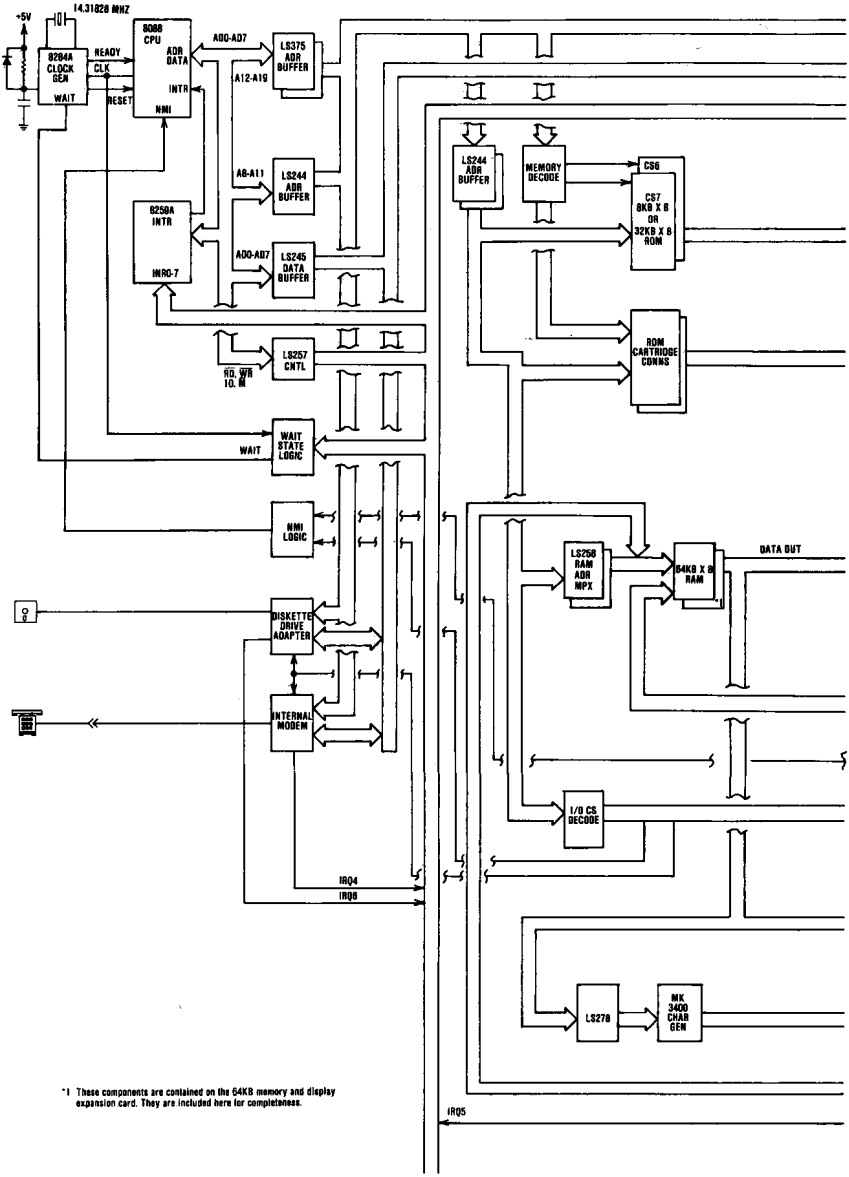
- IBM PC*jr* Adapter Cable for Cassette

  – This option is an adapter cable that allows a cassette recorder to be connected to the IBM PC*jr*.

- IBM PC*jr* Adapter Cable for Color Display

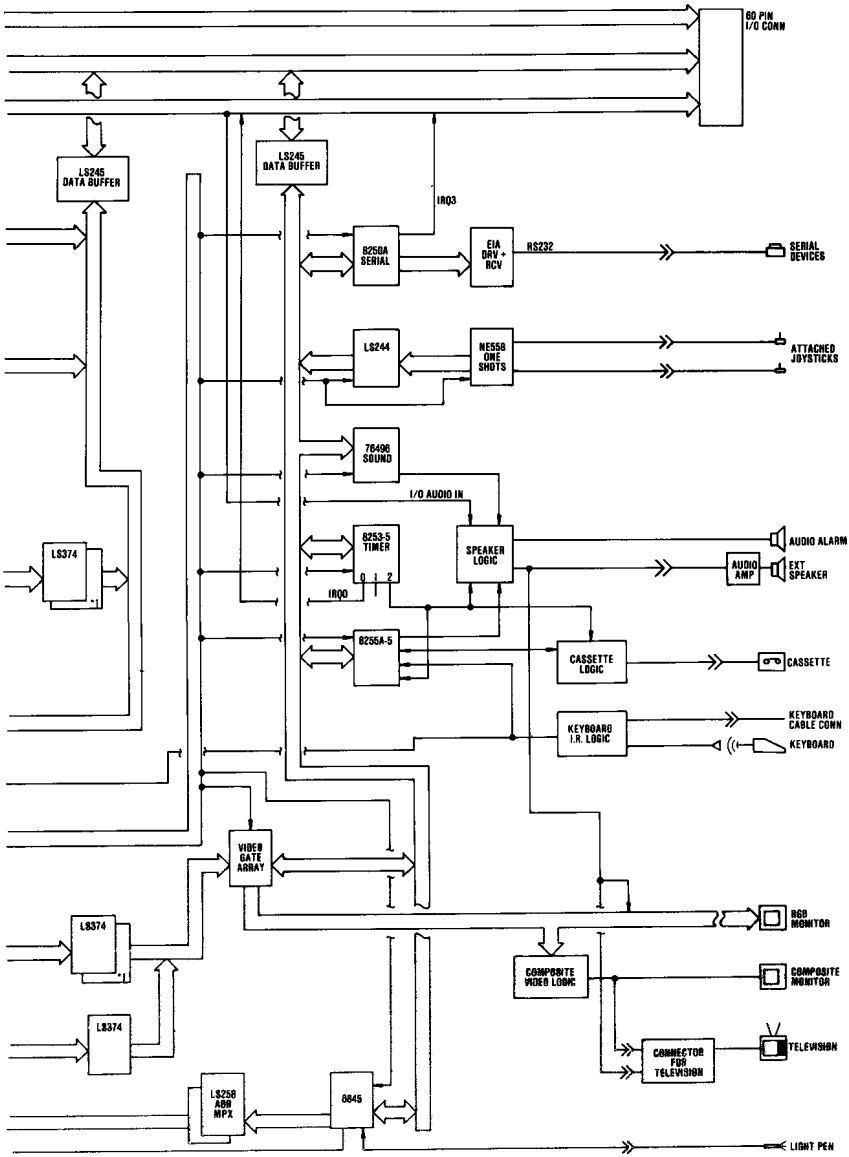
  – This adapter cable allows the IBM Color Display to be connected to the IBM PC*jr*.

The following is a block diagram of the IBM PC*jr* system.



*1 These components are contained on the 64KB memory and display expansion card. They are included here for completeness.

System Block Diagram (Sheet 1 of 2)



*1 These components are contained on the 64K6 memory and display expansion card. They are included here for completeness.

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Notes:

Introduction

The PC*jr* base-system hardware consists of the system unit, a 62-key cordless-keyboard, and a power transformer.

The PC*jr* system board is the center of the PC*jr* system unit. The system board fits horizontally in the base of the system unit and is approximately 255 mm by 350 mm (10 inches by 13.8 inches). It is double-sided, with an internal-power/ground plane. Low voltage ac power enters the power supply adapter, is converted to dc voltage, and enters the system board through the power supply adapter edge-connector. Other system board connectors provide interfaces for a variety of input/output (I/O) devices and are individually keyed to prevent improper installation. The following is a list of these connectors:

- 64KB Memory and Display Expansion Connector
- Diskette Drive Adapter Connector
- Internal Modem Connector
- Infra-Red (IR) Link Receiver Board Connector
- Program Cartridge Connectors (2)
- I/O Channel Expansion Connector
- Serial Port (RS232) Connector (with optional adapter cable)
- Direct Drive (RGBI) Video Connector
- Composite Video Connector
- IBM Connector for Television Connector (external RF modulator)
- Light Pen Connector
- External Audio Connector
- IBM PC*jr* Keyboard Cord Connector
- Cassette Connector (with optional adapter cable)
- IBM PC*jr* Attachable Joystick Connectors (2)

The system board consists of seven functional subsystems: the processor subsystem and its support elements, the read-only (ROM) subsystem, the read/write (R/W) subsystem, the audio subsystem, the video subsystem, the games subsystem, and the I/O channel. All are described in this section.

The nucleus of the system board is the Intel 8088 microprocessor. This processor is an 8-bit external bus version of Intel's 16-bit 8086 processor, and is software-compatible with the 8086. The 8088 supports 16-bit operations, including multiplication and division, and supports 20 bits of addressing (1 megabyte of storage). It operates in the minimum mode at 4.77 MHz. This frequency, which is derived from a 14.31818-MHz crystal, is divided by 3 for the processor clock, and by 4 to obtain the 3.58-MHz color-burst signal required for color televisions.

For additional information about the 8088, refer to the publications listed in "Bibliography".

The processor is supported by a set of high-function support-devices providing three 16-bit timer-counter channels, and nine prioritized-interrupt levels.

The three programmable timer/counters are provided by an Intel 8253-5 programmable interval-timer and are used by the system in the following manner: Channel 0 is used as a general-purpose timer providing a constant time-base for implementing a time-of-day clock; Channel 1 is used to deserialize the keyboard data and for time-of-day overflow during diskette operations. Channel 2 is used to support the tone generation for the audio speaker and to write data to the cassette.

Of the nine prioritized levels of interrupt, three are bused to the system's I/O channel for use by adapters. Five levels are used on the system board. Level 0, the

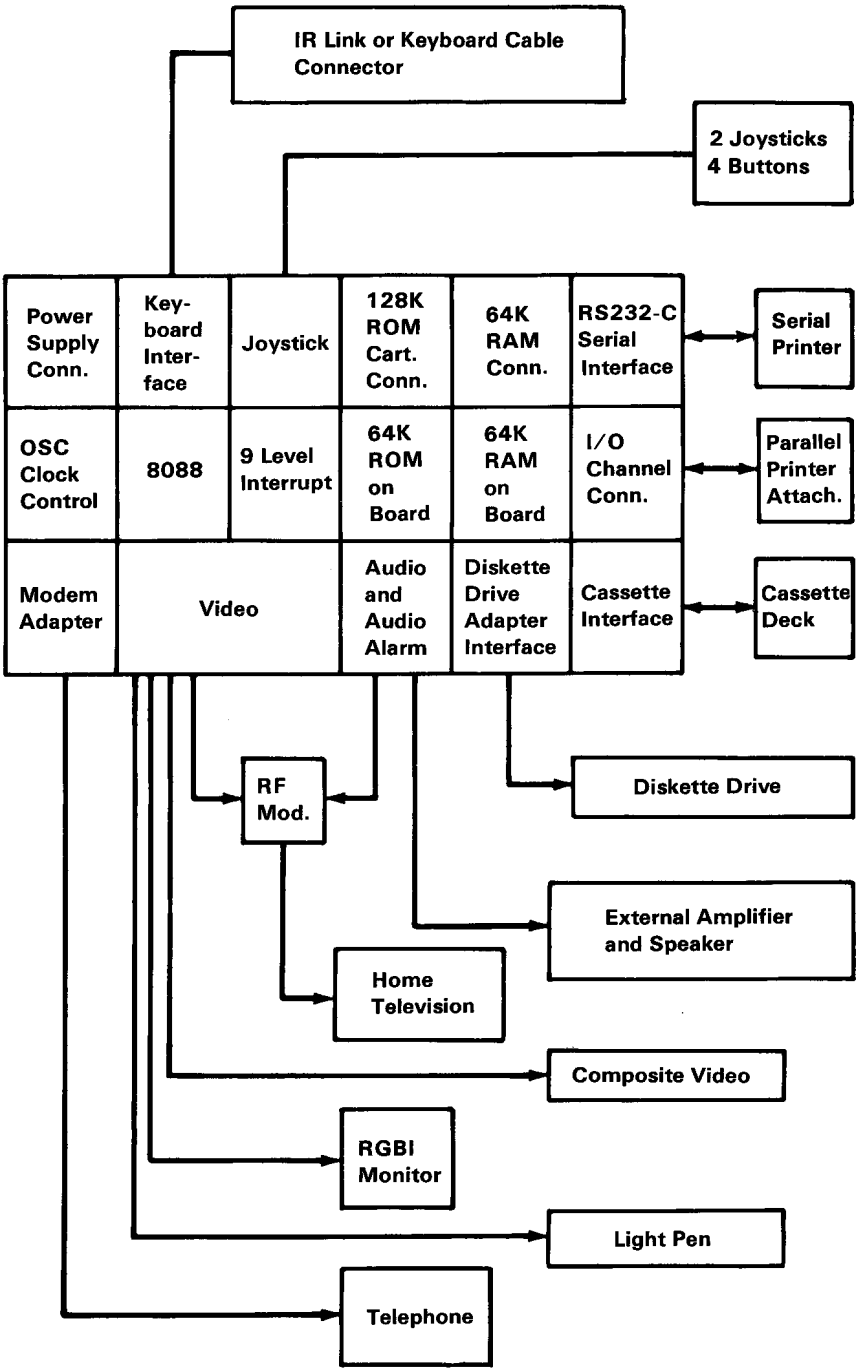
highest priority, is attached to Channel 0 of the timer/counter and provides a periodic interrupt for the time-of-day clock; level 3 is the serial-port-access interrupt; level 4 is the modem-access interrupt; level 5 is the vertical-retrace interrupt for the video; and level six is the diskette drive adapter-access interrupt. The non-maskable interrupt (NMI) of the 8088 is attached to the keyboard-interface circuits and receives an interrupt for each scan code sent by the keyboard.

The system board supports both read-only memory (ROM) and R/W memory (RAM). It has space for 64K bytes by 8 bits of ROM. There are two module sockets that accept a 32K byte by 8 bit ROM module. ROM is aligned at the top of the 8088's address space. This ROM contains the Power-On Self-Test, cassette-BASIC interpreter, cassette-operating system, I/O drivers, dot patterns for 256 characters in graphics mode, a diskette bootstrap-loader and user-selectable diagnostic-routines.

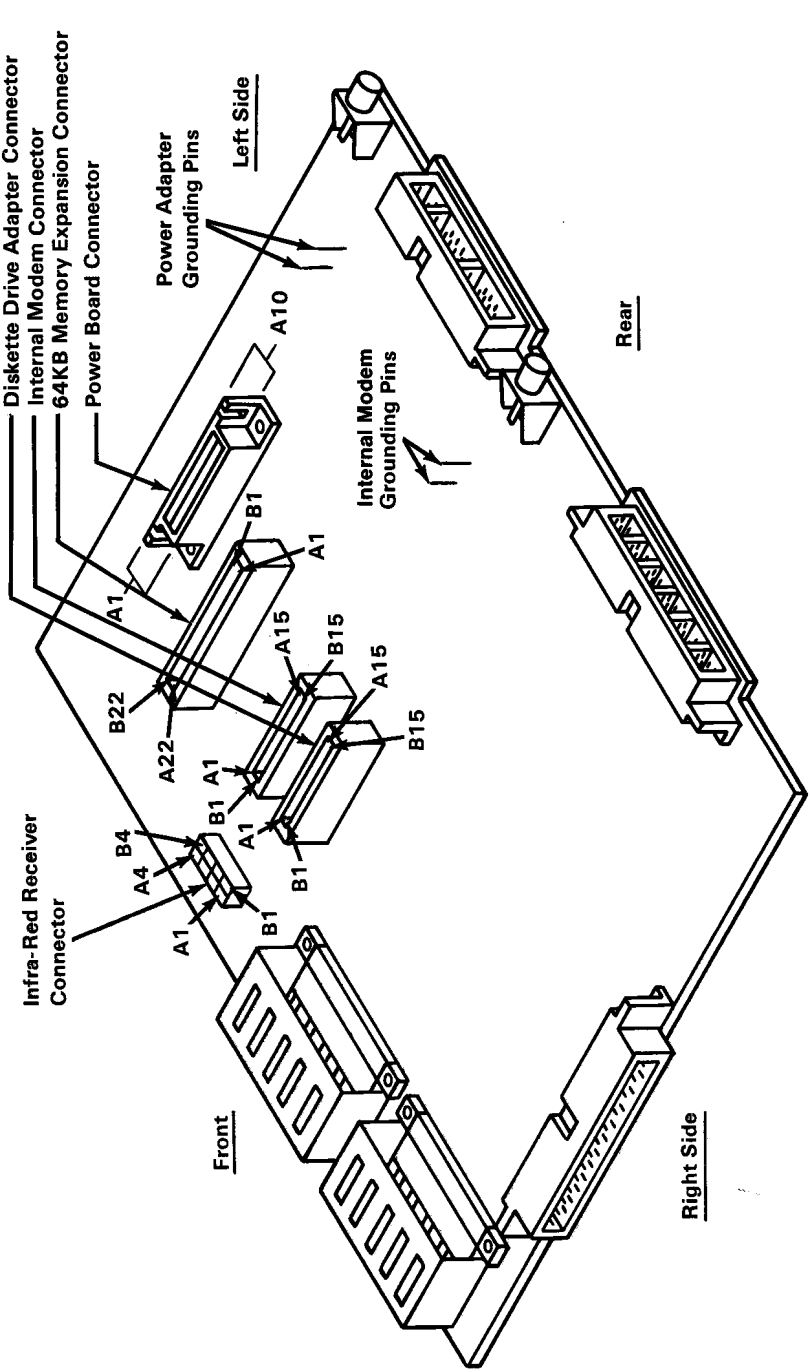
The system board contains the following major functional components:

- 8088 Microprocessor
- 64K ROM
- 128K ROM Cartridge Interface
- 64K Dynamic RAM
- 64KB Memory and Display Expansion Interface
- Serial Port (RS232)
- Audio Alarm (Beeper)
- Sound Subsystem
- Cassette Interface
- Joystick Interface
- Keyboard Interface
- Modem Interface
- Diskette Interface
- Video/Graphics Subsystem
- Light Pen Interface
- I/O Expansion Bus
- 9-Level Interrupt

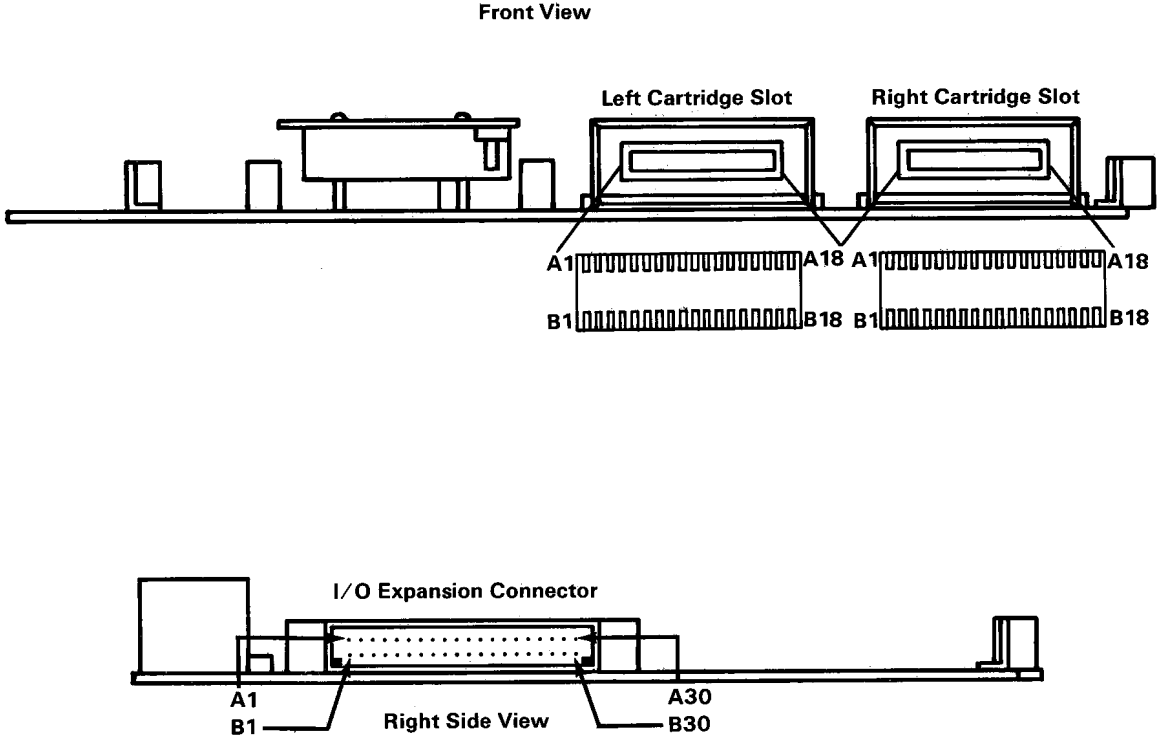
The following is a block diagram of the System Board.



System Board Block Diagram



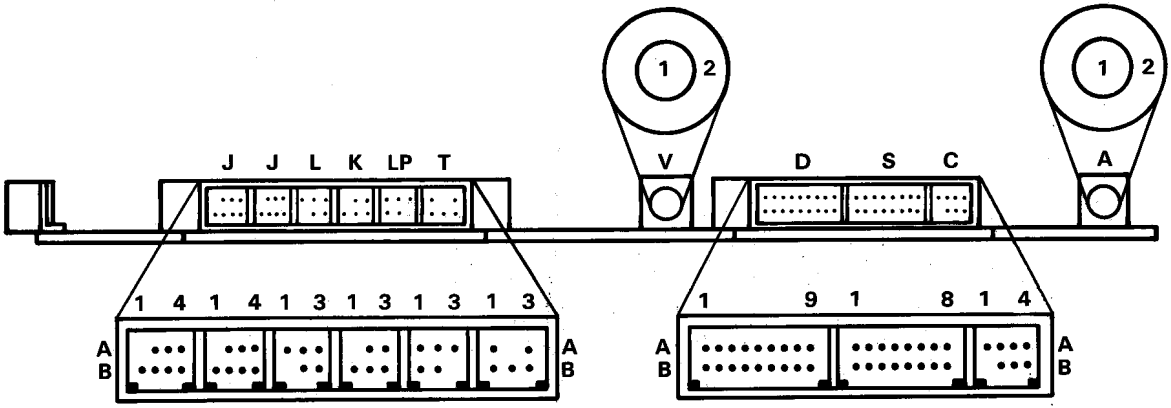
System Board Connector Specifications (Part 1 of 3)



System Board Connector Specifications (Part 2 of 3)

Letter Designation	Connector Use
J	Left Joystick
J	Right Joystick
L	Spare
K	Keyboard
LP	Light Pen
T	Television

Letter Designation	Connector Use
V	Composite Video
D	Direct Drive Video
S	Serial Device
C	Cassette
A	Audio



System Board Connector Specifications (Part 3 of 3)

Processor and Support

The (R) Intel 8088 Microprocessor is used as the system's central processor. Some of its characteristics are:

- 4.77 MHz clock
- 20 bit address bus
- 8-bit memory interface
- 16-bit ALU (arithmatic/logic unit) and registers
- Extensive instruction set
- DMA and interrupt capabilities
- Hardware fixed-point multiply and divide

The system clock is provided by one Intel 8284A clock chip. The 8088 is operated in the minimum mode.

Performance

The 8088 is operated at 4.77 MHz which results in a clock cycle-time of 210 ns.

Normally four clock cycles are required for a bus cycle so that an 840 ns ROM memory cycle time is achieved. RAM write and read cycles will incur an average of two wait states because of sharing with video, leading to an average of six clock cycles. I/O reads and writes also take six clock cycles leading to a bus cycle time of 1.260 μs.

Notes:

PC*jr* Hardware Interrupts

Nine hardware levels of interrupts are available for the PC*jr* system. The highest-priority interrupt is the NMI interrupt in the 8088. The NMI is followed by eight prioritized interrupt-levels (0-7) in the 8259A Programmable Interrupt Controller, with IRQ 0 as the highest and IRQ 7 as the lowest. The interrupt level assignments follow:

Level		Function
8088	NMI	Keyboard Interrupt
8259A	IRQ 0	Timer Clock Interrupt
8259A	IRQ 1	I/O Channel (Reserved)
8259A	IRQ 2	I/O Channel
8259A	IRQ 3	Asynchronous Port Interrupt (RS-232C)
8259A	IRQ 4	Modem Interrupt
8259A	IRQ 5	Vertical Retrace Interrupt (Display)
8259A	IRQ 6	Diskette Interrupt
8259A	IRQ 7	I/O Channel (Parallel Printer)

Hardware Interrupts

8259A Programming Considerations

The 8259A is set up with the following characteristics:

- Buffered Mode
- 8086 Mode
- Edge Triggered Mode
- Single Mode Master (No Cascading is Allowed)

The 8259A I/O is located at I/O address hex 20 and hex 21. The 8259A is set up to issue interrupt types hex 8 to hex F which use pointers to point to memory address hex 20 to hex 3F.

The following figure is an example setup.

0263 BO 13	MOV AL, 13H	; ICW1 - Reset edge sense circuit set single ; 8259 Chip and ICW4 read
0265 E6 20	OUT INTA00,AL	
0267 BO 08	MOV AL,8	; ICW2 - Set interrupt type 8 (8-F)
0269 E6 21	OUT INTA01,AL	
026B BO 09	MOV AL,9	; ICW4 - Set buffered mode/master and 8086 mode
026D E6 21	OUT INTA01,AL	

Example Set Up

64K RAM

The 64K bytes of R/W memory reside on the system board and require no user configuration.

Eight 64K byte by 1, 150 ns, dynamic memory modules are used to provide 64K byte of storage. The RAM has no parity. Sources of these memory modules include the Motorola MCM6665AL15 and the Texas Instruments TMS4164-15 or equivalent.

The system board 64K RAM is mapped at the bottom of the 1 MEG address space. The system board 64K RAM is mapped to the next 64K bytes of address space if the 64KB Memory and Display Expansion option is not installed. If read or written to, this higher block of address space will look just like the low-order 64K-byte block. This means the bottom 128K bytes of address space is always reserved for RAM. If the 64KB Memory and Display Expansion option is installed, it is mapped to the 'ODD' memory space within the 128K byte-reserved space while the system board memory is mapped to the 'EVEN' space. Memory refresh is provided by the 6845 CRT Controller and gate array. The gate array cycles the RAM and resolves contention between the CRT and processor cycles.

See "IBM PC*jr* 64KB Memory and Display Expansion" in Section 3 for a detailed description.

Notes:

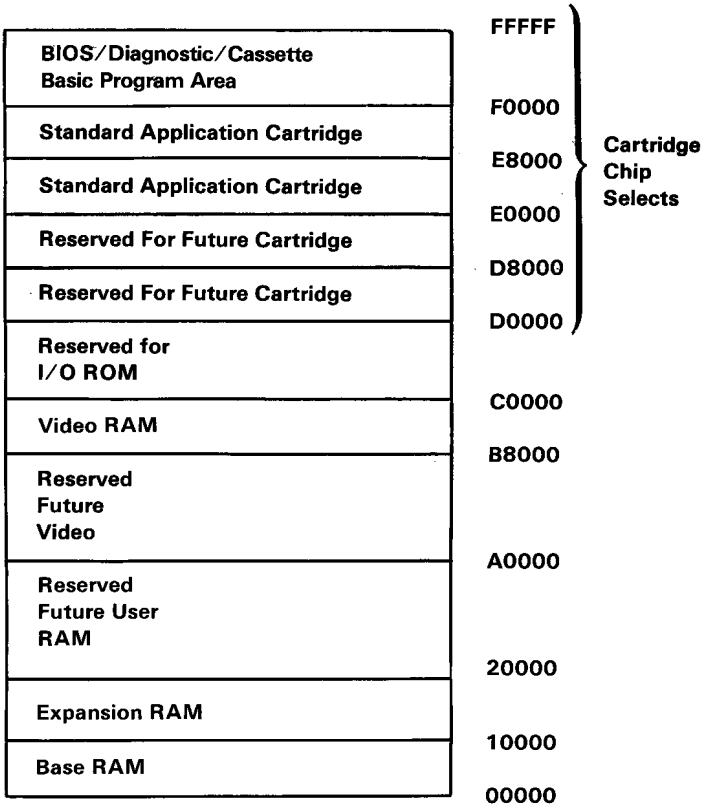
ROM Subsystem

The ROM subsystem is made up of 64K bytes of ROM aligned at the top of the 1 MEG address space. The ROM is built using 32K byte by 8 ROM-modules. The ROM has no parity. The general memory specifications for the ROM are:

```
Access Time  -  250 ns
Cycle Time   -  375 ns
```

ROM modules Mk 38000 from Mostek, TMM23256P or equivelent are used. Address A14 is wired to both pin 1 and pin 27.

The following figure is a map of the sections of memory allocated for use by the system:


BIOS/Diagnostic/Cassette
Basic Program Area
Standard Application Cartridge
Standard Application Cartridge
Reserved For Future Cartridge
Reserved For Future Cartridge
Reserved for
I/O ROM
Video RAM
Reserved
Future
Video
Reserved
Future User
RAM
Expansion RAM
Base RAM
FFFFF
F0000
E8000
E0000
D8000
D0000
C0000
B8000
A0000
20000
10000
00000
Cartridge
Chip
Selects

Memory Map

Input Output Channel

The Input/Out channel (I/O) is an extension of the 8088 microprocessor bus. It is however, demultiplexed, repowered, and enhanced by the addition of interrupts.

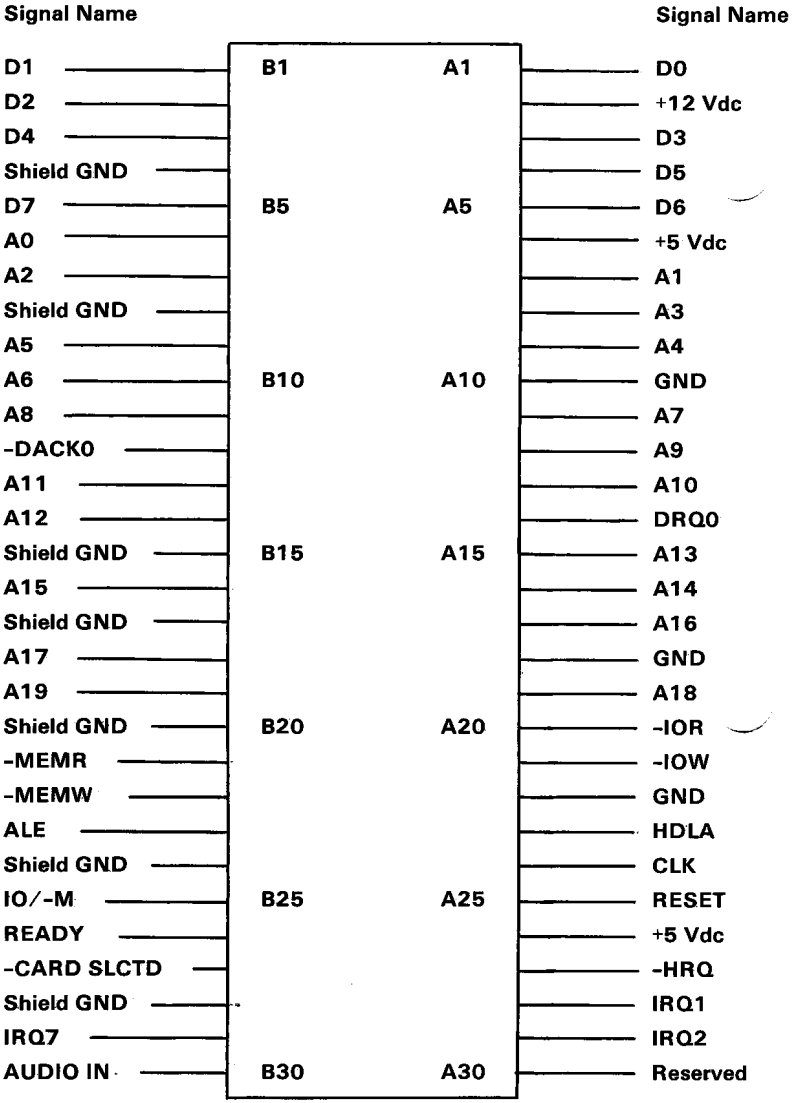
The I/O channel contains an 8-bit bidirectional bus, 20 address lines, 3 levels of interrupt, control lines for memory and I/O read or write, clock and timing lines, and power and ground for the adapters. Voltages of +5 dc and +12 dc are provided for external adapters. Any additional power needs will require a separate power-module.

All I/O Channel functions are bused to the right-hand side of the system unit and are provided by a right-angle, 60-pin connector. Each external adapter connects to the I/O bus and passes the bus along for the next attachment.

A 'ready' line is available on the I/O Channel to allow operation with slow I/O or memory devices. If the channel's 'ready' line is not activated by an addressed device, all processor-generated memory-read and write cycles take four 210-ns clocks or 840-ns/byte. All processor-generated I/O-read or write cycles require six clocks for a cycle time of 1.26-μs/byte.

The I/O Channel also contains the capability to add bus masters to the channel. These devices could be DMA devices or alternate processors.

The I/O Channel signals have sufficient drive to support five I/O Channel expansion-adapters and the internal modem and diskette drive adapter, assuming one standard TTL load per attachment. For information on power available for external adapters, see "System Power Supply", later in this Section.

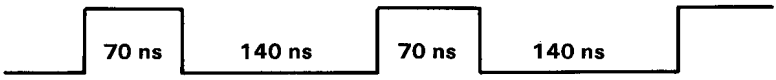


I/O Channel Expansion Connector Specifications

System Board I/O Channel Description

The following is a description of the I/O Channel. All signals are TTL compatible.

Signal	I/O	Description
CLK	O	System Clock: It is a divide-by-three of the 14.31818 MHz oscillator and has a period of 210 ns (4.77 MHz). The clock has a 33% duty cycle.



Duty Cycle

RESET	O	This line is used to reset or initialize system logic upon power-up. This line is synchronized to the falling edge of the clock and is 'active high'. Its duration upon power up is 26.5 μs.
A0-A19	I/O	Address Bits 0 to 19: These lines are used to address memory and I/O devices within the system. The 20 address lines allow access of up to 1 megabyte of memory. A0 is the least-significant- bit (LSB) while A19 is the most-significant-bit (MSB). These lines are normally driven by the 8088 microprocessor as

		outputs, but can become inputs from an external bus-master by issuing an HRQ and receiving an HLDA.
D0-D7	I/O	Data Bits 0-7: These lines provide data-bus bits 0 to 7 for the processor, memory, and I/O devices. D0 is the least-significant-bit (LSB) and D7 is the most-significant-bit (MSB). These lines can be controlled by an external bus-master by issuing an HRQ and receiving an HLDA.
ALE	O	Address Latch Enable: This line is provided to allow the addition of wait states in memory and I/O cycles.
READY	I	This line, normally 'high' ('ready'), is pulled 'low' ('not ready') by a memory or I/O device to lengthen I/O or memory cycles. It allows slower devices to attach to the I/O Channel with a minimum of difficulty. Any slow device requiring this line should drive it 'low' immediately upon detecting a valid address and IO/-M signal. Machine cycles (I/O and memory) are extended by an integral number of CLK cycles (210 ns). Any bus master on the I/O Channel should also honor this 'ready' line. It is pulled 'low' by the system board

		on memory read and write cycles and outputting to the sound subsystem.
IRQ1, IRQ2, IRQ7	I	Interrupt Request 1, 2, and 7: These lines are used to signal the processor that an I/O device requires attention. They are prioritized with IRQ1 as the highest priority and IRQ7 as the lowest. An Interrupt Request is generated by raising an IRQ line ('low' to 'high') and holding it 'high' until it is acknowledged by the processor (interrupt-service routine).
-IOR	I/O	I/O Read Command: This command line instructs an I/O device to drive its data onto the data bus. This signal may be driven by the 8088 microprocessor or by an external bus-master after it has gained control of the bus. This line is active 'low'.
-IOW	I/O	I/O Write Command: This command line instructs an I/O device to read the data on the data bus. This signal may be driven by the 8088 microprocessor or by an external bus-master after it has gained control of the bus. This line is active 'low'.
-MEMR	I/O	Memory Read Command: This command line instructs the

		memory to drive its data onto the data bus. This signal may be driven by the 8088 microprocessor or by an external bus-master after it has gained control of the bus. This line is active 'low'.
-MEMW	I/O	Memory Write Command: This command line instructs the memory to store the data present on the data bus. This signal may be driven by the 8088 microprocessor or by an external bus-master after it has gained control of the bus. This line is active low.
IO/-M	I/O	I/O or Memory Status: This status line is used to distinguish a memory access from an I/O access. This line should be driven by a bus master after it has gained control of the bus. If this line is 'high' it indicates an I/O Address is on the Address Bus; if this line is 'low', it indicates a memory address is on the Address Bus.
-HRQ	I	Hold Request: This line indicates that another bus master is requesting the I/O Channel. To gain bus-master status, a device on the channel must assert -HRQ (active 'low'). The 8088 will respond to a -HRQ by asserting an HLDA. After receiving an HLDA, the new bus master may

		control the bus, and must continue to assert the -HRQ until it is ready to relinquish the bus. A -HRQ is not an asynchronous signal and should be synchronized to the system clock. All channel devices with bus-master capabilities must latch data-bit D4 during any 'Out' instruction to A0-A7. The resulting signal should be used to qualify -HRQ as follows: Latched value = 1 --> -HRQ is inhibited. Latched value = 0 --> -HRQ is allowed. For more detail, see the explanation of the A0 port.
DRQ 0	0	This line comes from the floppy disk controller (FDC) and can be used by an external DMA to indicate that a byte should be transferred to the FDC.
-DACK 0	I	This line should come from an external DMA and should indicate that a byte is being transferred from memory to the FDC.
HLDA	O	Hold Acknowledge: This line indicates to a bus master on the channel that -HRQ has been honored and that the 8088 has floated its bus and control lines.

-CARD SLCTD	I	This line should be pulled down by any adapter when it is selected with address and IO/-M. This line will be used for bus expansion. It is pulled up with a resistor and should be pulled down with an open collector device.
AUDIO IN	I	Channel devices may provide sound sources to the system-board sound-subsystem through this line. It is 1 volt peak-to-peak, dc biased at 2.5 volts above ground.

Hex Range	9	8	7	6	5	4	3	2	1	0	Device
20-27	0	0	0	0	1	0	0	X	X	A0	PIC 8259
40-47	0	0	0	1	0	0	0	0	A1	A0	Timer 8253-5
60-67	0	0	0	1	1	0	0	X	A1	A0	PPI 8255-5
A0-A7	0	0	1	0	1	0	0	X	X	X	NMI Mask Reg.
C0-C7	0	0	1	1	0	0	0	X	X	X	Sound SN76496N
F0-FF	0	0	1	1	1	1	X	A2	A1	A0	Diskette
200-207	1	0	0	0	0	0	0	X	X	X	Joystick
2F8-2FF	1	0	1	1	1	1	1	A2	A1	A0	Serial Port
3D0-3DF	1	1	1	1	0	1	A3	A2	A1	A0	Video Subsystem
3F8-3FF	1	1	1	1	1	1	1	A2	A1	A0	Modem

I/O Map

X = Don't care (that is, not in decode.)

- Any I/O which is not decoded on the system board may be decoded on the I/O Channel.
- At Power-On time the NMI into the 8088 is masked 'off'. This mask bit can be set by system software as follows:

Write to Port A0 D7=ENA NMI D6=IR TEST ENA D5=SELC CLK1 INPUT D4=+Disable HRQ

8255 Bit Assignments

PA Output
PA0 Reserved for Keystroke Storage
PA1 Reserved for Keystroke Storage
PA2 Reserved for Keystroke Storage
PA3 Reserved for Keystroke Storage
PA4 Reserved for Keystroke Storage
PA5 Reserved for Keystroke Storage
PA6 Reserved for Keystroke Storage
PA7 Reserved for Keystroke Storage
PB Output
PB0 +Timer2 Gate (Speaker)
PB1 +Speaker Data
PB2 +Alpha (-Graphics)
PB3 +Cassette Motor Off
PB4 +Disable Internal Beeper and Cassette Motor Relay
PB5 SPKR Switch 0
PB6 SPKR Switch 1
PB7 Reserved
PC Input
PC0 Keyboard Latched
PC1 -Internal MODEM Card Installed
PC2 -Diskette Drive Card Installed
PC3 -64KB Memory and Display Expansion Installed
PC4 Cassette Data In
PC5 Timer Channel 2 Output
PC6 +Keyboard Data
PC7 -Keyboard Cable Connected

8255 Bit Assignment Description

PA0 thru PA7	(Output Lines)	Port A is configured as an output. The output lines are not used by the hardware, but are used to store keystrokes. This is done to maintain compatibility with the Personal Computer, and Personal Computer XT.
PB0	(+Timer 2 Gate)	This line is routed to the gate input of timer 2 on the 8253-5. When this bit is 'low', the counter operation is halted. This bit and PB1 (+Speaker Data) controls the operation of the 8253-5 sound source.
PB1	(+Speaker Data)	This bit ANDS 'off' the output of the 8253-5 timer 2. It can be used to disable the 8253-5 sound source, or modify its output. When this bit is a 1, it enables the output, a 0 forces the output to zero.
PB2	(+Alpha -Graphics)	This bit is used to steer data from the memory into the Video Gate Array. This bit should be a 1 for all alpha modes, and a 0 for all graphics modes.

PB3	(+Cassette Motor Off)	When this bit is a 1, the cassette relay is 'open' and the cassette motor is 'off'. When this bit is a 0, and PB4 = 0, the cassette motor is 'on'.
PB4	(+Disable internal beeper and cassette motor relay)	When this bit is a 1, the internal beeper is 'disabled' and the 8253-5 timer 2 sound source can only be heard if it is steered to the audio output. This bit also disables the cassette motor when it is a 1. To 'enable' the cassette motor, this bit must be a 0. In this case, PB1 should be used to gate 'off' the internal beeper and 8253-5 sound source.
PB5, PB6	(Speaker switch 0,1)	These bits steer one of 4 sound sources. This is available to the RF modulator or the external audio jack. The sound sources selected are shown below.

PB6	**PB5**	**Sound Source**
0	0	8253-5 Timer 2
0	1	Cassette Audio Input
1	0	I/O Channel Audio In
1	1	76496

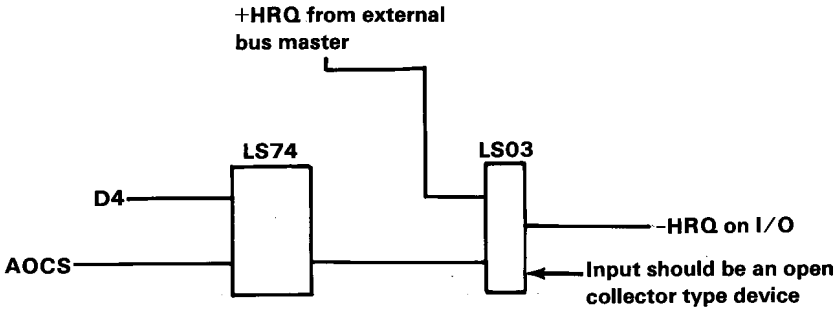
PB7	(Open)	Reserved for future use.

PC0	(Keyboard latched)	This input comes from a latch which is set to a 1 on the first rising edge of the Keyboard Data stream. The output of this latch also causes the NMI to occur. This latch is cleared by doing a dummy 'Read' operation to port A0. This input is provided so that a program can tell if a keystroke occurred during a time when the NMI was masked 'off' and a keystroke has been missed. The program will then be able to give an error indication of the missed keystroke.
PC1	(-Modem card installed)	When this bit is a 0, it indicates that the Internal Modem card is installed.
PC2	(-Diskette card installed)	When this bit is a zero, it indicates that the Diskette Drive Adapter is installed.
PC3	(-64KB Memory and Display Expansion installed)	When this bit is a 0, it indicates that the 64KB Memory and Display Expansion is installed.

PC4	(Cassette data in)	If the cassette-motor relay is 'closed', and the cassette motor is 'on', this pin will contain data which has been wave shaped from the cassette. If the cassette-motor relay is 'off', this pin will contain the same data as the 8253-5 timer 2 output.
PC5	(Timer channel 2 output)	This input is wired to the timer channel 2 output of the 8253-5.
PC6	(+Keyboard data)	This input contains keyboard data. The keyboard data comes from the cable if attached, or from the IR Receiver if the cable is not attached.
PC7	(-Keyboard cable connected)	If this bit is 'low', it indicates that the keyboard cable is connected.

Port A0 Output Description

D7	**(Enable NMI)**	When this bit is a 1, the NMI is 'enabled'. When it is a 0, it is 'disabled'.
D6	**(IR test ENA)**	This bit enables the 8253-5 timer 2 output into an IR diode on the IR Receiver board. This information is then wrapped back to the keyboard input. If the cable is not connected, timer 2 should be set for 40 kHz which is the IR-modulation frequency. This feature is used only for a diagnostic test of the IR Receiver board.
D5	**(Selc Clk1 input)**	This bit selects one of two input Clks to the 8253-5 timer 1. A 0 selects a 1.1925 MHz Clk input used to assist the program in de-serializing the keyboard data. A 1 selects the timer 0 output to be used as the Clk input to timer 1. This is used to catch timer 0 overflows during diskette drive operations when interrupts are masked 'off'. This is then used to update the time-of-day.
D4	**(+Disable HRQ)**	This bit is not actually implemented on the system board, but is supported by the programming. This bit is used to disable -HRQs from external bus-masters (DMA, Alternate Processors, etc.) The logic for this bit must exist on each bus-master attachment. A 0 should 'enable' -HRQ, and a 1 should 'disable' -HRQ.



Port A0 Output Description

Port A0 Input Operation

A 'read' to I/O port A0 will clear the keyboard NMI latch. This latch causes an NMI on the first rising edge of the keyboard data if the enable NMI bit (port A0 bit D7) is 'on'. This latch can also be read on the 8255 PC0. The program can determine if a keystroke occurred while the NMI was 'disabled' by reading the status of this latch. This latch must be cleared before another NMI can be received.

The System board provides for selection of keyboard data from either a cable or the IR-receiver board. The IR-receiver board is mounted on the system board and can receive data through an IR link. The source of the keyboard's data is determined by the -Cable Connected signal at the keyboard cable connector. Keyboard serial data is available to the 8088 at bit PC6 of the 8255 PPI.

The system board is responsible for the de-serialization of keyboard data. The start bit in the serial stream causes an NMI to be generated. The 8088 then reads the 8253 timer to determine when to interrogate the

serial stream. After de-serialization the NMI service-routine does a 'Read' from hex A0 to clear the NMI latch.

During certain time-critical operations, such as diskette I/O, the processor will mask 'off' the NMI interrupt. Keyboard inputs during this time cannot be serviced. A keyboard latch is provided so that at the end of such operations the processor will determine whether any keys were pressed and take appropriate actions. The keyboard latch is 'set' by any key being pressed and is 'reset' by 'Reading' the NMI port. (No data is presented to the microprocessor during this 'Read'.) Keyboard latch data is available to the processor at bit PC0 of the 8255 PPI.

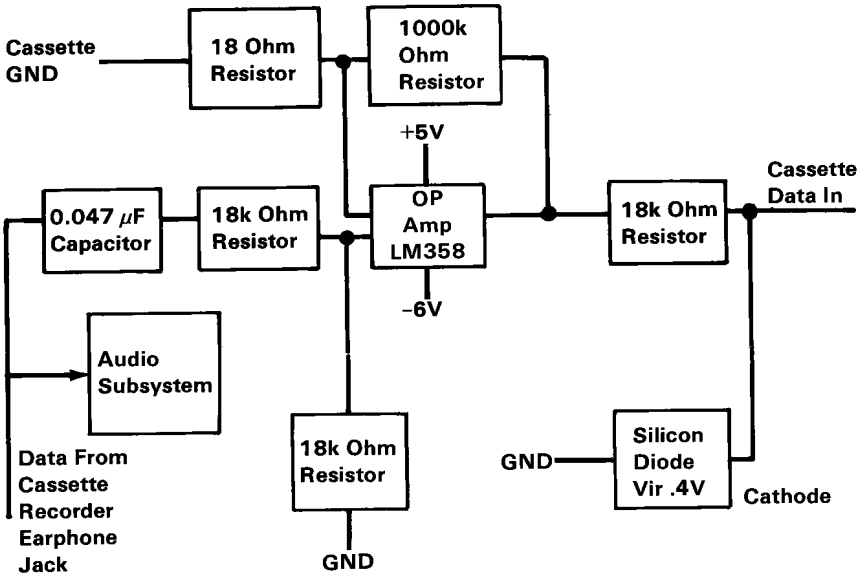
Notes:

Cassette Interface

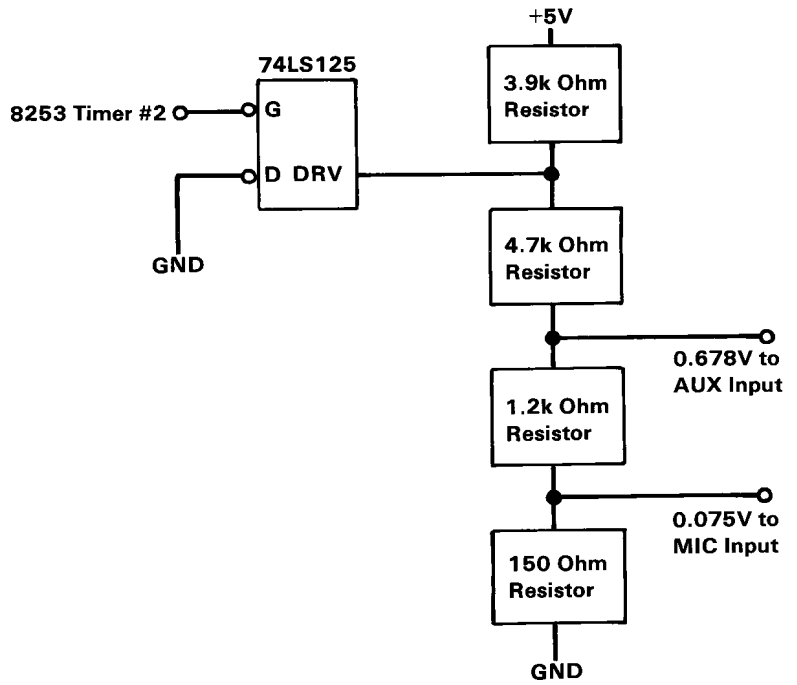
The cassette interface is controlled through software. An output from the 8253 timer controls the data to the cassette recorder through the cassette connector at the rear of the system board. The cassette-input data is read by an input-port bit of the 8255A-5 programmable-peripheral-interface (PPI) (8255A-5 PC4). Software algorithms are used to generate and read cassette-data. The cassette drive- motor is controlled by Bit PB3 of the 8255. Bit PB4, which 'enables' the 7547 relay driver, must be 'low' when the motor is to be turned on. The cassette interface has a wrap feature which connects the output to the input when the motor control is 'off'. See "BIOS Cassette Logic" in Section 5 for information on data storage and retrival.

A mechanism is provided that will direct the cassette input to the audio subsystem. Please see "Sound Subsection" in Section 2.

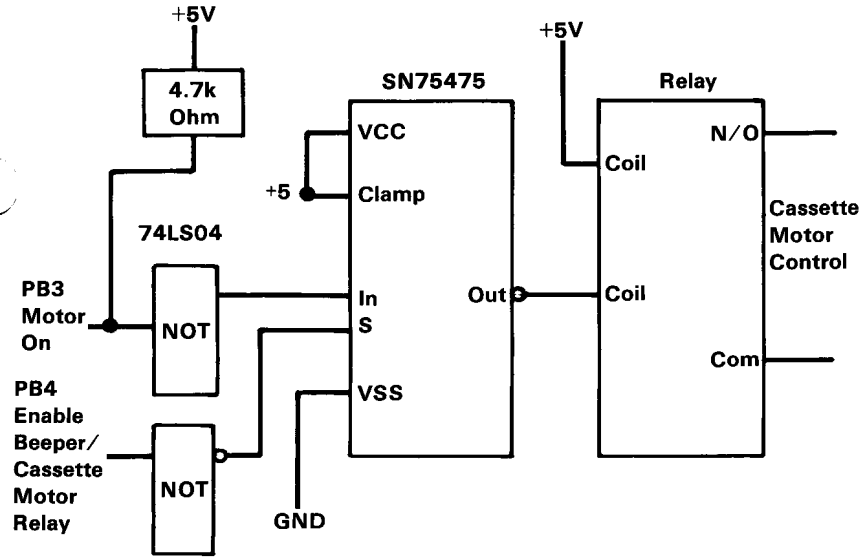
Circuit block diagrams for the cassette-interface read, write, and motor control are illustrated in the following figures.



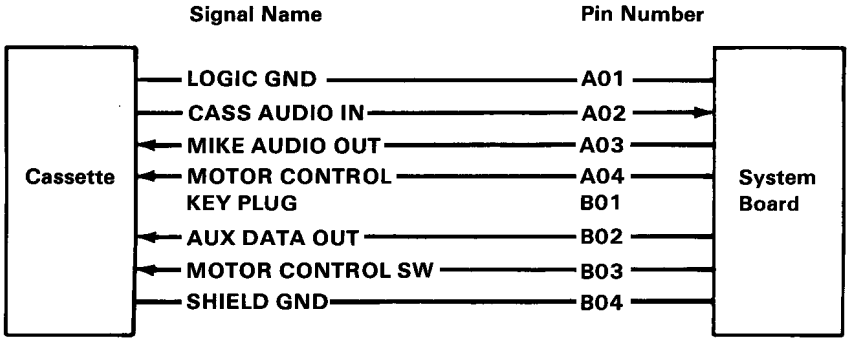
Cassette-Interface Read-Hardware Block Diagram



Cassette-Interface Write-Hardware Block Diagram



Cassette-Motor Control Block Diagram



Cassette Connector Specifications

Notes:

Video Color/Graphics Subsystem

The video subsystem is designed so that the IBM Color Display, composite monitors, and a home television set can be attached. It is capable of operating in black-and-white or color. It provides three video ports: a composite-video, a direct-drive, and a connector for an RF modulator to be used with home televisions. In addition, it contains a light pen interface.

Note: The IBM Personal Computer Monochrome Display cannot be used with the PC*jr* system.

Note: An IBM Connector for Television option must be obtained to attach a home TV.

The subsystem has two basic modes of operation: alphanumeric (A/N) and all points addressable graphics (APA). Additional modes are available within the A/N and APA modes.

In the A/N mode, the display can be operated in either a 40-column by 25-row mode for a low-resolution display home television, or an 80-column by 25-row mode for high-resolution monitors. In both modes, characters are defined in an 8-wide by 8-high character box and are 7-wide by 7-high, with one line of descender. Both A/N modes can operate in either color or black-and-white.

In the A/N black-and-white mode, the character attributes of reverse video, blinking, highlighting and gray shades are available.

In the A/N color mode, sixteen foreground-colors and sixteen background-colors are available for each character. In addition, blinking on a per-character basis

is available. When blinking is used, only eight background-colors are available. One of 16 colors, or gray shades can be selected for the screen's border in all A/N modes.

In both A/N modes, characters are formed from a ROM character-generator. The character generator contains dot patterns for 256 different characters. The character set contains the following major groupings of characters:

- 16 special characters for game support
- 15 characters for word-processing editing support
- 96 characters for the standard-ASCII-graphics set
- 48 characters for foreign-language support
- 48 characters for business block-graphics (allowing drawing of charts, boxes, and tables using single or double lines)
- 16 selected Greek symbols
- 15 selected scientific-notation characters

In the APA mode, there are three resolutions available: a low-resolution mode (160 PELs [Picture ELements] by 200 rows), a medium-resolution mode (320 PELs by 200 rows), and a high-resolution mode (640 PELs by 200 rows).

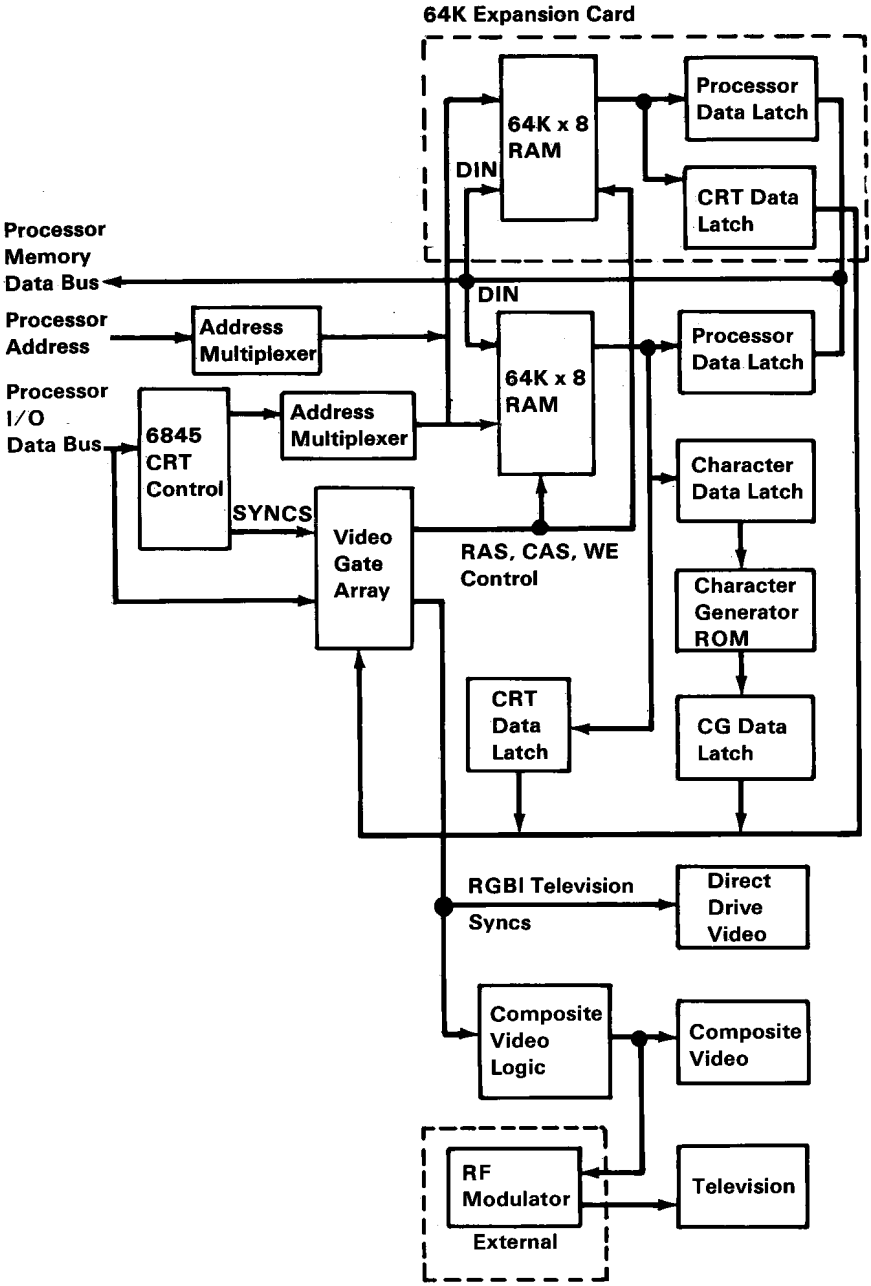
Different color modes exist within each of the APA resolutions. Two, four, or sixteen colors are available in APA color, and two, four, or sixteen gray shades are available in APA black-and-white.

One of sixteen colors, or grey shades can be selected for the screen's border in all APA modes.

The direct drive, composite video and RF Modulator connector are right-angle-mounted connectors extending through the rear of the system unit.

The video color/graphics subsystem is implemented using a Motorola 6845 CRT controller device and a Video Gate Array (VGA) (LSI5220). The video subsystem is highly programmable with respect to raster and character parameters. Thus many additional modes are possible with the proper programming.

The following figure shows a block diagram of the video color/graphics subsystem.



Video Color/Graphic Subsystem Block Diagram

Major Components Definitions

Motorola 6845 CRT Controller

This device provides the necessary interface to drive a raster-scan CRT. Additional information about this component is provided in publications listed in "Bibliography".

Storage Organization

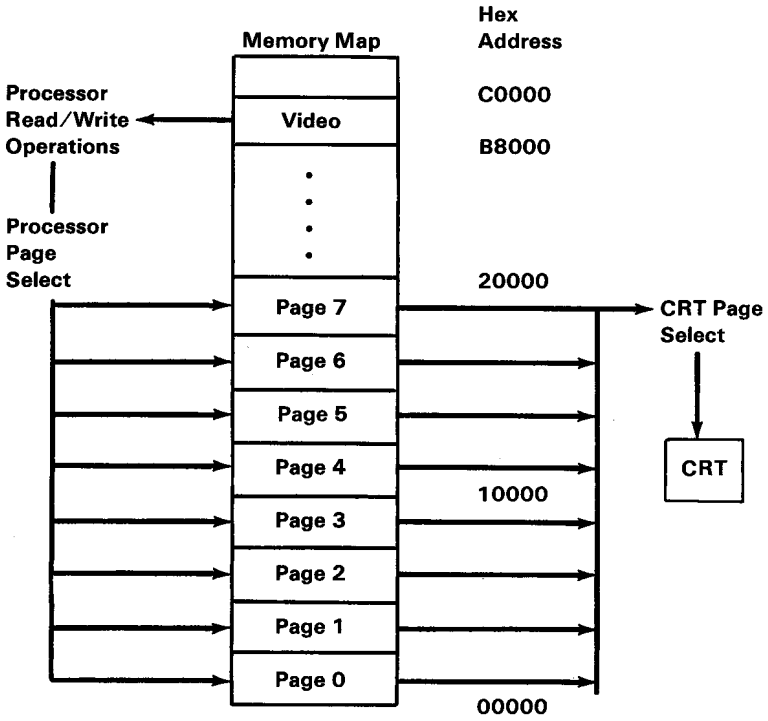
The base video-color/graphics-subsystem accesses 64K bytes of read/write memory (RAM). A 64KB Memory and Display Expansion can be added to increase the amount of system RAM to 128K bytes. This memory-storage area serves two functions; as the video-display buffer and as the system processor is (8088) main-RAM.

The RAM is located at address hex 0000 and is either 64K bytes or 128K bytes with the memory expansion option. The 8088 can access the memory by reading from and writing to address locations hex 00000 to 1FFFF or by reading from or writing to the 16K-byte region starting at address hex B8000. The page affected by a read or write operation is determined by the processor's page register. The processor can access the RAM at any time in all modes with no adverse effect to the video information. The page that the video information is taken from is determined by the CRT page register.

The processor and CRT page registers are write only registers and can be changed at any time. These registers allow the processor to work in one page while the display is displaying another page. The processor can switch pages at the vertical-retrace time. This will aid animation on the video color/graphics subsystem.

Also, since all 128K bytes of read/write memory are available for display purposes, the application can use as little or as much memory as needed for the display.

The following figure is a map of the video color/graphics subsystem.



Video Color/Graphics Subsystem Memory Map

Bandwidth

The video bandwidth is either 3.5, 7 or 14 MHz depending on the mode of operation. The processor bandwidth is the same for all modes. The processor is allowed one cycle every 1.1 microseconds. An average of two wait states will be inserted in a processor RAM read cycle, because the average latency time for the processor to get a cycle is 560 ns and the cycle time is 350 ns. There is no performance penalty for redirecting processor reads and writes through the B8000 - BFFFF address area.

Character Generator

The ROM character-generator consists of 2K bytes of storage which cannot be read from, or written to under software control. It is implemented with a MCM68A316E or equivalent. Its specifications are 350 ns access, 350 ns cycle static operation. The device is pin compatible with 2716 and 2732 EPROMS.

Video Gate Array

A CMOS gate array is used to generate storage-timing (RAS, CAS, WE), direct-drive, composite-color and status signals. See "Video Gate Array" later in this section.

Palette

The video color/graphics subsystem contains a 16-word by 4-bit palette in the Video Gate Array which takes PEL (Picture ELement) information from the read/write memory and uses it to select the color to display. This palette is used in all A/N and APA modes. Any input to the palette can be individually masked 'off' if a mode does not support the full complement of 16 colors. This masking allows the user to select a unique palette of colors whenever any mode does not support all 16 colors.

In two-color modes, the palette is defined by using one bit (PA0), with the following logic:

Palette Address Bit	
PA0	**Function**
0	Palette Register 0
1	Palette Register 1

Palette Logic (1 of 3)

In four-color modes, the palette is defined by using two bits (PA1 and PA0), with the following logic:

Palette Address Bits		Function
PA1	PA0	
0	0	Palette Register 0
0	1	Palette Register 1
1	0	Palette Register 2
1	1	Palette Register 3

Palette Logic (2 of 3)

In sixteen-color modes, the palette is defined by using four bits (PA3, PA2, PA1, and PA0), with the following logic:

Palette Address Bits				Function
PA3	PA2	PA1	PA0	
0	0	0	0	Palette Register 0
0	0	0	1	Palette Register 1
0	0	1	0	Palette Register 2
0	0	1	1	Palette Register 3
0	1	0	0	Palette Register 4
0	1	0	1	Palette Register 5
0	1	1	0	Palette Register 6
0	1	1	1	Palette Register 7
1	0	0	0	Palette Register 8
1	0	0	1	Palette Register 9
1	0	1	0	Palette Register 10
1	0	1	1	Palette Register 11
1	1	0	0	Palette Register 12
1	1	0	1	Palette Register 13
1	1	1	0	Palette Register 14
1	1	1	1	Palette Register 15

Palette Logic (3 of 3)

The sixteen colors available to all A/N and APA modes are selected through combinations of the I (Intensity), R (Red), G (Green), and B (Blue) bits. These colors are listed in the following figure:

I	R	G	B	Color
0	0	0	0	Black
0	0	0	1	Blue
0	0	1	0	Green
0	0	1	1	Cyan
0	1	0	0	Red
0	1	0	1	Magenta
0	1	1	0	Brown
0	1	1	1	Light Gray
1	0	0	0	Dark Gray
1	0	0	1	Light Blue
1	0	1	0	Light Green
1	0	1	1	Light Cyan
1	1	0	0	Pink
1	1	0	1	Light Magenta
1	1	1	0	Yellow
1	1	1	1	White

Note: The "I" bit provides extra luminance (brightness) to each available shade. This results in the light colors listed above, except for monitors that do not recognize the "I" bit.

Summary of Available Colors

Alphanumeric Modes

Every display-character position in the alphanumeric mode is defined by two bytes in the system read/write memory, using the following format:

Display Character Code Byte								Attribute Byte							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Display Format

The functions of the attribute byte are defined by the following figure:

Attribute Function	Attribute Byte Definition							
	7	6	5	4	3	2	1	0
	Fore-Ground Blink	PA2	PA1	PA0	PA3	PA2	PA1	PA0
		Background			Foreground			
Normal	B	0	0	0	I	1	1	1
Reverse Video	B	1	1	1	I	0	0	0
Nondisplay (Off)	B	0	0	0	I	0	0	0
Nondisplay (On)	B	1	1	1	I	1	1	1

I = Highlighted Foreground (Character)
B = Blinking Foreground (Character)

Attribute Functions

Graphics Mode

The Video Color/Graphics Subsystem can be programmed for a wide variety of modes within the graphics mode. Five graphics-modes are supported by the system's ROM BIOS. They are low-resolution 16-color graphics, medium-resolution 4-color graphics, medium-resolution 16-color graphics, high-resolution 2-color graphics, and high-resolution 4-color graphics. The table in the following figure summarizes the five modes:

Graphics Mode	Horiz. (PELs)	Vert. (Rows)	Number of Colors Available (Includes Background Color)
Low-Resolution 16-Color	160	200	16 (Includes b-and-w)
Medium-Resolution 4-Color	320	200	4 Colors of 16 Available
Medium-Resolution 16-Color	320	200	16 (Includes b-and-w)
High-Resolution 2-Color	640	200	2 Colors of 16 Available
High-Resolution 4-Color	640	200	4 Colors of 16 Available

Note: The screen's border color in all modes can be set to any 1 of the 16 possible colors. This border color is independent of the screen's work area colors. In Black and White each color maps to a distinct gray shade.

Graphics Modes

Low-Resolution 16-Color Graphics

The low-resolution mode supports home-television sets, low-resolution displays, and high-resolution displays. It has the following characteristics:

- Contains a maximum of 200 rows of 160 PELs
- Specifies 1 of 16 colors for each PEL by the I, R, G, and B bits
- Requires 16K bytes of read/write memory
- Formats 2 PELs per byte for each byte in the following manner:

7	6	5	4	3	2	1	0
PA3	PA2	PA1	PA0	PA3	PA2	PA1	PA0
First Display PEL				Second Display PEL			

Low-Resolution 16-Color Graphics

Medium-Resolution 4-Color Graphics

The medium-resolution mode supports home-television sets, low-resolution displays, and high-resolution displays. It has the following characteristics:

- Contains a maximum of 200 rows of 320 PELs
- Selects one of four colors for each PEL
- Requires 16K bytes of read/write memory
- Supports 4 of 16 possible colors
- Formats 4 PELs per byte for each byte in the following manner:

7	6	5	4	3	2	1	0
PA1	PA0	PA1	PA0	PA1	PA0	PA1	PA0
First Display PEL		Second Display PEL		Third Display PEL		Fourth Display PEL	

Medium-Resolution 4-Color Graphics

Medium-Resolution 16-Color Graphics

The medium-resolution 16-color graphics mode supports home television sets, low-resolution displays, and high-resolution displays. It has the following characteristics:

- Requires system configuration of 128K bytes of read/write memory
- Requires 32K bytes of read/write memory
- Contains a maximum of 200 rows of 320 PELs.
- Specifies 1 of 16 colors for each PEL
- Formats 2 PELs per byte for each byte in the following manner.

7	6	5	4	3	2	1	0
PA3	PA2	PA1	PA0	PA3	PA2	PA1	PA0
First Display PEL				Second Display PEL			

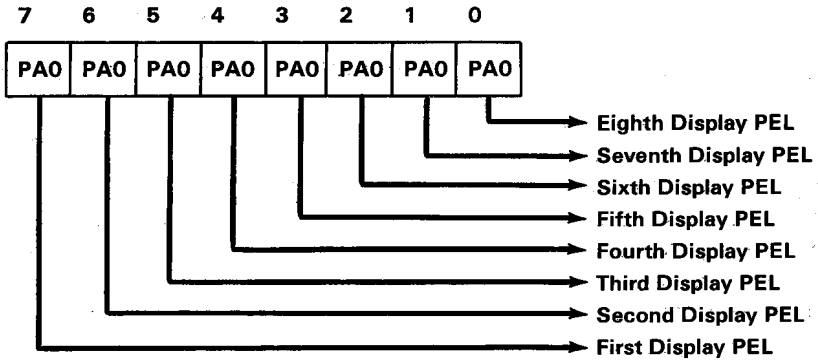
Medium-Resolution 16-Color Graphics

High-Resolution 2-Color Graphics

The high-resolution 2-color mode supports high-resolution monitors only. This mode has the following characteristics:

- Contains a maximum of 200 rows of 640 PELs
- Supports 2 of 16 possible colors.

- Requires 16K bytes of read/write memory.
- Formats 8 PELs per byte for each byte in the following manner:

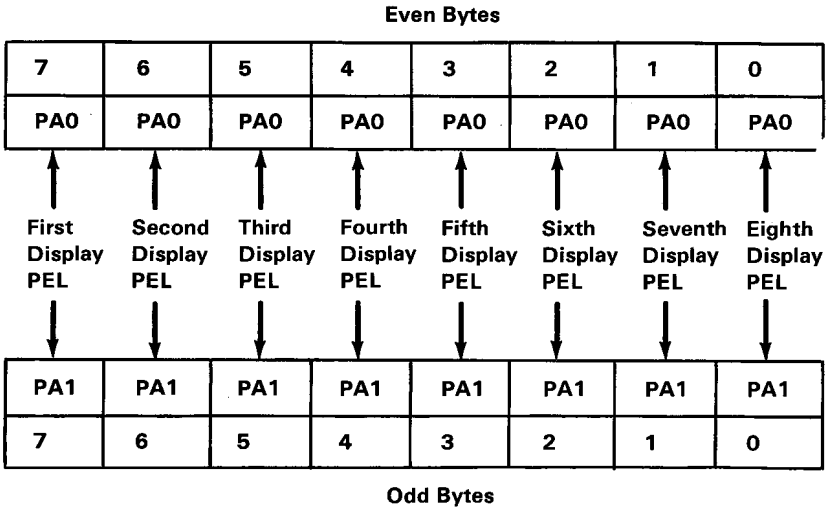


High-Resolution 2-Color Graphics

High-Resolution 4-Color Graphics

The high-resolution mode is used only with high-resolution monitors. This mode has the following characteristics:

- Requires system configuration of 128K Bytes read/write memory
- Requires 32K bytes of read/write memory
- Contains a maximum of 200 rows of 640 PELs
- Selects one of four colors for each PEL
- Supports 4 out of 16 colors
- Formats 8 PELs per two bytes (consisting of one even-byte and one odd-byte) in the following manner:

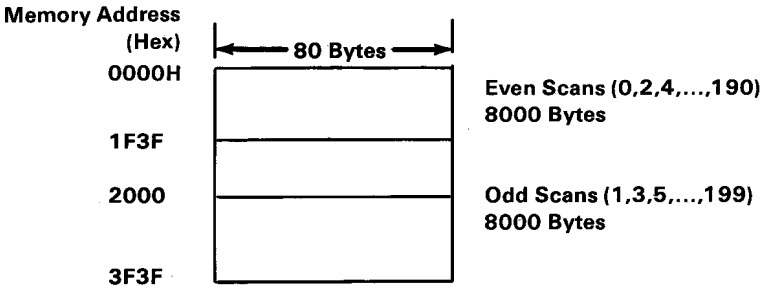


High-Resolution 4-Color Graphics

Graphics Storage Organization

For the low-resolution 16-color graphics, the medium-resolution 4-color graphics, and the high-resolution 2-color graphics, storage is organized into two banks of 8000 bytes each.

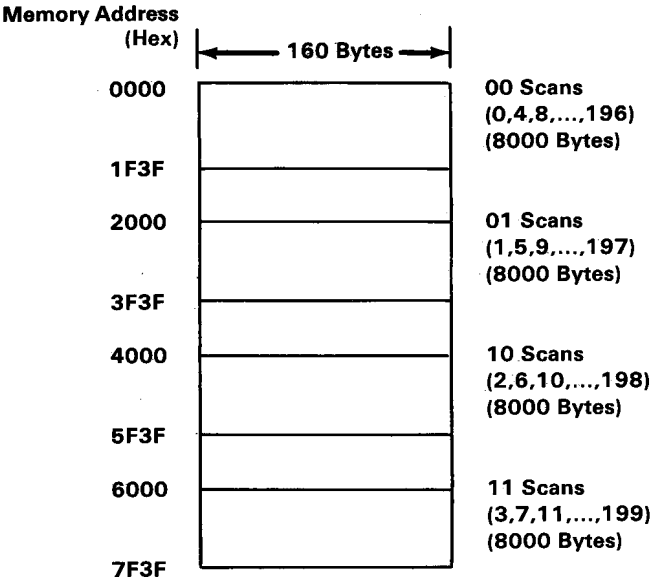
The following figure shows the organization of the graphics storage.



Graphics Storage Organization (Part 1 of 2)

Address 0000 contains PEL information for the upper-left corner of the display area.

For the medium-resolution 16-color graphics, and the high-resolution 4-color graphics modes, the graphics storage is organized into four banks of 8000 bytes each.



Graphics Storage Organization (Part 2 of 2)

Address 0000 contains PEL information for the upper-left corner of the display.

Video Gate Array

The Video Gate Array is located at I/O address hex 3DA, and is programmed by first writing a register address to port hex 3DA and then writing the data to port hex 3DA.

Any I/O 'write'-operations to hex address 3DA continuously toggle an internal address/data flip-flop. This internal flip-flop can be set to the address state by issuing an I/O 'read' instruction to port hex 3DA. An I/O 'read' instruction also 'reads' the status of the Video Gate Array. A description of each of the registers in the Video Gate Array follows.

Hex Address	Register
00	Mode Control 1
01	Palette Mask
02	Border Color
03	Mode Control 2
04	Reset
10-1F	Palette Registers

Video Gate Array Register Addresses

Mode Control 1 Register

This is a 5-bit 'write'-only register, it cannot be 'read'. Its address is 0 within the Video Gate Array. A description of this register's bit functions follows.

Bit 0	+HIBW/-LOBW
Bit 1	+Graphics/-Alpha
Bit 2	+B/W
Bit 3	+Video Enable
Bit 4	+16 Color Graphics

Mode Control 1 Register

Bit 0 This bit is 'high' (1) for all high-bandwidth modes. These modes are all modes which require the 64KB Memory and Display Expansion for a system total of 128K bytes of read/write memory. The high bandwidth modes are the 80 by 25 alphanumeric mode, the 640 by 200 4-color graphics mode, and the 320 by 200 16-color graphics mode. This bit is 'low' (0) for all low-bandwidth modes.

Bit 1 This bit is 'high' (1) for all graphics modes and is 'low' (0) for all alphanumeric modes.

Bit 2 When this bit is 'high' (1), the composite-video color-burst and chrominance are disabled, leaving only the composite intensity-levels for gray shades. When this bit is 'low' (0), the composite-video color is 'enabled'. This

bit should be set 'high' for high-resolution black-and-white display applications.

Note: This bit has no effect on direct-drive colors.

Bit 3 When this bit is 'high' (1), the video signal is 'enabled'. The video signal should be 'disabled' when changing modes. When the video signal is 'disabled', the screen is forced to the border color.

Bit 4 This bit must be 'high' (1) for all 16-color graphics-modes. These modes are the 160 by 200 16-color graphics-mode and the 320 by 200 16-color graphics-mode.

Palette Mask Register

This is a 4-bit write-only register, it cannot be 'read'. Its address in the Video Gate Array is hex 01. A description of this register's bit functions follows.

Bit 0	-Palette Mask 0
Bit 1	-Palette Mask 1
Bit 2	-Palette Mask 2
Bit 3	-Palette Mask 3

Palette Mask Register

When bits 0-3 are 0, they force the appropriate palette address to be 0 regardless of the incoming color

information. This can be used to make some information in memory a 'don't care' condition until it is requested.

In the 2-color and 4-color modes, the palette addresses should be 'masked' because only 1 or 2 color-lines contain valid information. For 4-color modes, the palette mask register should contain a hex 03 and, for 2-color modes, it should contain a hex 01.

Border Color Register

This is a 4-bit 'write'-only register, it cannot be 'read'. Its address in the Video Gate Array is hex 02. The following is a description of the register's bit functions:

Bit Number	Function
0	+ B (Blue) Border Color Select
1	+ G (Green) Border Color Select
2	+ R (Red) Border Color Select
3	+ I (Intensity) Border Color Select

Border Color Register

A combination of bits 0-3 selects the screen-border color as one of 16 colors, as listed in the "Summary of Available Colors" table in this section.

Mode Control 2 Register

This is a 4-bit, 'write'-only register, it cannot be 'read'. Its address inside the Video Gate Array is hex

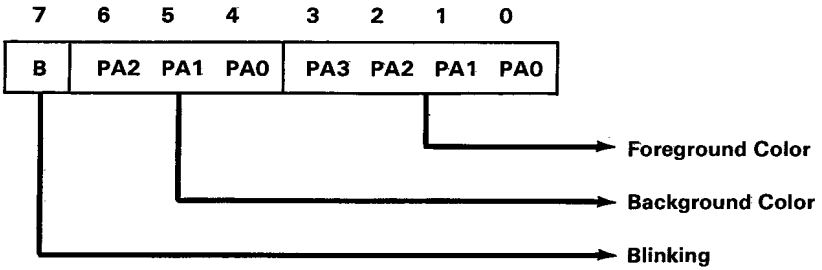
03. The following is a description of the register's bit functions:

Bit Number	Function
0	– Reserved = 0
1	+ Enable Blink
2	– Reserved = 0
3	+ 2-Color Graphics

Mode Control 2 Register

Bit 0 This bit is reserved, but should always be programmed as a 0.

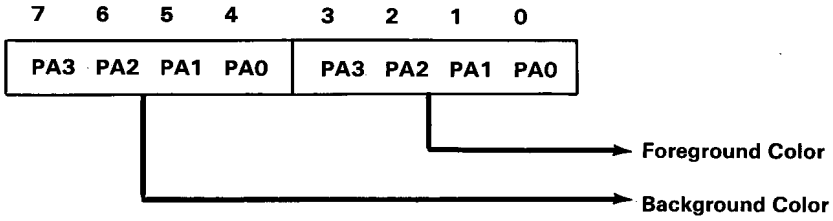
Bit 1 When this bit is 'high' (1) in the alphanumeric mode, the attribute byte has the following definition:



Where PA0 to PA3 are palette addresses.

Attribute Byte Definition (Part 1 of 2)

If the enable-blink bit is 'off' in the alphanumeric mode, the attribute byte takes on the following definition:



Attribute Byte Definition (Part 2 of 2)

If the enable-blink bit is on in a graphics mode, the high-order address of the palette (PA3) is replaced with the character-blink rate. This causes displayed colors to switch between two sets of colors.

If the colors in the lower half of the palette are the same as in the upper half of the palette, no color changes will occur. If the colors in the upper half of the palette are different from the lower half of the palette, the colors will alternately change between the 2 palette colors at the blink rate.

Only eight colors are available in the 16-color modes when using this feature. Bit 3 of the palette mask has no effect on this mode.

Bit 2 This bit is reserved, but should always be programmed as a 0.

Bit 3 This bit should be 'high' (1) when in the 640 by 200 2-color graphics-mode. It should be 'low' (0) for all other modes.

Reset Register

This is a 2-bit 'write'-only register, it cannot be 'read'. Its address inside the Video Gate Array is hex 04. The following is a description of the register's bit functions:

Bit 0	+Asynchronous Reset
Bit 1	+Synchronous Reset

Reset Register

Bit 0 When 'high' (1), this bit will issue an 'asynchronous reset' to the Video Gate Array. This will cause all memory cycles to stop and all output signals to be tri-stated. The 'asynchronous reset' should only be issued once at the system power-on time. This bit should be 'high' (1), the Video Gate Array and the 6845 programmed, and then it should be 'low' (0).

The system read/write memory (RAM) will not work until this power-on sequence is finished. After this power-on sequence, subsequent 'resets' should be 'synchronous resets'.

Note: Issuing an 'asynchronous reset' can cause the contents of RAM to be destroyed.

Bit 1 When 'high' (1), this bit will issue a 'synchronous reset' to the Video Gate Array. This will cause all memory cycles to stop and all output signals to stop. Bit 1 should be 'low' (0) before changing modes.

Before issuing a 'synchronous reset', the program should read 256 locations in RAM as every other location in 512 locations. The program should then issue the 'synchronous reset' and change the mode. This changes the Video Gate Array mode-control registers and the 6845 registers.

Next, the 'synchronous reset' should be removed and the 256 RAM locations should be 'read' again as above. This procedure will ensure system RAM data-integrity during mode changes. 'Synchronous resets' need only be issued when changing between high-bandwidth, and low- bandwidth modes. (Bit 0 in mode control 1 register)

Note: No accesses to RAM can be made while the video gate array is in a 'reset' state. 'Resets' must be done from code in ROM or EPROM's.

Palette Registers

There are sixteen 4-bit-wide palette-registers. These registers are 'write'-only, they cannot be 'read'. Their addresses in the Video Gate Array are from hex 10 to 1F.

Palette address hex 10 is accessed whenever the color code from memory is a hex 0, address hex 11 is accessed whenever the color code from memory is a hex 1, and so forth. A description of the color codes is in "Summary of Available Colors" in this section.

Note: The palette address can be 'masked' by using the palette mask register.

The following is a description of the register's bit functions:

Bit Number	Function
0	+ Blue
1	+ Green
2	+ Red
3	+ Intensity

Palette Register Format

When loading the palette, the video is 'disabled' and the color viewed on the screen is the data contained in the register being addressed by the processor.

When the program has completed loading the palette, it must change the hex address to some address less than hex 10 for video to be 'enabled' again.

If a programmer does not wish a user to see the adverse effects of loading the palette, the palette should be loaded during the vertical-retrace time. The program must modify the palette and change the video gate array address to less than hex 10 within the vertical-retrace time. A vertical-retrace interrupt and a status bit are provided to facilitate this procedure.

Status Register

This is a 5-bit 'read'-only register, it cannot be 'written'. The internal address of the video gate array is a 'don't care' condition for the status-register read-operation. A description of the register's bit functions follows:

Bit 0	+Display Enable
Bit 1	+Light Pen Trigger Set
Bit 2	-Light Pen Switch Made
Bit 3	+Vertical Retrace
Bit 4	+Video Dots

Status Register

Bit 0 When 'high' (1), this bit indicates video is being displayed.

Bit 1 When 'high' (1), this bit indicates that a positive- going edge from the light pen input has set the light pen trigger. This trigger is 'low' (0) upon a system power-on, and may also be cleared by performing an I/O 'Out' command to address hex 3DB. No specific data is required, this action is address-activated.

Bit 2 This bit indicates the status of the light pen switch. The switch is not latched or debounced. When this bit is 'low' (0), the light pen switch is 'on'.

Bit 3 When 'high' (1), this bit indicates the vertical retrace is 'active'.

Bit 4 When 'high' (1), this bit indicates that video-dot information is available. The two low-order bits of the address register determine the video-dot information presented through the following logic:

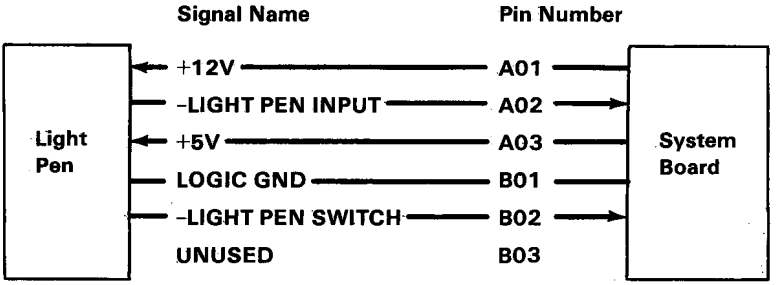
Address Register Bit 1	Address Register Bit 0	Video Dot Information Selected
0	0	Blue
0	1	Green
1	0	Red
1	1	Intensity

Address Register

This bit is provided for testing purposes. It verifies that video is occurring properly, and that the palette registers and all other 'write'-only registers are operating correctly.

Light Pen

A light pen can be used on the PC*jr* by connecting it to the six-pin connector for light pens on the back of the system board.



Connector Specifications

Note: The light pen interface is set for RGBI (Red, Green, Blue, Intensity). Due to timing differences between different displays (Different phosphors take longer to turn on, and different circuits take longer to accomplish their task.) the row, column value returned from the CRT can vary. This difference must be compensated for through software.

Programming Considerations

Programming the 6845 CRT Controller

The 6845 has 19 accessible, internal registers, which are used to define and control a raster-scanned CRT display. One of these registers, the Index Register, is actually used as a pointer to the other 18 registers. It is a 'write'-only register, which is loaded from the processor by executing an 'Out' instruction to I/O address hex 3D4. The five least-significant-bits of the I/O bus are loaded into the Index Register.

In order to load any of the other 18 registers, the Index Register is first loaded with the necessary pointer; then the Data Register is loaded with the information to be

placed in the selected register. The Data Register is loaded from the processor by executing an 'Out' instruction to I/O address hex 3D5.

The following table defines the values that must be loaded into the 6845-CRT-Controller registers to control the different modes of operation supported by the attachment:

Hex Addr.	Register #	Register Type	Units	I/O	Alphanumeric 40x25	Alphanumeric 80x25	Low/High Band Width Graphics
0	R0	Horizontal Total	Char.	Write Only	38	71	38/71
1	R1	Horizontal Display	Char.	Write Only	28	50	28/50
2	R2	Horizontal Sync Position	Char.	Write Only	2C	5A	2B/56
3	R3	Horizontal Sync Width	Char.	Write Only	06	0C	06/0C
4	R4	Vertical Total	Char. Row	Write Only	1F	1F	7F/3F
5	R5	Vertical Total Adjustment	Scan Line	Write Only	06	06	06/06
Note: All register values are given in hexadecimal.							

6845 Register Table (Part 1 of 3)

Hex Addr.	Register #	Register Type	Units	I/O	Alphanumeric 40x25	Alphanumeric 80x25	Low/High Band Width Graphics
6	R6	Vertical Displayed	Char. Row	Write Only	19	19	64/32
7	R7	Vertical Sync Position	Char. Row	Write Only	1C	1C	70/38
8	R8	Interlace Mode	—	Write Only	02	02	02/02
9	R9	Maximum Scan Line Address	Scan Line	Write Only	07	07	01/03
A	R10	Cursor Start	Scan Line	Write Only	06	06	26/26
B	R11	Cursor End	Scan Line	Write Only	07	07	07/07

Note: All register values are given in hexademical.

6845 Register Table (Part 2 of 3)

Hex Addr.	Register #	Register Type	Units	I/O	Alphanumeric 40x25	Alphanumeric 80x25	Low/High Band Width Graphics
C	R12	Start Addr. (H)	—	Write Only	00	00	00/00
D	R13	Start Addr. (L)	—	Write Only	00	00	00/00
E	R14	Cursor Addr. (H)	—	Read/ Write	00	00	00/00
F	R15	Cursor Addr. (L)	—	Read/ Write	00	00	00/00
10	R16	Light Pen (H)	—	Read Only	NA	NA	NA/NA
11	R17	Light Pen (L)	—	Read Only	NA	NA	NA/NA
Note: All register values are given in hexadecimal.							

6845 Register Table (Part 3 of 3)

CRT/Processor Page Register

This register is an 8-bit 'write'-only register, that cannot be read. Its address is hex 3DF. The following is a description of the Register functions.

Bit Number	Description
0	CRT Page 0
1	CRT Page 1
2	CRT Page 2
3	Processor Page 1
4	Processor Page 2
5	Processor Page 3
6	Video Address Mode 0
7	Video Address Mode 1

CRT/Processor Page Register (Part 1 of 2)

CRT Page 0-2 These bits select which 16K byte memory-page between 00000 to hex 1FFFF is being displayed. If there is no expansion RAM in the system, the high- order bit is a 'don't care', and only 4 pages are supported. For graphics modes which require 32K bytes the low-order bit is a 'don't care'.

Processor Page 0-2 These bits select the 16K byte memory-page region where memory cycles to B8000 are redirected. If there is no expansion RAM installed in the system, the high-order bit is a 'don't care' and only 4 pages are supported.

Video Adr Mode 0-1 These bits control whether the row scan addresses are used as part of the memory address. These should be programmed as follows:

Video Address Mode		Resulting Modes
1 (Bit 7)	0 (Bit 6)	
0	0	All Alpha Modes
0	1	Low-Resolution-Graphics Modes
1	1	High-Resolution-Graphics Modes
1	0	Unused, Reserved

CRT/Processor Page Register (Part 2 of 2)

The following I/O devices are defined on the video color/graphics subsystem:

Hex Address	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Function of Register
3DA	1	1	1	1	0	1	1	0	1	0	Gate Array Address and Status Register
3DB	1	1	1	1	0	1	1	0	1	1	Clear Light Pen Latch
3DC	1	1	1	1	0	1	1	1	0	0	Preset Light Pen Latch
3D0,3D4	1	1	1	1	0	1	0	x	x	0	6845 Index Register
3D1,3D5	1	1	1	1	0	1	0	x	x	1	6845 Data Register
3DF	1	1	1	1	0	1	1	1	1	1	CRT, Processor Page Register
x = "don't care" condition											

Video I/O Devices

Mode Selection Summary

Four registers of the Video Gate Array allow the user to access all the alphanumeric and graphics modes supported by the system ROM BIOS. The following table summarizes the modes and their register settings:

Mode	Video Gate Array Reg.			
	00	01	02	03
40 by 25 Alphanumeric Black-and-White	0C	0F	00	02
40 by 25 Alphanumeric Color	08	0F	00	02
80 by 25 Alphanumeric Black-and-White	0D	0F	00	02
80 by 25 Alphanumeric Color	09	0F	00	02
160 by 200 16-Color Graphics	1A	0F	00	00
320 by 200 4-Color Graphics	0A	03	00	00
320 by 200 4-Shade Black-and-White	0E	03	00	00
320 by 200 16-Color Graphics	1B	0F	00	00
640 by 200 2-Color Graphics	0E	01	00	08
640 by 200 4-Color Graphics	0B	03	00	00

Note: All values are given in hexadecimal.

Mode Summary

Sequence of Events for Changing Modes

1. Determine the mode of operation.
2. Reset the 'video enable' bit in the Video Gate Array to disable video.
3. Program the 6845 CRT Controller to select the mode.
   Read 256 bytes of memory
   Reset gate array
4. Program the Video Gate Array registers.

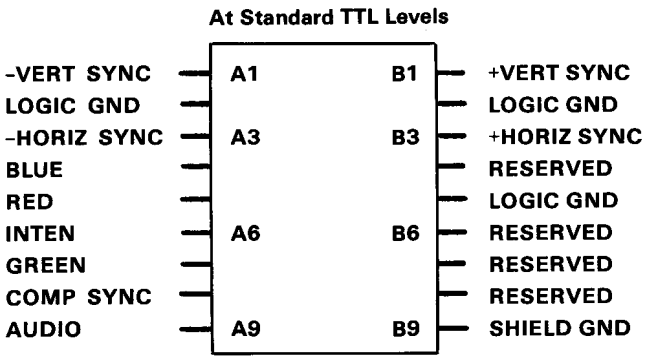
Remove gate-array reset
Read 256 bytes of memory

5. Re-enable video.

Note: The gate array needs to be reset only when changing the high-bandwidth/low-bandwidth register.

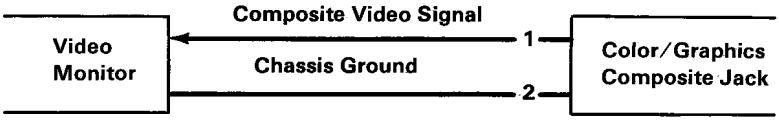
Interrupt Information

The Video Gate Array uses interrupt level 5 of the Intel 8259 to provide the vertical retrace interrupt to the system.



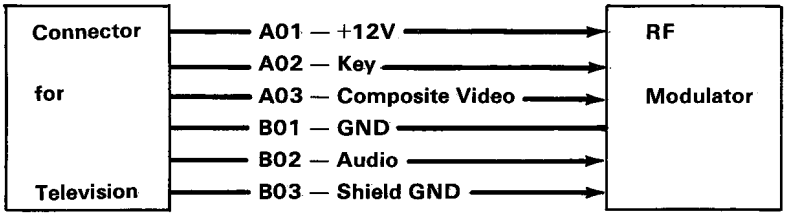
Connector Specifications

The direct-drive signals are standard TTL levels except the audio output which is a 1V peak-to-peak signal biased at 0V which can drive a 10K ohm or greater input-impedence.



Connector Specifications

The composite-video signal is 1V peak to peak biased at .7V with a 75 ohm load.



Television Connector Specifications

The Connector for Television connector has the composite-video signal at 1V peak to peak biased at .7V with a 75 ohm load. The connector also has the audio output which is 1V peak-to-peak signal biased at 0V which can drive a 10K ohm or greater input impedence.

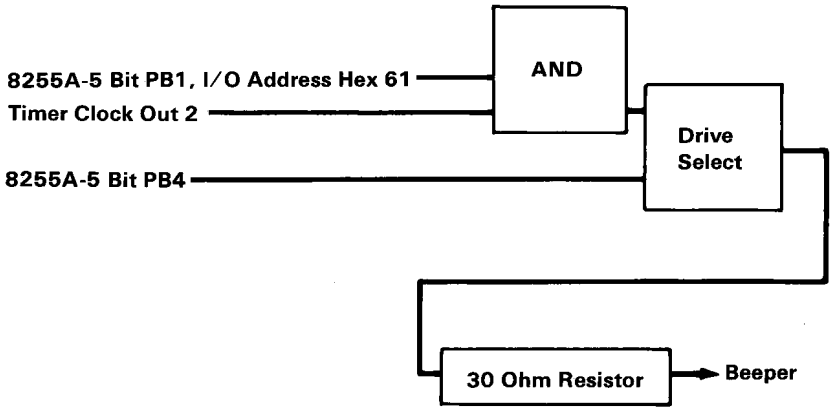
Notes:

Beeper

The system beeper is a small, piezoelectric- speaker, which can be driven from one or both of two sources. The two sources are:

- The 8255A-5 PPI output-bit PB1
- A timer clock out of an 8253-5 timer which has a 1.19 MHz-clock input. The timer gate is also controlled by an 8255-5 outport bit PB0.

  Note: The TI76496 Sound Generator cannot be directed through the beeper.

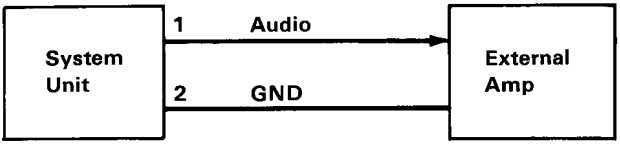


Beeper Block Diagram

Notes:

Sound Subsystem

The nucleus of the sound subsystem is an analog multiplexer (mpx) which allows 1 of 4 different sound sources to be selected, amplified, and sent to the audio outputs. The mpx and amplifier are configured so the amplifier's gain is unique to and consistent with each sound source. This provides a consistent level of output with any of the sound sources. The output of the amplifier is supplied to the IBM Connector for Television interface and external-amplifier interface. If an external speaker is used, an external amplifier must be used to drive it. The amplifier is configured as a single-pole low pass filter with a 3 dB cut-off frequency of 4.8 kHz. This filter is used to "round" off the corners of the square-wave signals. BIOS Power-on will initialize the sound subsystem to use the 8253 programmable-timer mode.



Connector Specifications

The audio output is a 1V peak-to-peak signal biased at 0V. It can drive a 10k ohm or greater input-impedence.

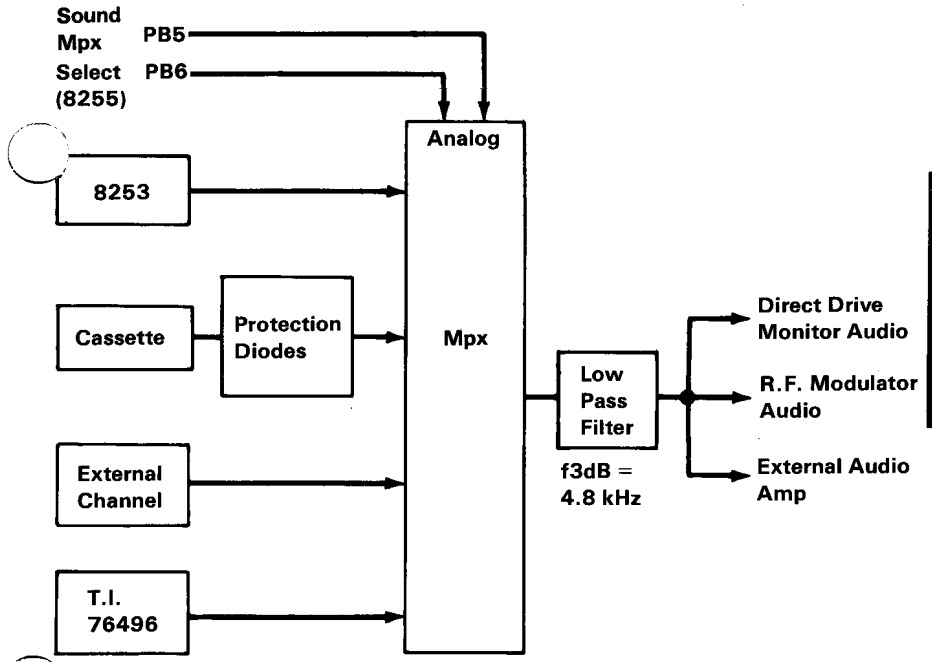
Source	Port Bits	
	PB6	PB5
Complex Sound Generator (TI 76496)	1	1
Programmable Timer (8253)	0	0
Cassette Audio	0	1
I/O Channel Audio	1	0
Port bits PB5 and PB6, of the 8255, control which source is selected.		

Sound Sources

Complex Sound Generator

The Complex Sound Generator chip (SN76496N) has 3 programmable frequencies which may be mixed to form chords and a white noise generator which may also be mixed for special effects. Each of the 3 channels as well as the white noise generator can be independently attenuated. The processor controls the sound chip by writing to port hex C0.

The Sound Generator is described in greater detail later in this section. More information can be obtained by referring to Texas Instruments' data sheets and application notes.



Sound Block Diagram

Audio Tone Generator

Features

- 3 Programmable Tone-Generators
- Programmable White Noise
- Programmable Attenuation
- Simultaneous Sounds
- TTL Compatible
- 3.579 MHz Clock Input
- Audio Mixer

Processor to Sound-Generator Interface

The system microprocessor communicates with the SN76496N through the 8 data lines and 3 control lines

(WE, CE and READY). Each tone generator requires 10 bits of information to select the frequency and 4 bits of information to select the attenuation. A frequency update requires a double-byte transfer, while an attenuator update requires a single-byte transfer.

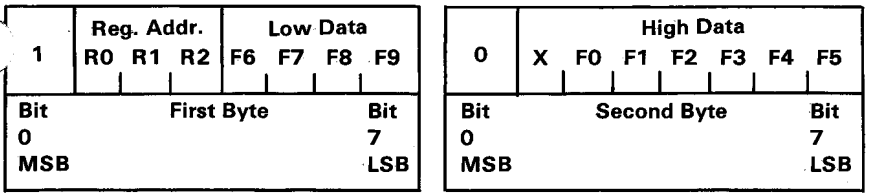
If no other control registers on the chip are accessed, a tone generator may be rapidly updated by initially sending both types of frequency and register data, followed by just the second byte of data for succeeding values. The register address is latched on the chip, so the data will continue going into the same register. This allows the 6 most-significant bits to be quickly modified for frequency sweeps.

Control Registers

The sound generator has 8 internal registers which are used to control the 3 tone generators and the noise source. During all data transfers to the sound generator, the first byte contains a 3-bit field which determines the destination control register. The register address codes are as follows:

Register Address Field			Destination Control Register
MSB R0	R1	LSB R2	
0	0	0	Tone 1 Frequency
0	0	1	Tone 1 Attenuation
0	1	0	Tone 2 Frequency
0	1	1	Tone 2 Attenuation
1	0	0	Tone 3 Frequency
1	0	1	Tone 3 Attenuation
1	1	0	Noise Control
1	1	1	Noise Attenuation

Register Address Field



Frequency (Double or Single Byte Transfer)

Frequency Generation

Each tone generator consists of a frequency-synthesis section and an attenuation section. The frequency-synthesis section requires 10 bits of information (hex F0-F9) to define half the period of the desired frequency (n). Hex F0 is the most-significant bit and hex F9 is the least-significant bit. This information is

loaded into a 10-stage tone-counter, which is decremented at an N/16 rate where N is the input-clock frequency. When the tone counter decrements to 0, a borrow signal is produced. This borrow signal toggles the frequency flip-flop and also reloads the tone counter. Thus, the period of the desired frequency is twice the value of the period register.

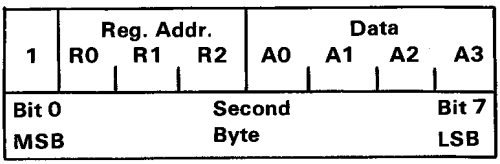
The frequency can be calculated by the following:

$$f = \frac{N}{32n}$$

where N = ref clock in Hz (3.579 MHz)

n = 10-bit binary-number

Attenuator



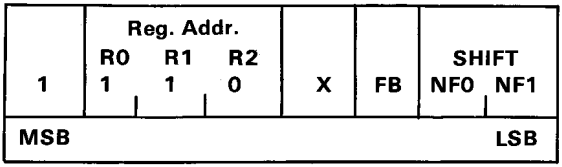
Update Attenuation (Single Byte Transfer)

The output of the frequency flip-flop feeds into a four-stage attenuator. The attenuator values, along with their bit position in the data word, are shown in the following figure. Multiple-attenuation control-bits may be 'true' simultaneously. Thus, the maximum theoretical attenuation is 28 dB typically.

Bit Position				
MSB A0	A1	A2	LSB A3	Weight
0	0	0	1	2dB
0	0	1	0	4dB
0	1	0	0	8dB
1	0	0	0	16db
1	1	1	1	OFF

Attenuator Values

Noise Generator



Update Noise Source (Single Byte Transfer)

The noise generator consists of a noise source and an attenuator. The noise source is a shift register with an exclusive-OR feedback-network. The feedback network has provisions to protect the shift register from being locked in the zero state.

FB	Configuration
0	Periodic Noise
1	White Noise

Noise Feedback Control

Whenever the noise-control register is changed, the shift register is cleared. The shift register will shift at one of four rates as determined by the two NF bits. The fixed shift-rates are derived from the input clock.

Bits		
NF0	NF1	Shift Rate
0	0	N/512
0	1	N/1024
1	0	N/2048
1	1	Tone Generator #3 Output

Noise Generator Frequency Control

The output of the noise source is connected to a programmable attenuator.

Audio Mixer/Output Buffer

The mixer is a conventional operational-amplifier summing-circuit. It will sum the three tone-generator

outputs, and the noise-generator output. The output buffer will generate up to 10 mA.

Data Transfer

The sound generator requires approximately 32 clock cycles to load the data into the register. The open collector READY output is used to synchronize the microprocessor to this transfer and is pulled to the false state (low voltage) immediately following the leading edge of CE. It is released to go to the true state (external pull-up) when the data transfer is completed.

This will insert approximately 42 wait states (8.9 μs) for each data transfer.

Warning: Do not attempt to issue an I/O read operation to the TI76496 port (COH). Such an operation will cause the system to hang indefinitely.

Note: If DMA is added to the system on the I/O channel, I/O WRITES to the 76496 will increase the latency time.

Notes:

Infra-Red Link

The infra-red link provides cordless communications between the keyboard and the system unit. Two infra-red-emitting diodes, mounted in the keyboard, transmit coded information to the system unit. The keyboard transmitter is fully discussed in "Cordless Keyboard" in this section. The infra-red receiver, which is located in the system unit, has an infra-red-sensitive device that demodulates the signal transmitted from the keyboard and sends it to the system.

Infra-Red Receiver

The receiver card measures 57.15 mm wide by 63 mm (2.25 in. by 2.50 in.) long. The infra-red receiver is mounted on the system board, component-side down, with two snap-in-type standoffs. Signal output and power input is through an 8-pin connector, located at the rear of the infra-red receiver. The infra-red-sensitive device is located on the front of the board and receives its input through an opening in the front of the system unit's cover. There is also an infra-red transmitter mounted on the receiver board for diagnostic purposes.

Functional Description

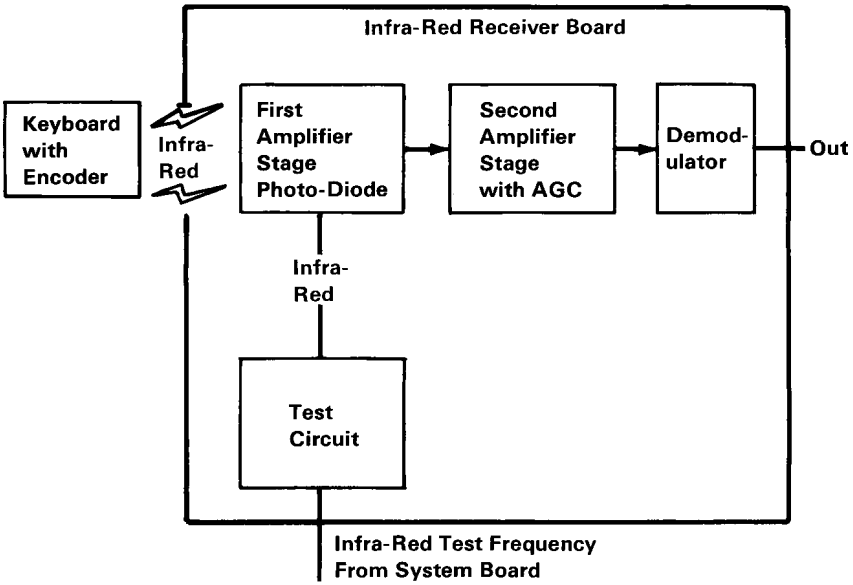
The following figure is the Infra-Red Receiver Block Diagram. During keyboard operation, the emitted light is modulated, transmitted, and received in the following sequence:

1. A key is pushed.

2. The data stream is sent using the infra-red-emitting diodes.
3. The receiver amplifies and processes the signal.
4. The demodulated signal is sent to the system board.

The signal received consists of an infra-red-light transmission modulated at 40 kHz.

An input is available (I/R Test Frequency) to the system for receiver-circuit-operational verification.



Infra-Red Receiver Block Diagram

Application Notes

The Infra-Red Receiver Board can serve as a general-purpose infra-red-receiver, however, the

demodulator timings are tailored to the needs of the system.

Programming Considerations

The serially-encoded word is software de-serialized by the 8088 processor on the system unit. The leading edge of the start bit will generate a non-maskable interrupt (NMI). Once the processor enters the NMI routine to handle the deserialization, the keyboard-data line is sampled and the processor waits to sample the trailing edge of the start bit. When the trailing edge of the start bit is sampled, the processor will wait for 310 μs and sample the first half of the first data bit. This delay causes the processor to sample in the nominal center of the first half of the first data bit. The processor then samples the keyboard data every half-bit cell-time. The sampling interval is 220 μs. The processor samples each half-bit-sample 5 times and will determine the logical level of the sample by majority rule. This enables the processor to discriminate against transient glitches and to filter out noise. The 8088 processor utilizes one 8255 PPI bit (PORT C BIT 6) and shares one 8253 timer channel (CHANNEL 1) to do the software de-serialization of the keyboard data. See the "Cordless Keyboard" in this section for more information on the data-transmission protocal.

Detectable Error Conditions

Errors	Cause
Phase Errors	The 1st half of the bit-cell sample is not equal to the inverse of the 2nd half of the bit-cell sample.
Parity Errors	The received encoded word did not maintain odd parity.

Note: Errors will be signaled by the processor with a short tone from the audio alarm or external speaker.

Operational Parameters

The operational distance from infra-red devices to the system should not exceed 6.1 meters (20 feet) (line-of-sight). Operational efficiency can be impaired by outside sources. These sources are, excessively-bright lights, and high-voltage lines, which include some TV sets. High-energy sources will generally cause an audible alarm within the system unit. These sources may downgrade the operational distance from the keyboard to the system. A keyboard cable is recommended if the above interference conditions are not controllable.

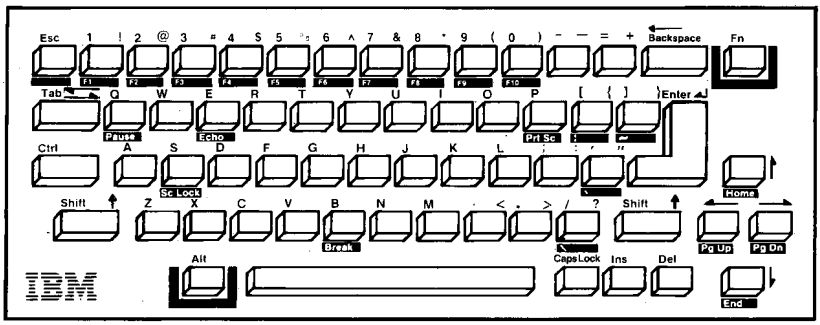
Pin	Signal	Input/Output
A01	+12 Volts	Input
A02	Ground	Input
A03	Ground-Shield	Input
A04	I.R. TEST FREQ.	Input
B01	GROUND	Input
B02	+5 Volts	Input
B03	–I.R. KBD DATA	Output
B04	GROUND	Input

Infra-Red Connector Specifications

IBM PC*jr* Cordless Keyboard

The keyboard is a low-profile, 62-key, detached keyboard with full-travel keys. The keys are arranged in a standard typewriter layout with the addition of a function key and cursor-control keys. The keybuttons are unmarked; however, an overlay is used to provide the keys' functional descriptions.

The following figure shows the layout of the cordless keyboard.



The keyboard is battery powered and communicates to the system unit with an infra-red (IR) link. The infra-red link makes the remote keyboard a truly portable hand-held device. An optional-cord connection to the system unit is available. Power is sent to the keyboard and serially-encoded data received by the system unit through the optional cord. When connected, the cord's keyboard-connector removes the battery power and the -CABLE CONNECT signal disables the infra-red-receiver circuit. The disabling of the circuit also allows other infrared devices to be used

without interfering with the system. The data which is received through the IR link or by the cord, have the same format.

The keyboard interface is designed to maximize system-software flexibility in defining keyboard operations such as shift states of keys, and typematic operation. This is accomplished by having the keyboard return scan codes rather than American National Standard Code for Information Interchange (ASCII) codes. The scan codes are compatible with Personal Computer and Personal Computer XT scan codes at the BIOS interface level. All of the keys are typematic and generate both a make and a break scan-code. For example, key 1 produces scan code hex 01 on make and code hex 81 on break. Break codes are formed by adding hex 80 to the make codes. The keyboard I/O driver can define keyboard keys as shift keys or typematic, as required by the application.

The microprocessor in the keyboard performs keyboard scanning, phantom-key detection, key debounce, buffering of up to 16 key-scan-codes, and transfer of serially-encoded data to the system unit. The keyboard microprocessor is normally in a standby power-down mode until a key is pressed. This causes the microprocessor to scan the keyboard. The microprocessor then transmits the scan code, and re-enters the power-down mode if its buffer is empty and no keys are pressed.

The keyboard electronics is designed with low-power CMOS integrated-circuitry for battery power operation. Four AA-size batteries are required. Because the keyboard is normally in the standby power-down mode, which uses very little power, no on/off switch is needed.

Unlike other keyboards in the IBM Personal Computer family, the IBM PC*jr* Cordless Keyboard has phantom-key detection. Phantom-key detection occurs when invalid combinations of three or more keys are pressed simultaneously, causing a hex 55 scan-code to be sent to the keyboard's processor. The phantom-key scan-code instructs the keyboard's processor to ignore all of the keys that were pressed at that time. BIOS ignores the resulting scan-code that is sent to it.

The keyboard-cord connector provides a battery-disconnect function and also disables the infra-red-transmission circuitry when the mating plug for the modular jack is connected.

Note: See "Keyboard Encoding and Usage" in Section 5, for scan codes and further information.

Transmitter

Serially encoded words are transmitted to the system unit using the Infra-Red Link or the cable link. Encoded words are sent to the system unit with odd parity. Both the Infra-Red Link and the cable link use biphase serial-encoding and each is a simplex link.

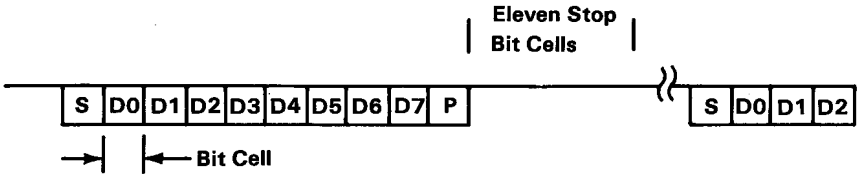
The 80C48 microprocessor does the biphase serial encoding with a bit cell of 440 μs. A biphase logically-encoded 1 is transmitted as logical 1 for the first half of the bit cell time and as a logical 0 for the second half of the bit cell. A biphase logically-encoded 0 is transmitted as a logical 0 for the first half of the bit cell time and as a logical 1 for the second half of the bit cell.

Each logical 1 transmission for the Infra-Red Link consists of a 40 kHz carrier burst at a 50% duty cycle.

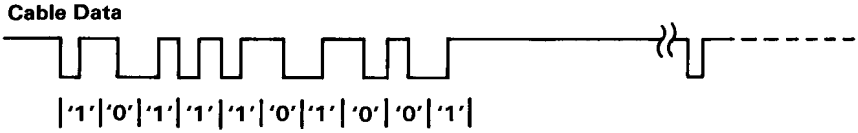
First Bit	Start Bit
Second Bit	Data Bit 0 (Least Significant Bit)
Third Bit	Data Bit 1
Fourth Bit	Data Bit 2
Fifth Bit	Data Bit 3
Sixth Bit	Data Bit 4
Seventh Bit	Data Bit 5
Eight Bit	Data Bit 6
Ninth Bit	Data Bit 7 (Most Significant Bit)
Tenth Bit	Parity Bit
Eleventh Bit	Stop Bit

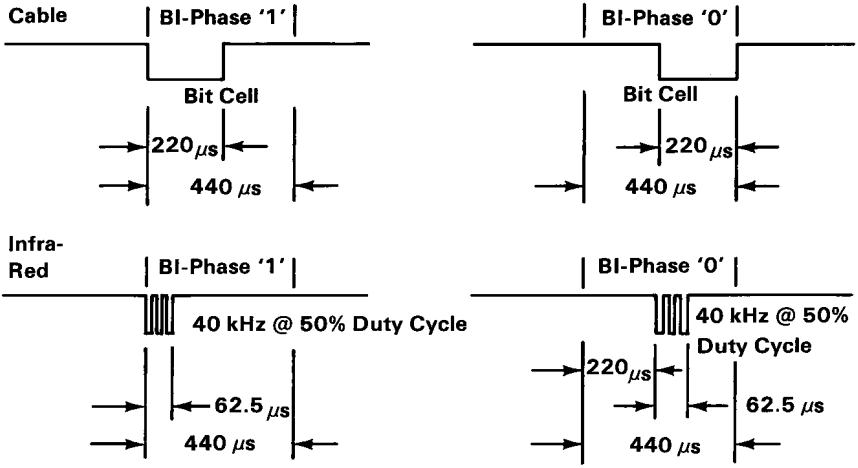
Data Stream Sequence

Eleven stop bits are inserted after every scan-code transmission. This is to allow some processor bandwidth between keystrokes to honor other types of interrupts, such as serial and time-of-day.

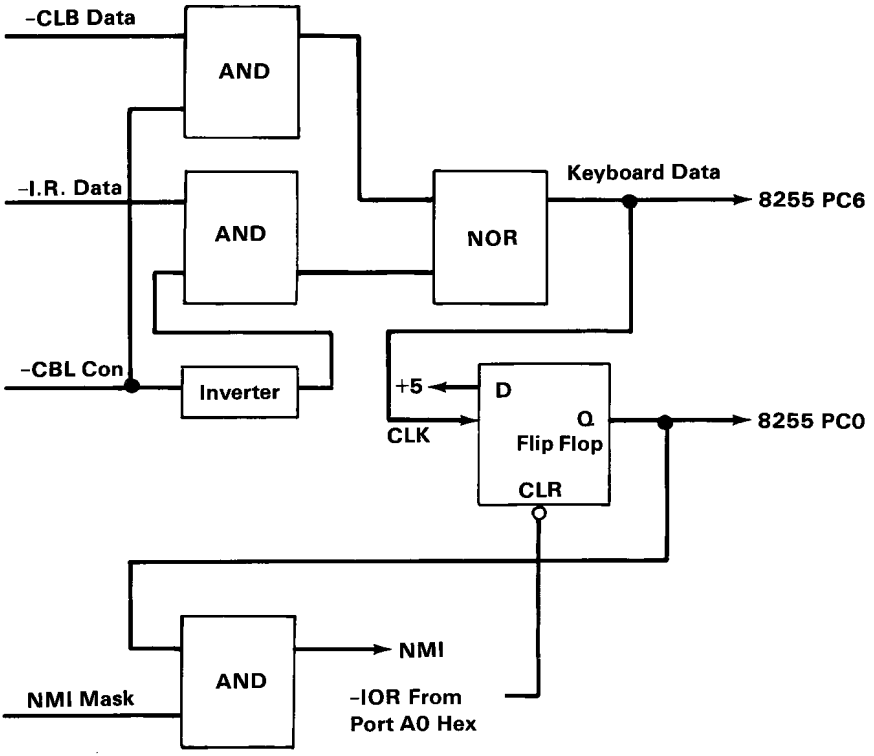


Example: DATA = "2EH" PARITY = '1'





Keyboard Transmission Timing



Keyboard Interface Logic

Program Cartridge and Interface

The Program Cartridge allows the addition of ROM to the system without removing the cover by plugging it into either of two slots in the front of the machine.

The 48 by 72 mm (2 by 3 inch) cartridge can hold one or two 32K byte by 8 ROMS (64K bytes total) of program storage. Smaller ROMS such as the 8K byte by 8 modules can be used in the cartridge. When a smaller module is used, the higher address lines are not used. To allow two smaller modules to be mapped to adjacent memory segments, each module's contents is addressed to multiple adjacent-memory segments, within the addressable range of the module's socket (32k).

Program Cartridge Slots

The Program Cartridge is designed to plug into either of two identical slots in the front of the machine. Each slot has 15 address signals, 8 data signals, 6 chip selects, 2 control signals, and power. Cartridge selection is accomplished by the chip selects, each of which addresses one of the high 32K memory-blocks. Each cartridge uses up to two of the six chip selects. Selection is determined on the basis of the intended use of the cartridge. This is done at the factory.

Two of the chip selects are used by the internal system-ROM. These two signals can be used to allow the internal ROM to be replaced by a Program Cartridge. This allows the machine to assume a different personality from the standard machine. To use this option of mapping the internal-ROM space to a cartridge, the Base-ROM-in-Cartridge function must be inserted. This function is a factory-installed

signal-jumper manufactured into particular program-cartridges that are intended to replace the system ROM.

Note: When the cartridge is inserted or removed with the system turned on, the system will 'reset' and go through a warm power-up. Any data in the system RAM will be lost.

Cartridge Storage Allocations

A. The following conventions will be followed for "Initial Program Loadable" program cartridges:

Location	Contents
0	055H
1	0AAH
2	Length
3,4,5	Jump to Initialize Code
6	0
Last 2 Addresses	CRC Bytes

Storage Conventions

- Locations 0 and 1 contain the word hex 55AA. This is used as a test for the presence of the cartridge during the configuration- determination portion of the power-on routines.
- Location 2 contains a length indicator representing the entire address space taken by the ROM on the cartridge. The algorithm for determining the