Schematics

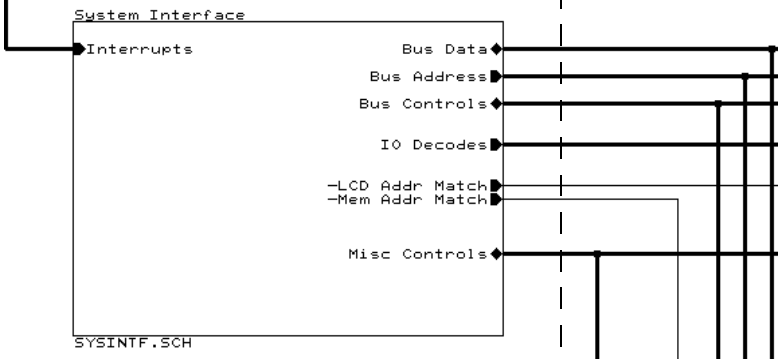
This appendix has all of the original schematic drawings, in their proper order, for your perusal. The schematics accompanying the text in each chapter are slightly different, because I omitted some connections that weren't relevant to the subject at hand. Here, you'll get the full story.

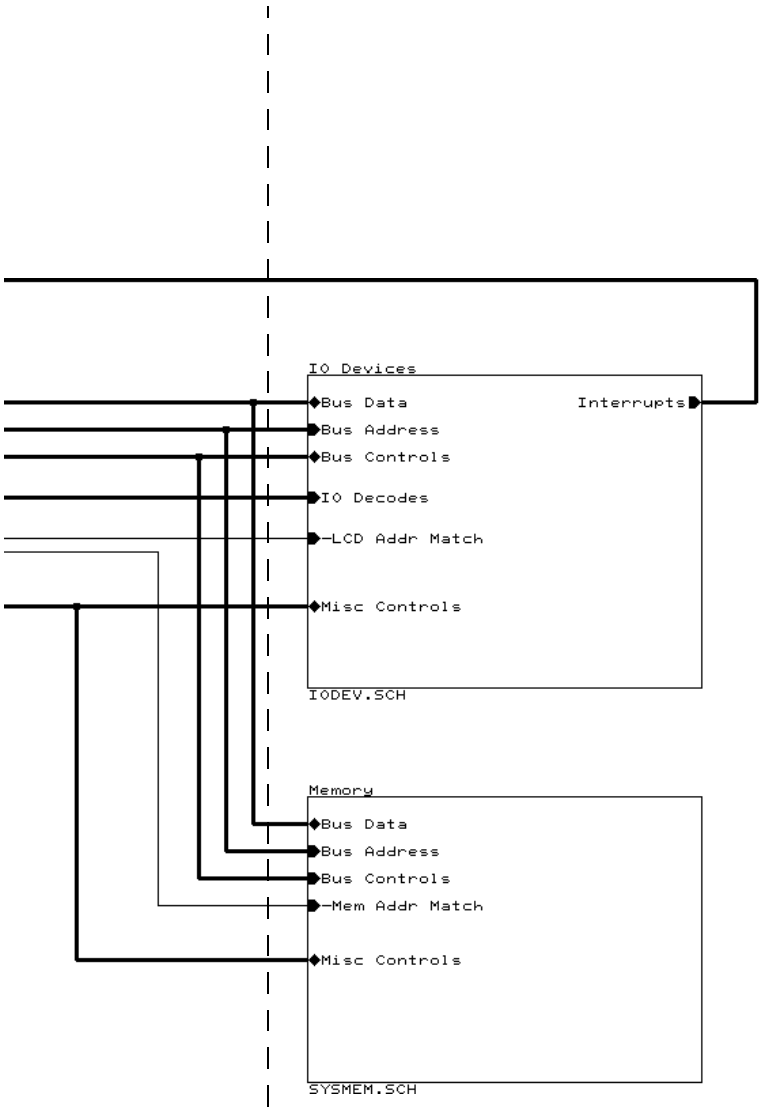
Each pair of facing pages holds a single schematic page with about an inch of overlap. The two dotted lines near the gutter in the middle mark the overlap boundaries, so you can rejoin the pieces fairly easily: squash the book down on a copier, blip the Copy button, trim one half to the line, overlap it with the other, and paste 'em together.

The source code diskette includes these schematics as `TIFF` files that you can load into nearly any graphics program and print on your own printer. After you decompress them, they'll take up about 3.5 MB on your disk and even more when you import them as graphic files. Check the `ReadMe` file for more information!

You'll find tables listing all the I/O ports, control and status bits, and memory addresses, as well as a Bill of Material, after the schematics. You can use those tables as a ready reference as you trace through the schematics.

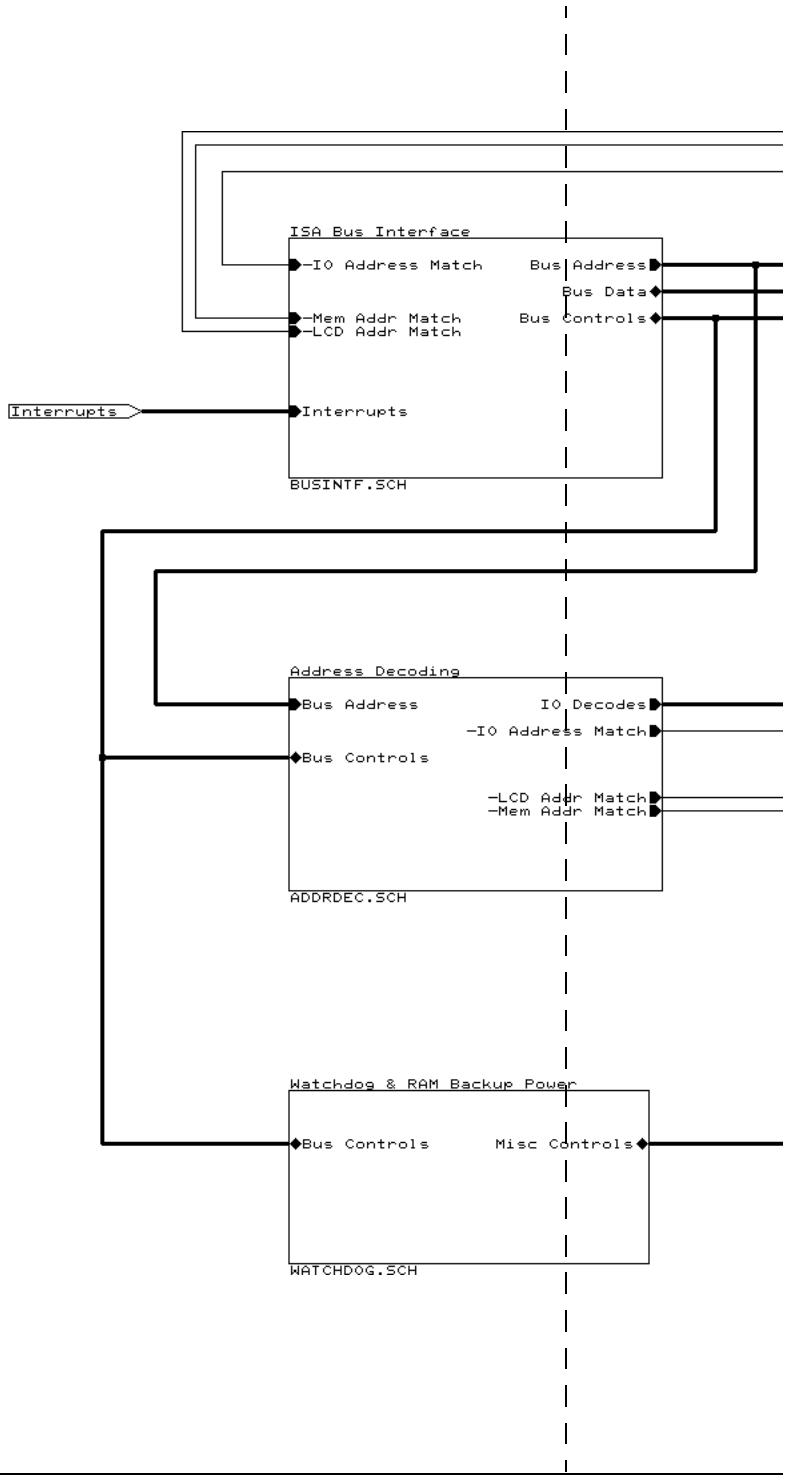
Enjoy!

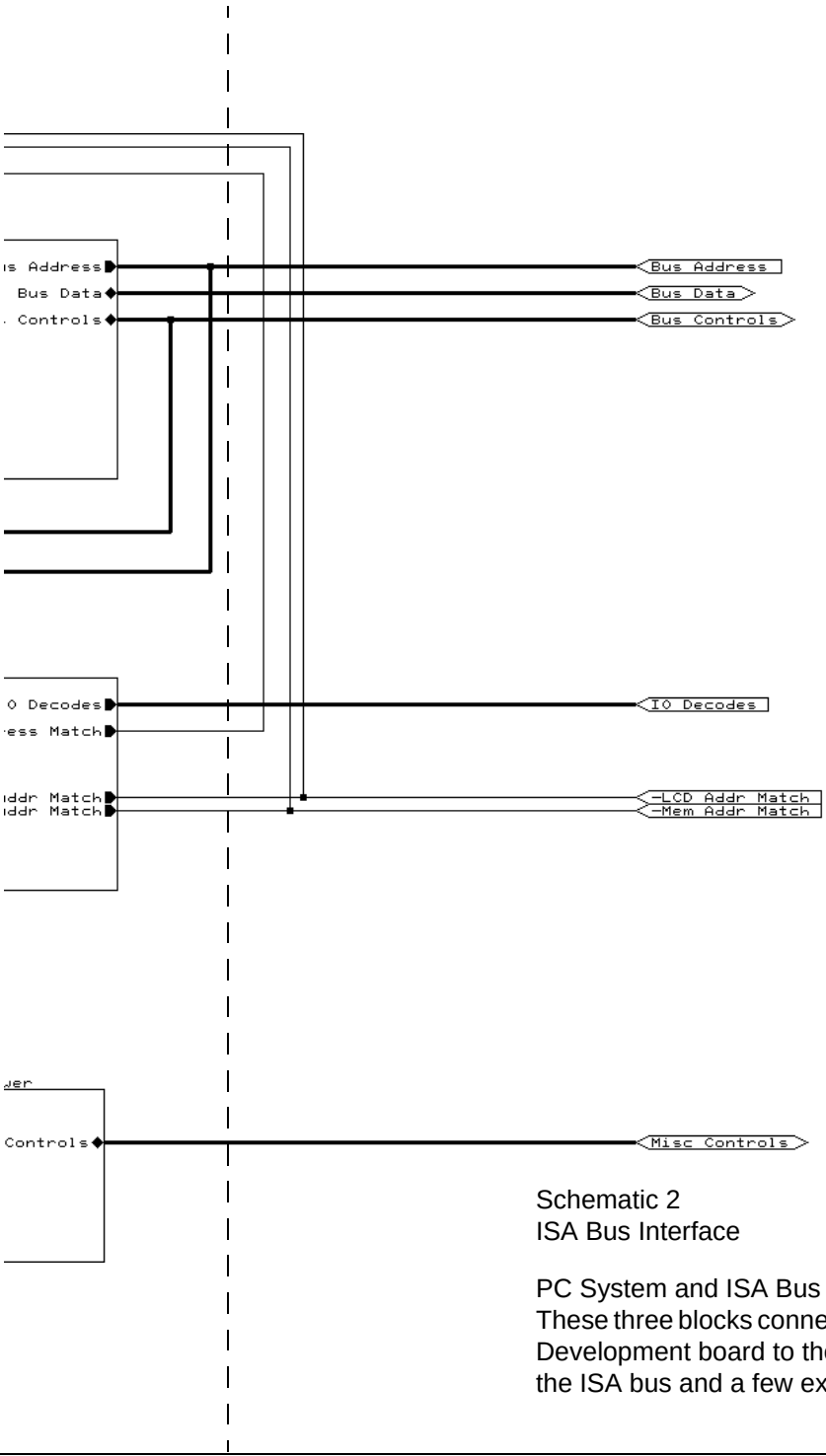

System Interface
Interrupts
Bus Data
Bus Address
Bus Controls
IO Decodes
-LCD Addr Match
-Mem Addr Match
Misc Controls
SYSINTF.SCH



Schematic 1
Board Overview

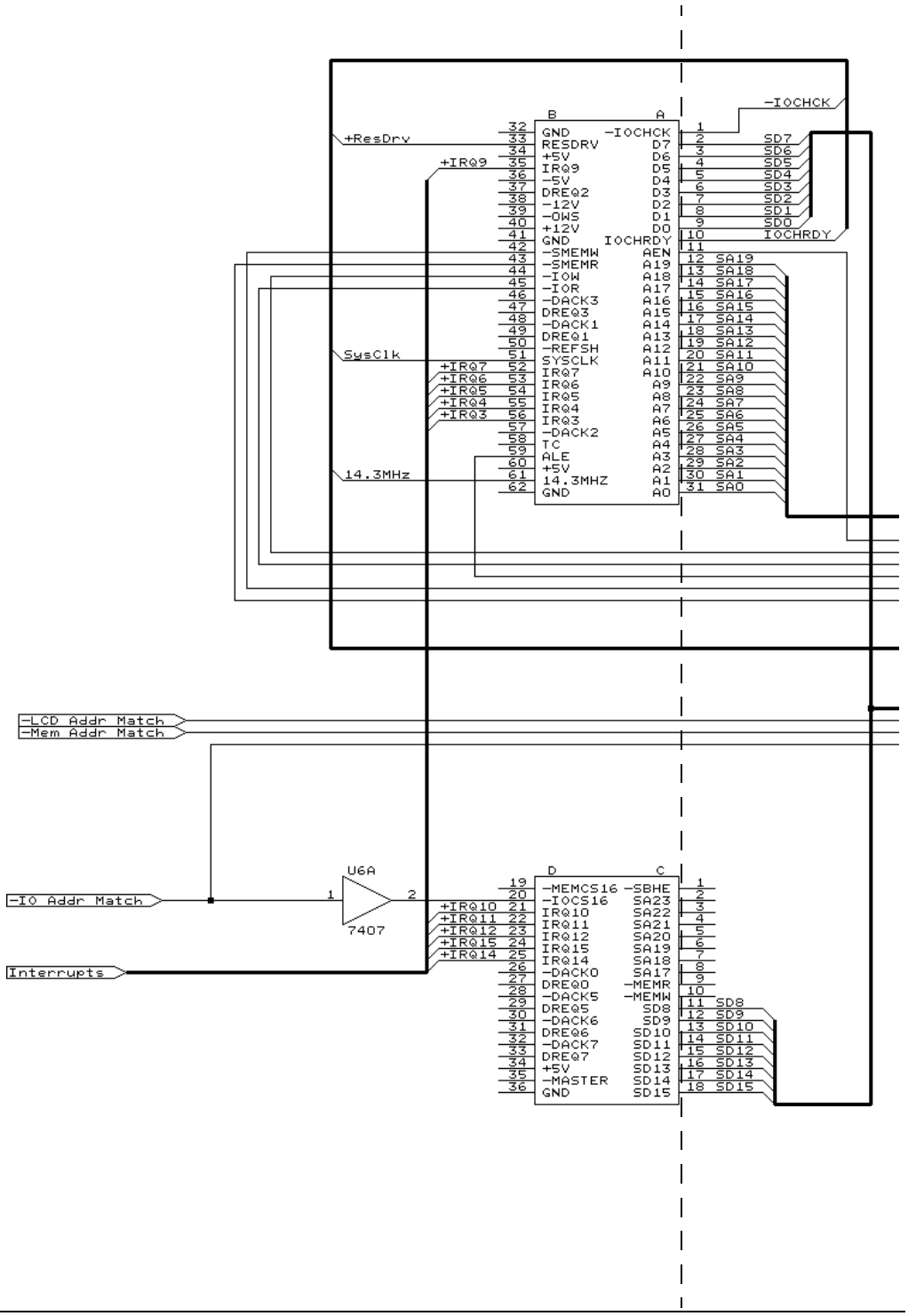
The Firmware Development Board has three major functional blocks. The next pages explore each block in detail.

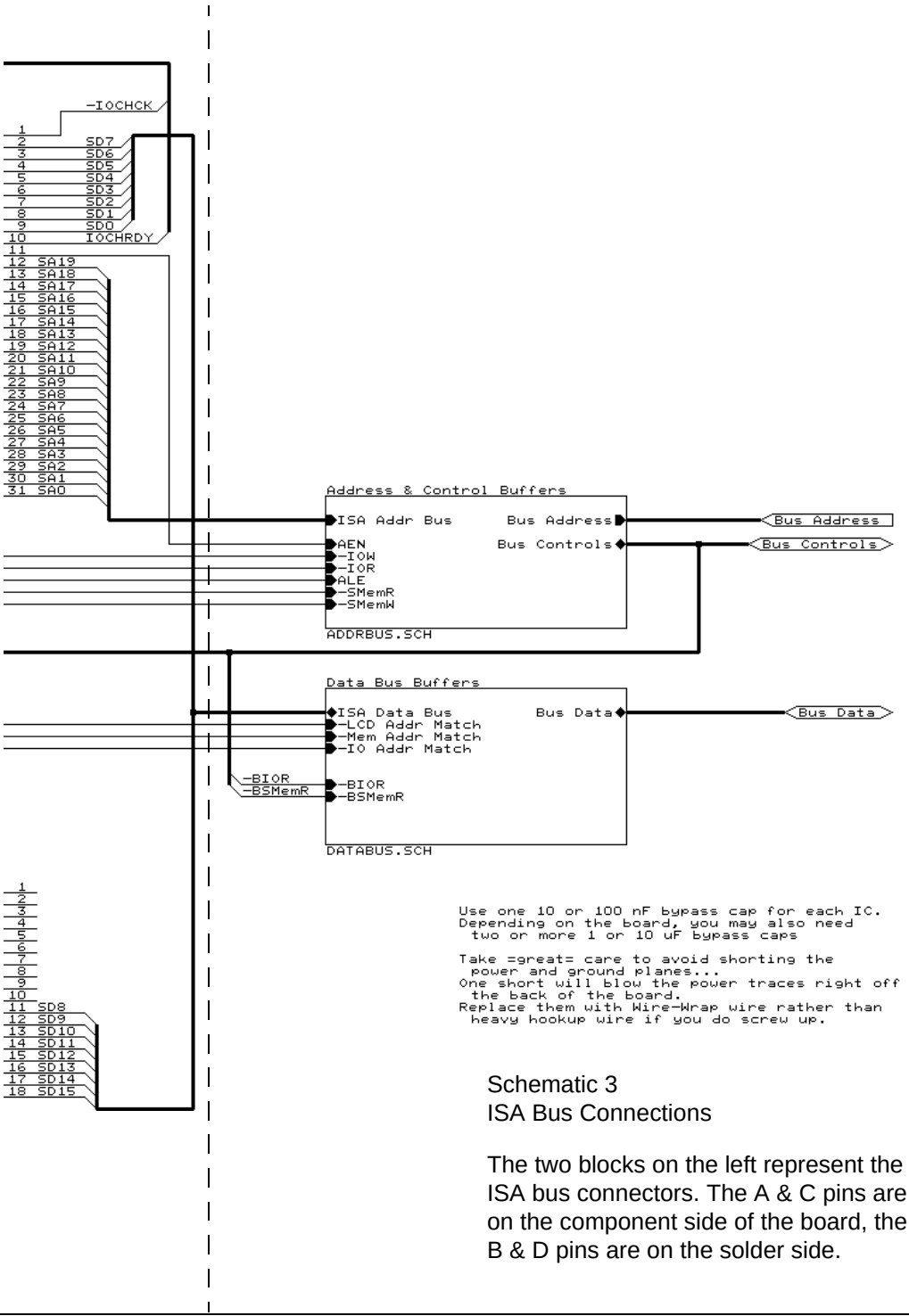

ISA Bus Interface
-IO Address Match
Bus Address
Bus Data
-Mem Addr Match
-LCD Addr Match
Bus Controls
Interrupts
Interrupts
BUSINTF.SCH
Address Decoding
Bus Address
IO Decodes
-IO Address Match
Bus Controls
-LCD Addr Match
-Mem Addr Match
ADDRDEC.SCH
Watchdog & RAM Backup Power
Bus Controls
Misc Controls
WATCHDOG.SCH



Schematic 2
ISA Bus Interface

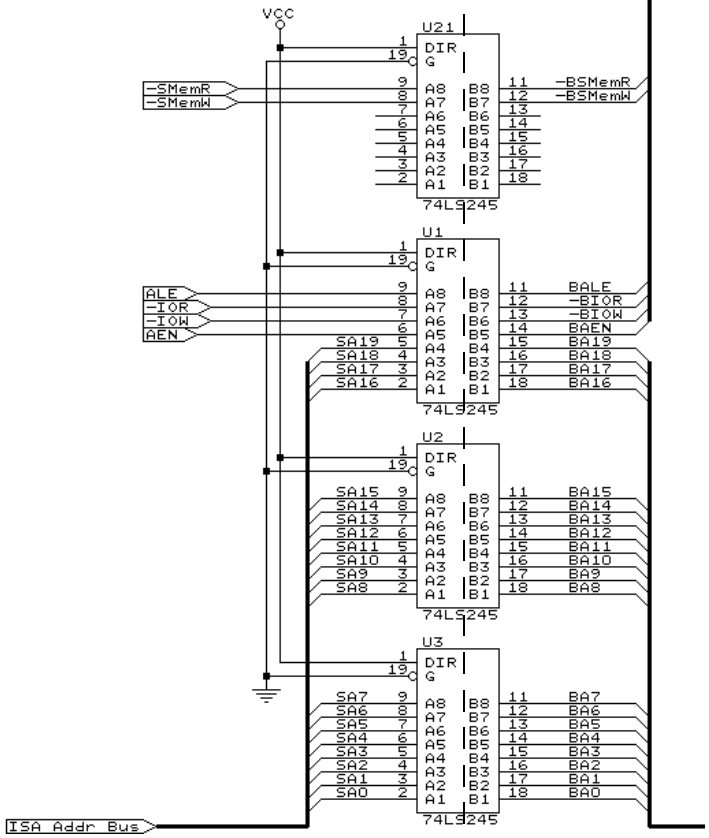
PC System and ISA Bus Interface
These three blocks connect the Firmware Development board to the PC through the ISA bus and a few external wires.

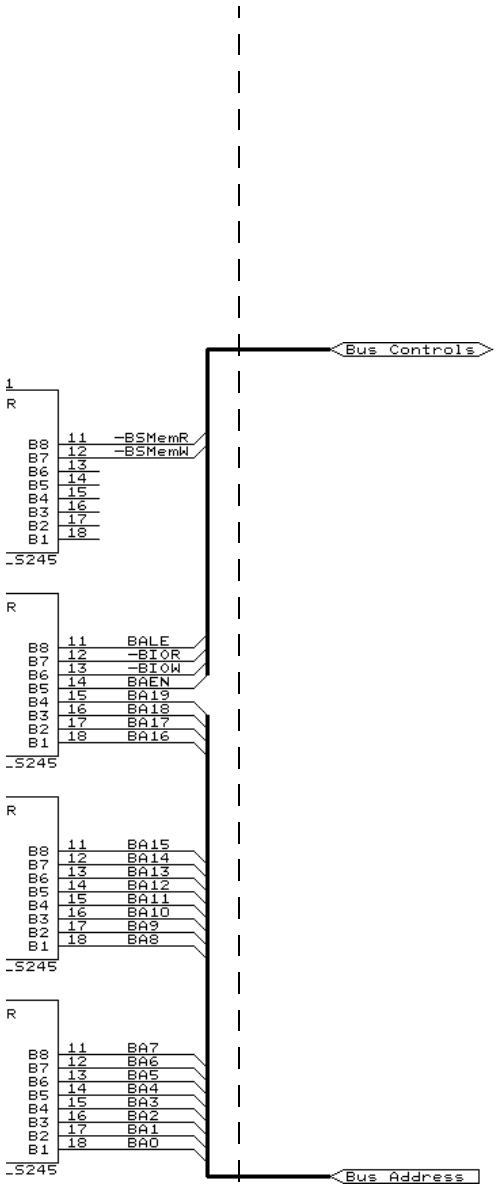




Schematic 3
ISA Bus Connections

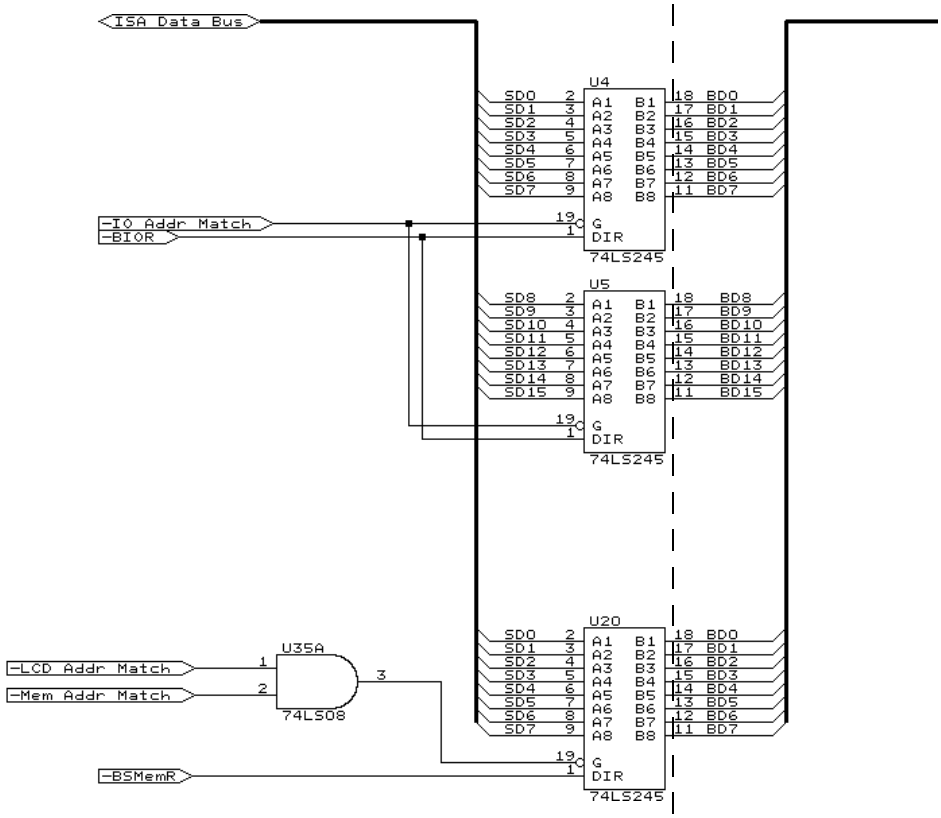
The two blocks on the left represent the ISA bus connectors. The A & C pins are on the component side of the board, the B & D pins are on the solder side.

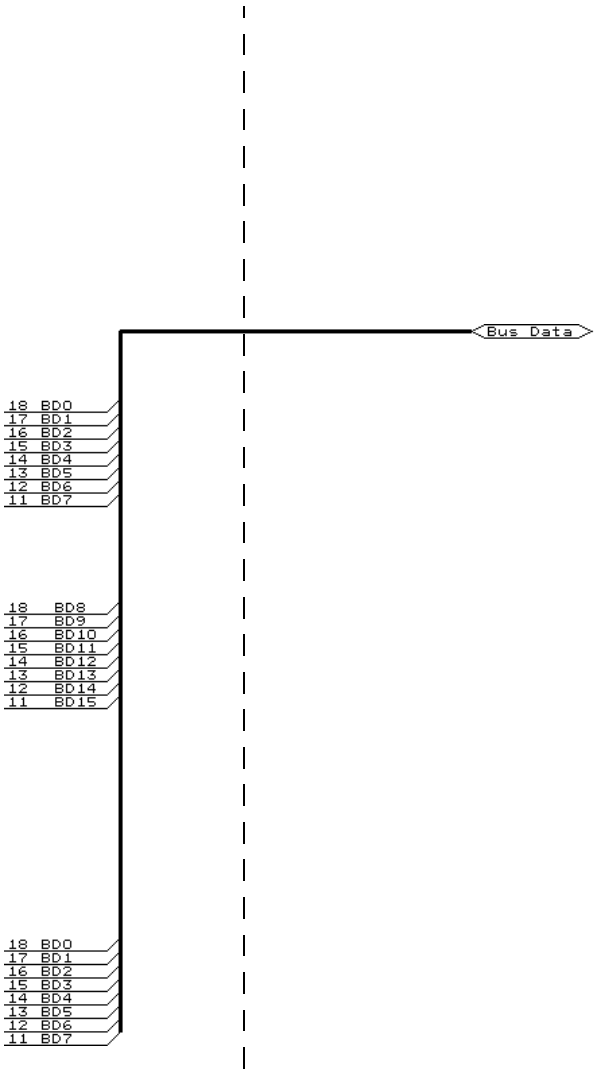




Schematic 4
Address & Control Buffers

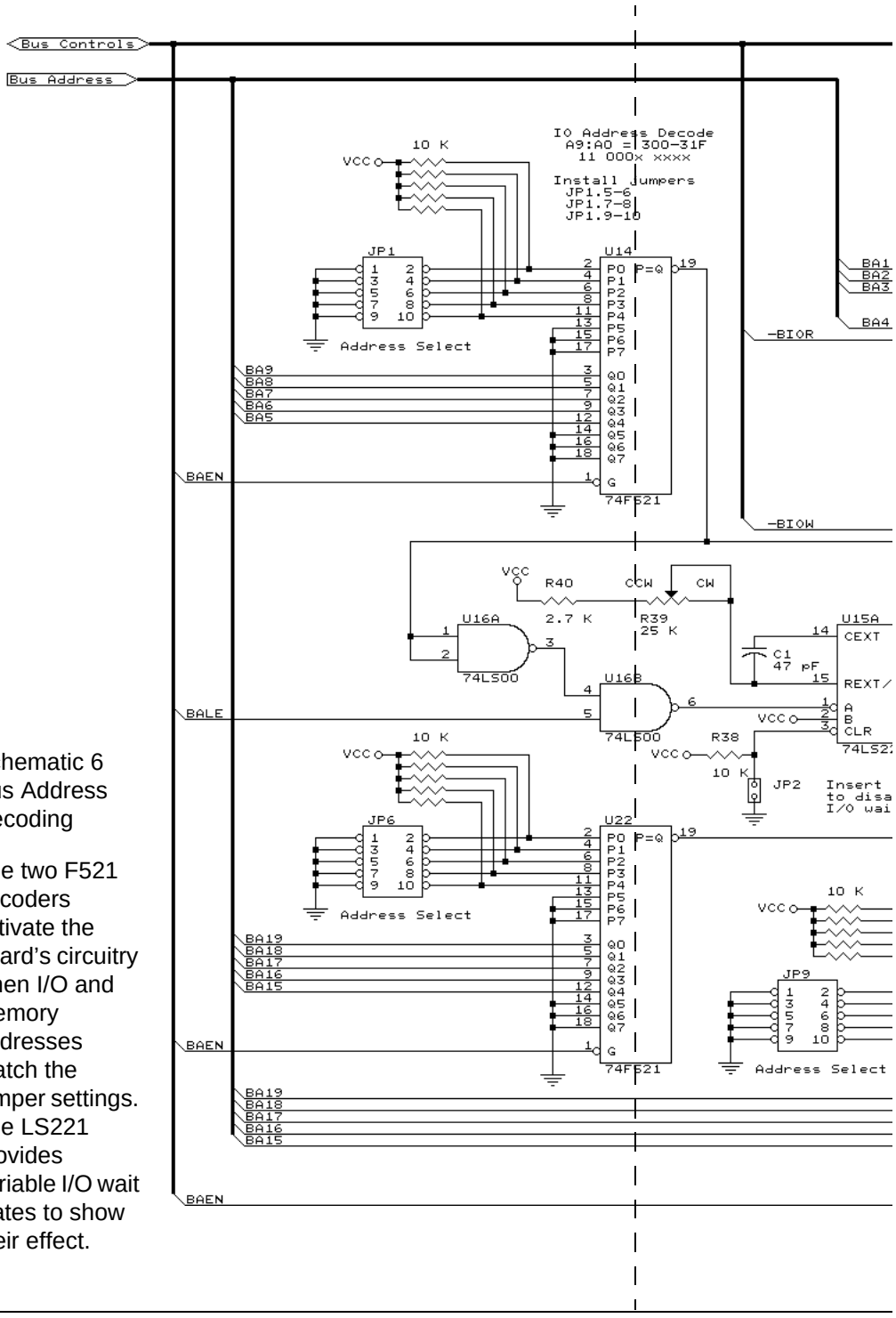
These chips provide the proper isolation and loading on the ISA bus. The buffers are always active, so their outputs always track the current bus signals.


ISA Data Bus
U4
SD0 2
SD1 3
SD2 4
SD3 5
SD4 6
SD5 7
SD6 8
SD7 9
A1 B1
A2 B2
A3 B3
A4 B4
A5 B5
A6 B6
A7 B7
A8 B8
18 BD0
17 BD1
16 BD2
15 BD3
14 BD4
13 BD5
12 BD6
11 BD7
-IO Addr Match
-BIOR
19
1
G
DIR
74LS245
U5
SD8 2
SD9 3
SD10 4
SD11 5
SD12 6
SD13 7
SD14 8
SD15 9
18 BD8
17 BD9
16 BD10
15 BD11
14 BD12
13 BD13
12 BD14
11 BD15
U20
U35A
-LCD Addr Match
-Mem Addr Match
1
2
3
74LS08
-BSMemR



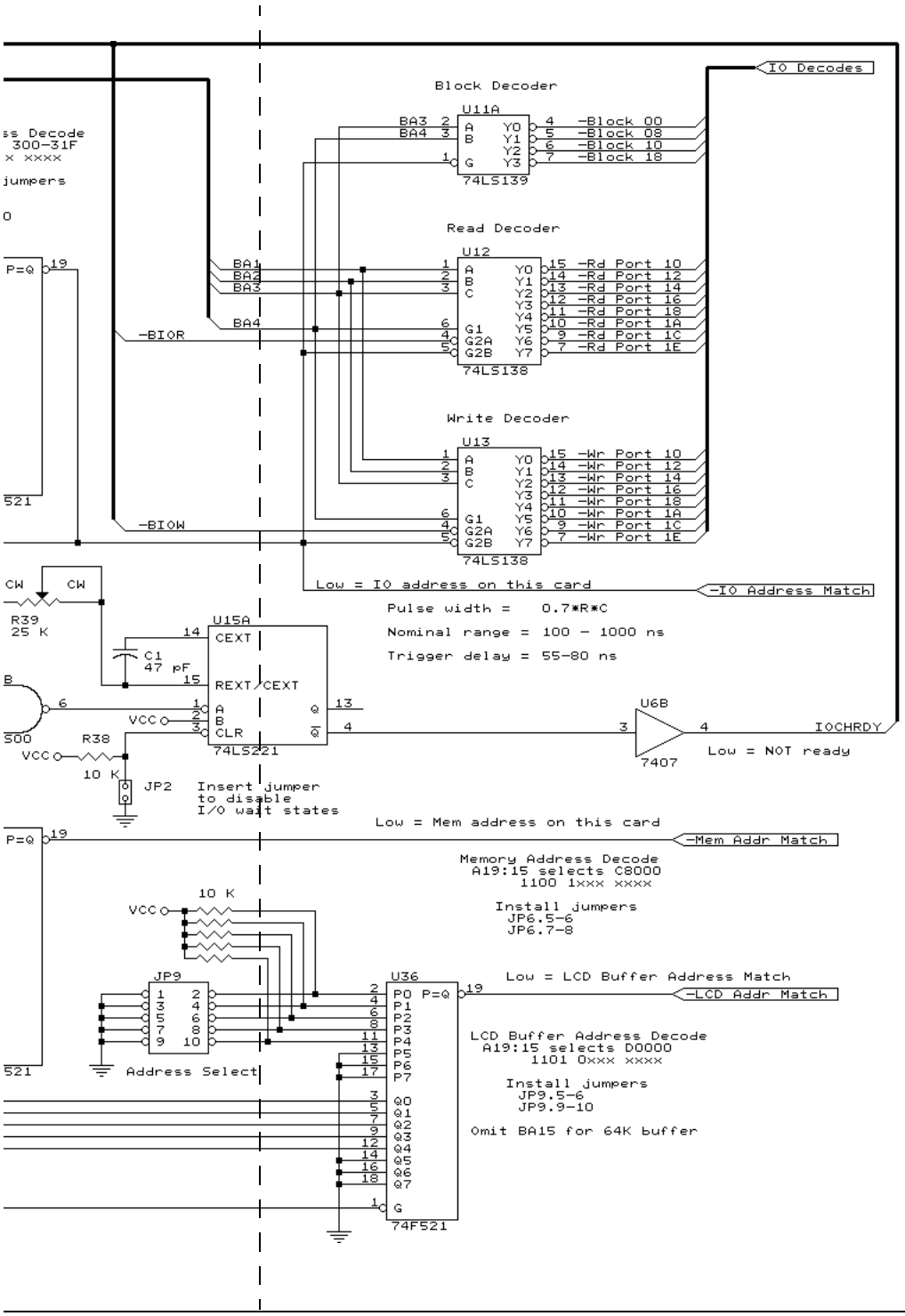
Schematic 5
Data Bus Buffers

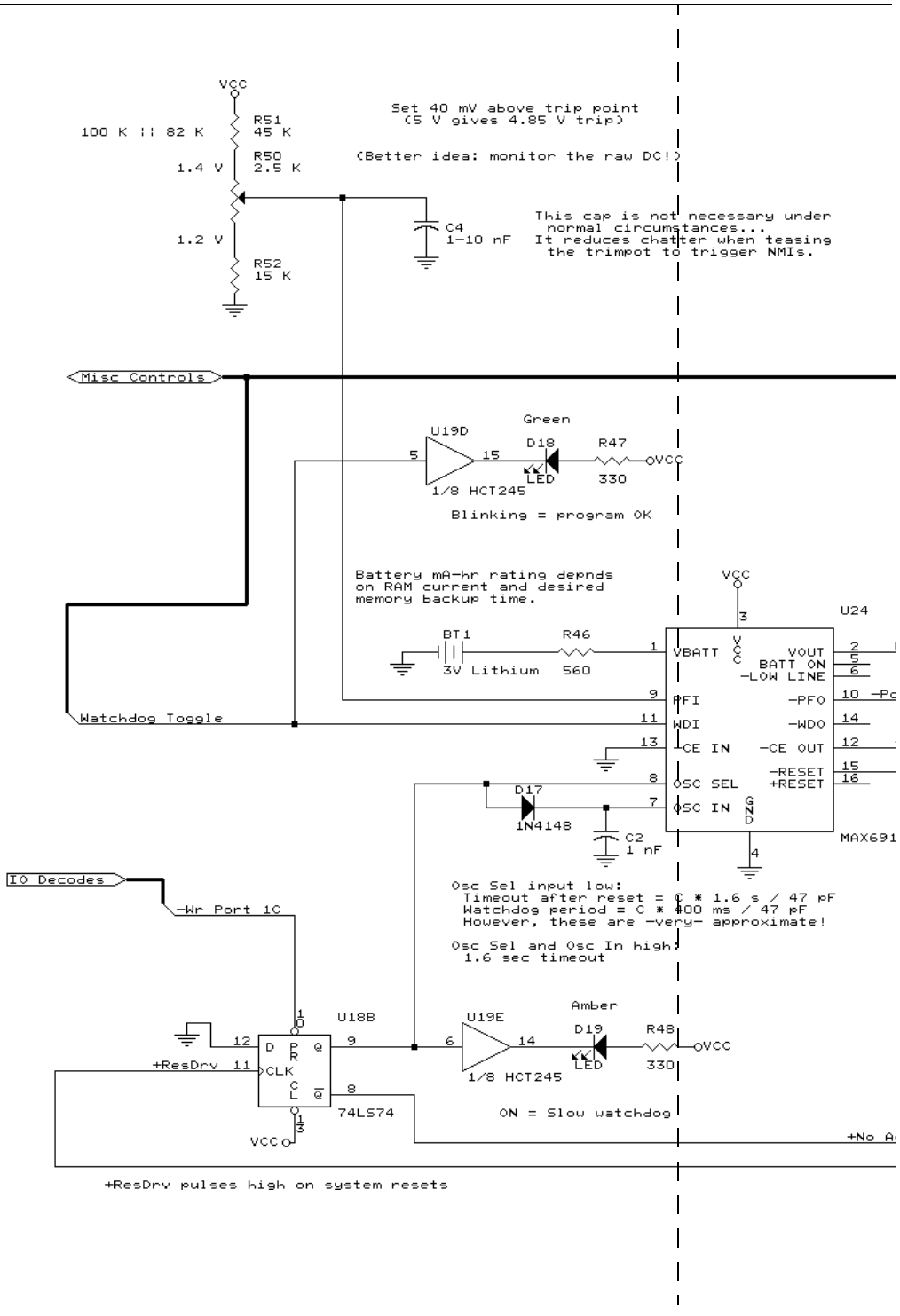
These chips provide bidirectional control of the data bus signals for I/O and memory accesses. Note that memory accesses use 8-bit transfers, not 16-bit.

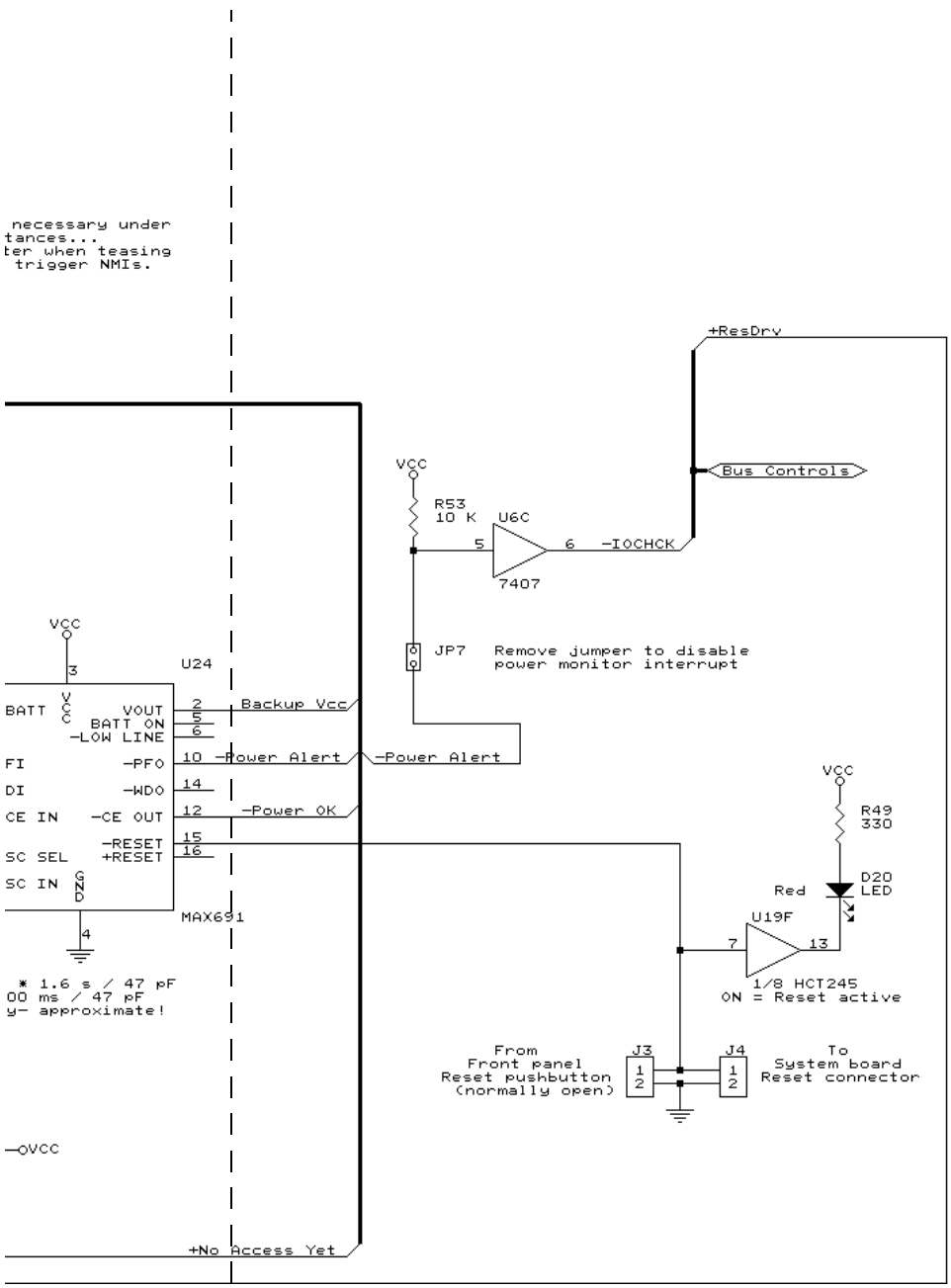


Schematic 6 Bus Address Decoding

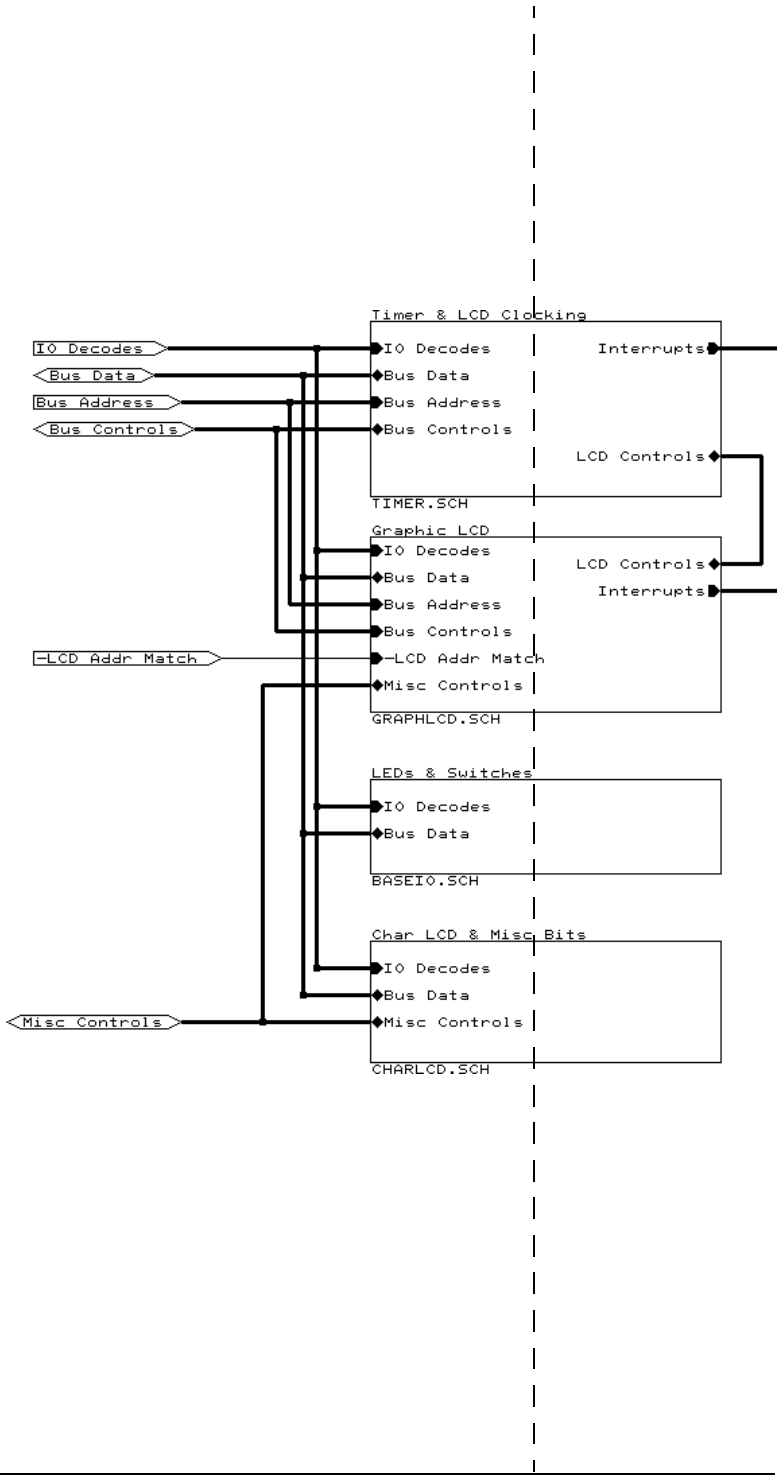
The two F521 decoders activate the board's circuitry when I/O and memory addresses match the jumper settings. The LS221 provides variable I/O wait states to show their effect.

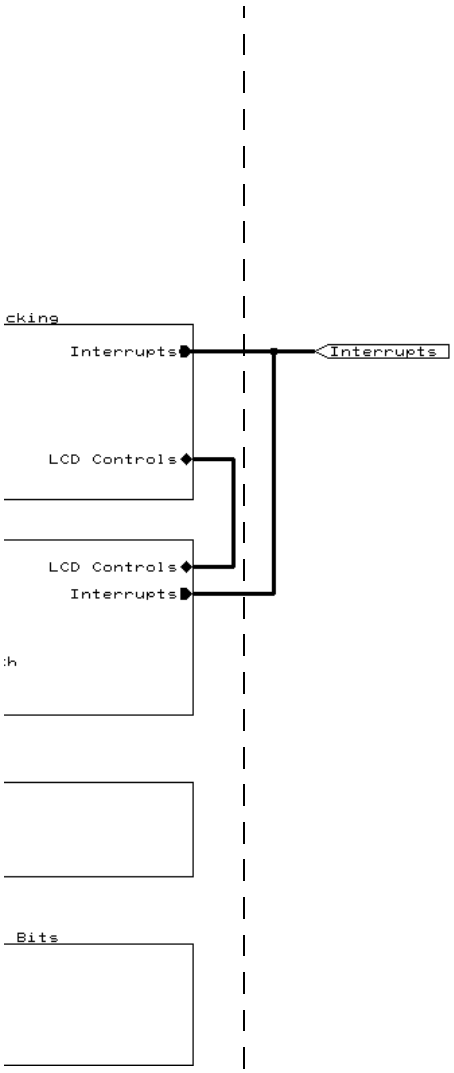

I0 Decodes
Block Decoder
U11A
74LS139
-Block 00
-Block 08
-Block 10
-Block 18
Read Decoder
U12
74LS138
-Rd Port 10
-Rd Port 12
-Rd Port 14
-Rd Port 16
-Rd Port 18
-Rd Port 1A
-Rd Port 1C
-Rd Port 1E
Write Decoder
U13
74LS138
-Wr Port 10
-Wr Port 12
-Wr Port 14
-Wr Port 16
-Wr Port 18
-Wr Port 1A
-Wr Port 1C
-Wr Port 1E
-BI0R
-BI0W
Low = I0 address on this card
-I0 Address Match
Pulse width = 0.7*R*C
Nominal range = 100 - 1000 ns
Trigger delay = 55-80 ns
R39
25 K
C1
47 pF
U15A
74LS221
R38
10 K
JP2
Insert jumper
to disable
I/O wait states
U6B
7407
IOCHRDY
Low = NOT ready
Low = Mem address on this card
-Mem Addr Match
Memory Address Decode
A19:15 selects C8000
1100 1xxx xxxx
Install jumpers
JP6.5-6
JP6.7-8
JP9
Address Select
U36
74F521
Low = LCD Buffer Address Match
-LCD Addr Match
LCD Buffer Address Decode
A19:15 selects D0000
1101 0xxx xxxx
Install jumpers
JP9.5-6
JP9.9-10
Omit BA15 for 64K buffer


VCC
R51
45 K
100 K || 82 K
R50
2.5 K
1.4 V
1.2 V
R52
15 K
Set 40 mV above trip point
(5 V gives 4.85 V trip)
(Better idea: monitor the raw DC!)
C4
1-10 nF
This cap is not necessary under
normal circumstances...
It reduces chatter when teasing
the trimpot to trigger NMIs.
Misc Controls
U19D
1/8 HCT245
Green
D18
LED
R47
330
VCC
Blinking = program OK
Battery mA-hr rating depnds
on RAM current and desired
memory backup time.
BT1
3V Lithium
R46
560
U24
VBATT
VOUT
BATT ON
-LOW LINE
PFI
-PFO
WDI
-WDO
-CE IN
-CE OUT
-RESET
+RESET
OSC SEL
OSC IN
GND
MAX691
Watchdog Toggle
D17
1N4148
C2
1 nF
Osc Sel input low:
Timeout after reset = C * 1.6 s / 47 pF
Watchdog period = C * 400 ms / 47 pF
However, these are -very- approximate!
Osc Sel and Osc In high:
1.6 sec timeout
IO Decodes
-Wr Port 1C
U18B
74LS74
+ResDrv
CLK
U19E
1/8 HCT245
Amber
D19
LED
R48
330
ON = Slow watchdog
+ResDrv pulses high on system resets



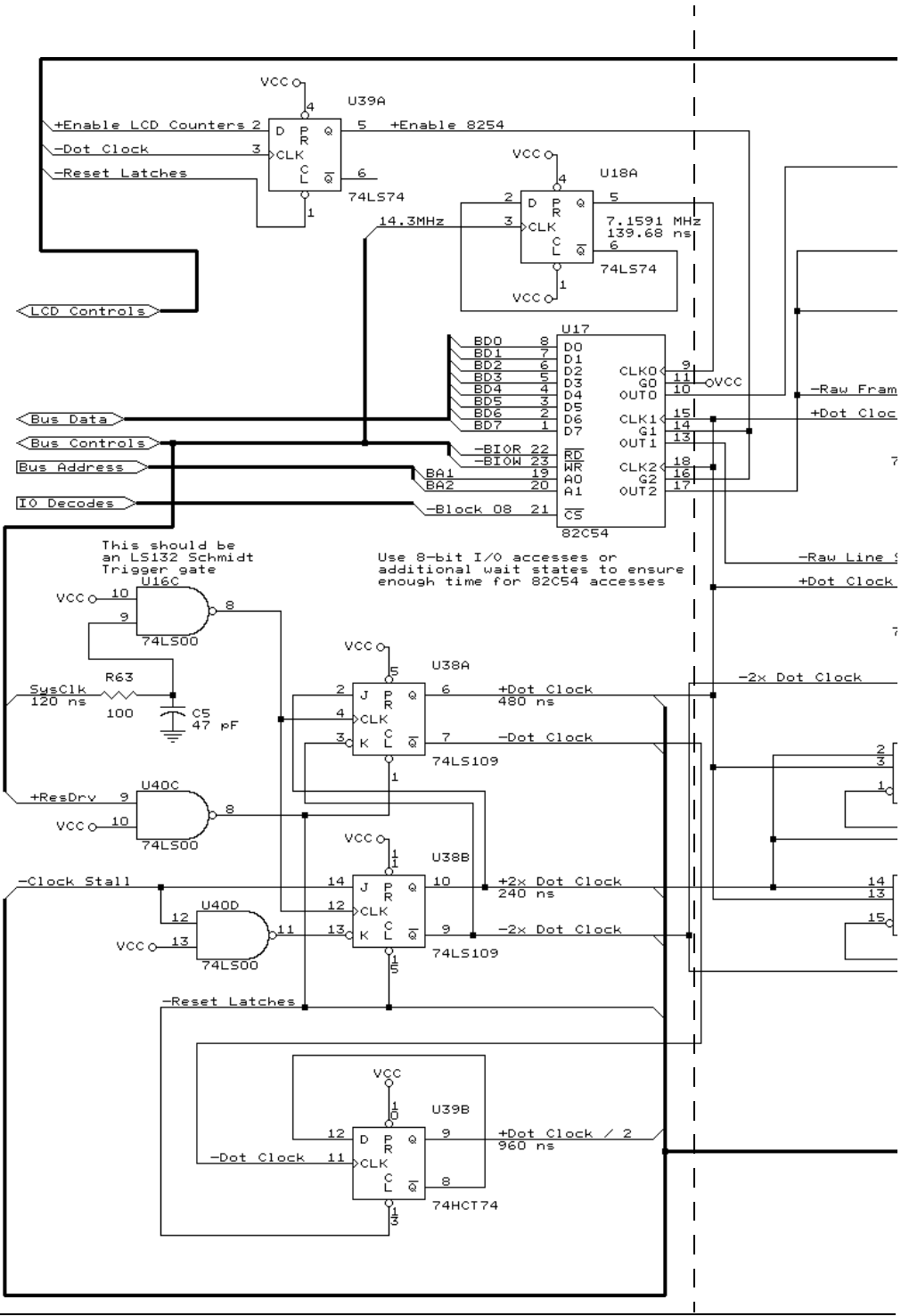
Schematic 7: Watchdog and Battery Backup
The MAX691 monitors the +5 V supply and triggers an NMI through the -IOCHCK bus line. Its watchdog timer output triggers a system reset using a wire to the Reset switch.

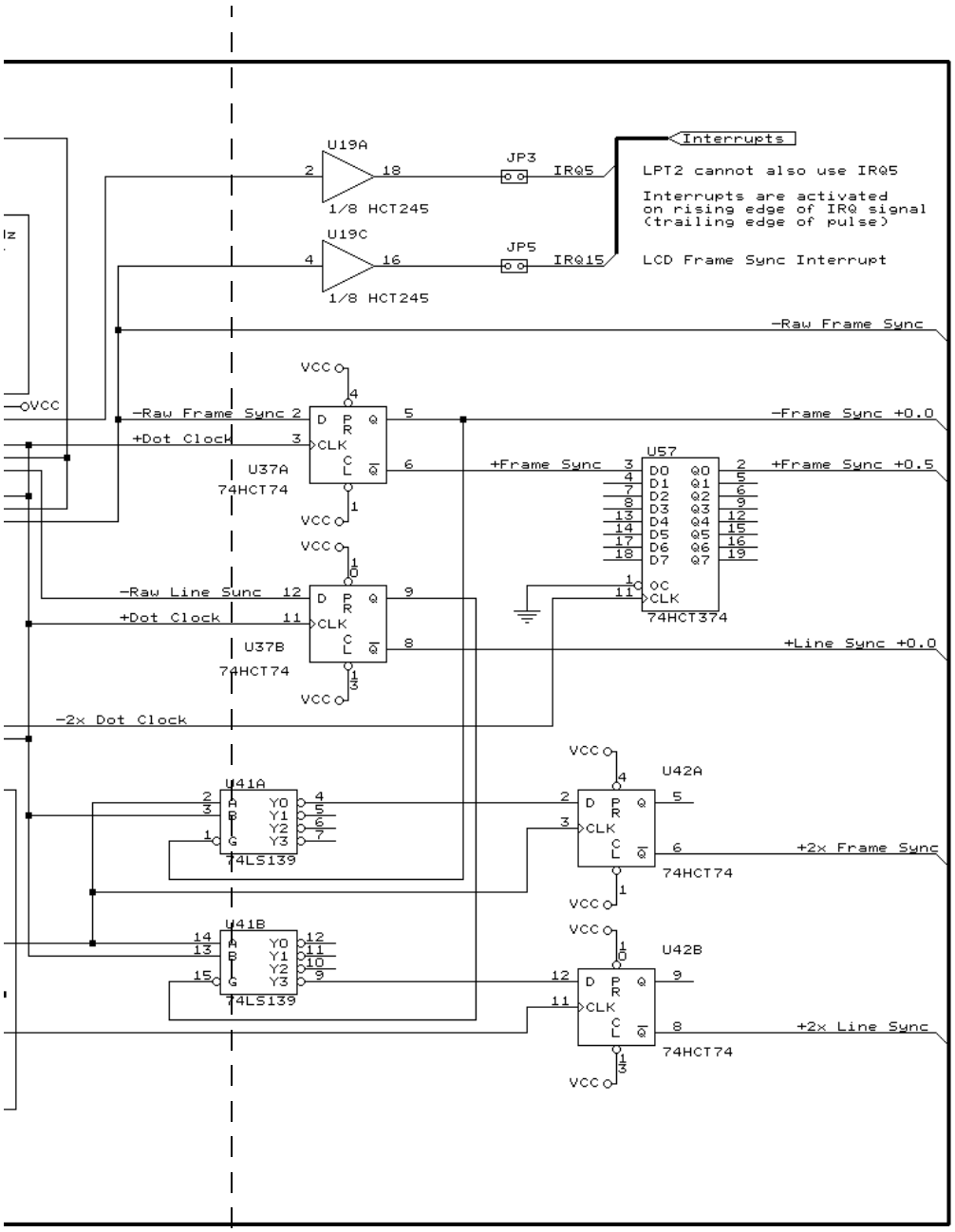

Timer & LCD Clocking
IO Decodes
Bus Data
Bus Address
Bus Controls
IO Decodes
Bus Data
Bus Address
Bus Controls
Interrupts
LCD Controls
TIMER.SCH
Graphic LCD
IO Decodes
Bus Data
Bus Address
Bus Controls
-LCD Addr Match
Misc Controls
LCD Controls
Interrupts
GRAPHLCD.SCH
LEDs & Switches
IO Decodes
Bus Data
BASEIO.SCH
Char LCD & Misc Bits
IO Decodes
Bus Data
Misc Controls
CHARLCD.SCH



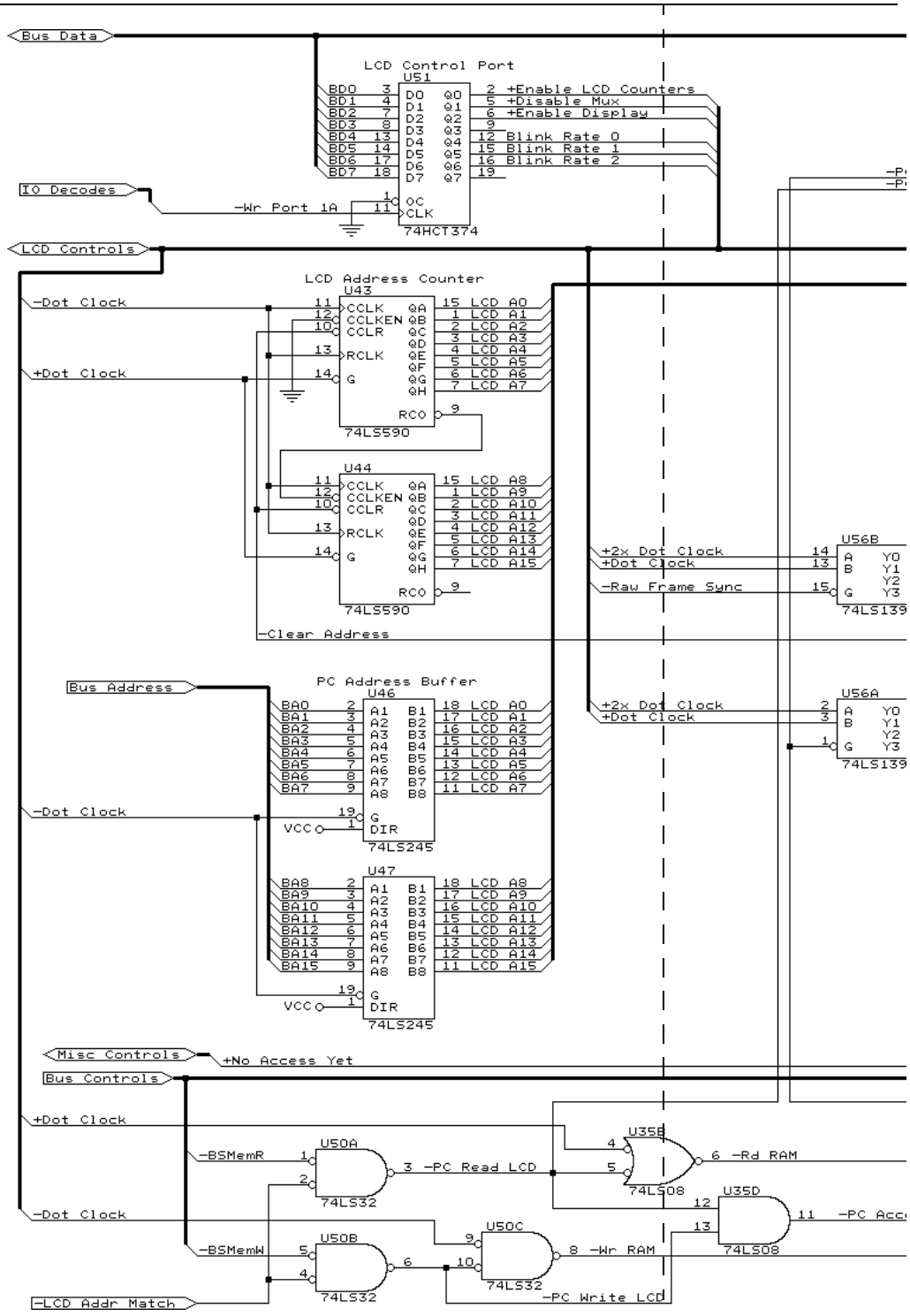
Schematic 8
I/O Devices

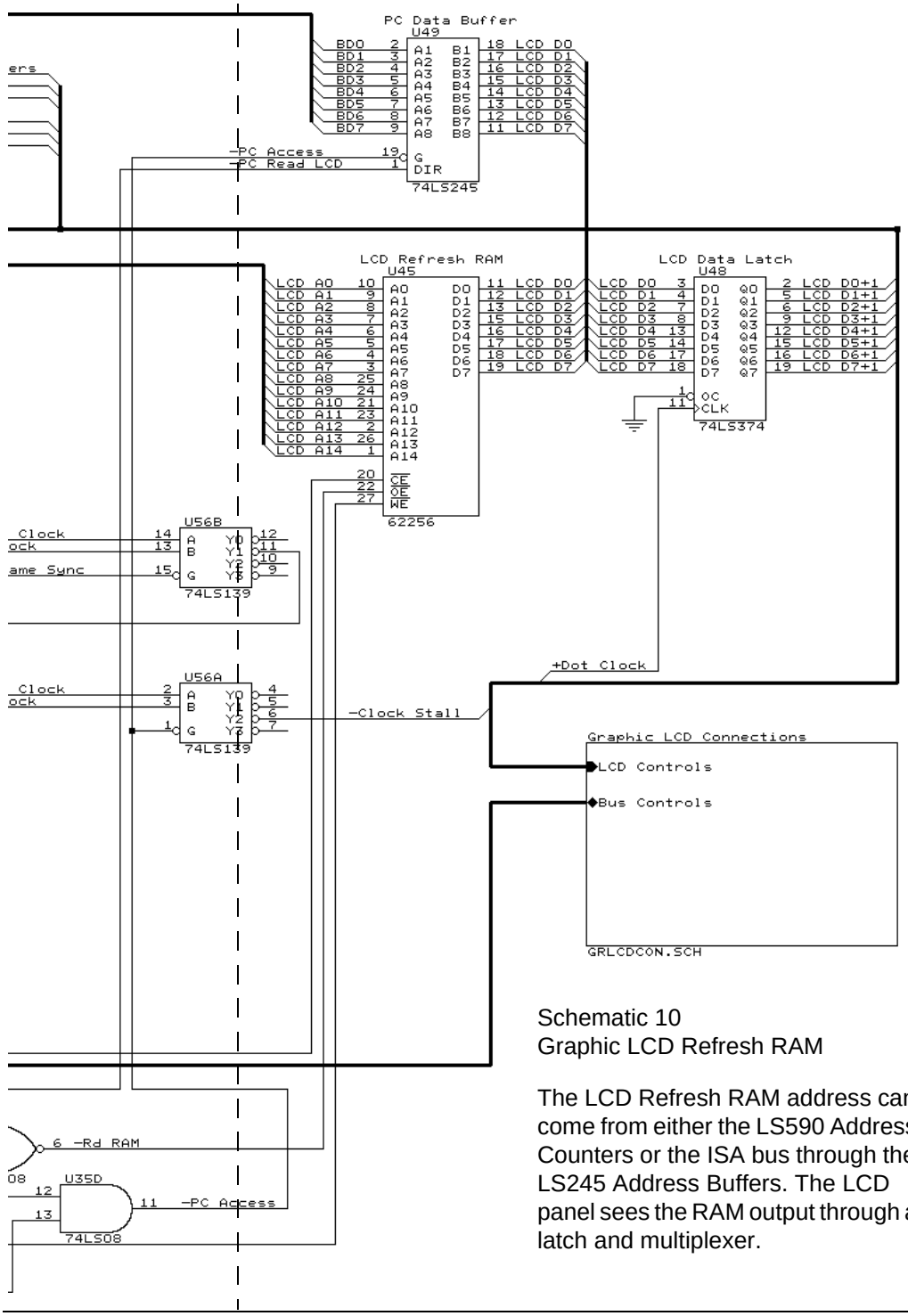
The Firmware Development Board includes three main I/O devices. Details of each gadget appear in successive pages.


VCC
U39A
+Enable LCD Counters
-Dot Clock
-Reset Latches
+Enable 8254
74LS74
U18A
14.3MHz
7.1591 MHz
139.68 ns
LCD Controls
U17
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
Bus Data
Bus Controls
Bus Address
IO Decodes
-BIOR
-BIOW
BA1
BA2
-Block 08
82C54
-Raw Fram
+Dot Cloc
-Raw Line
+Dot Clock
This should be an LS132 Schmidt Trigger gate
U16C
74LS00
Use 8-bit I/O accesses or additional wait states to ensure enough time for 82C54 accesses
SysClk
120 ns
R63
100
C5
47 pF
U38A
+Dot Clock
480 ns
-Dot Clock
74LS109
-2x Dot Clock
+ResDrv
U40C
U38B
-Clock Stall
U40D
+2x Dot Clock
240 ns
-Reset Latches
U39B
+Dot Clock / 2
960 ns
74HCT74



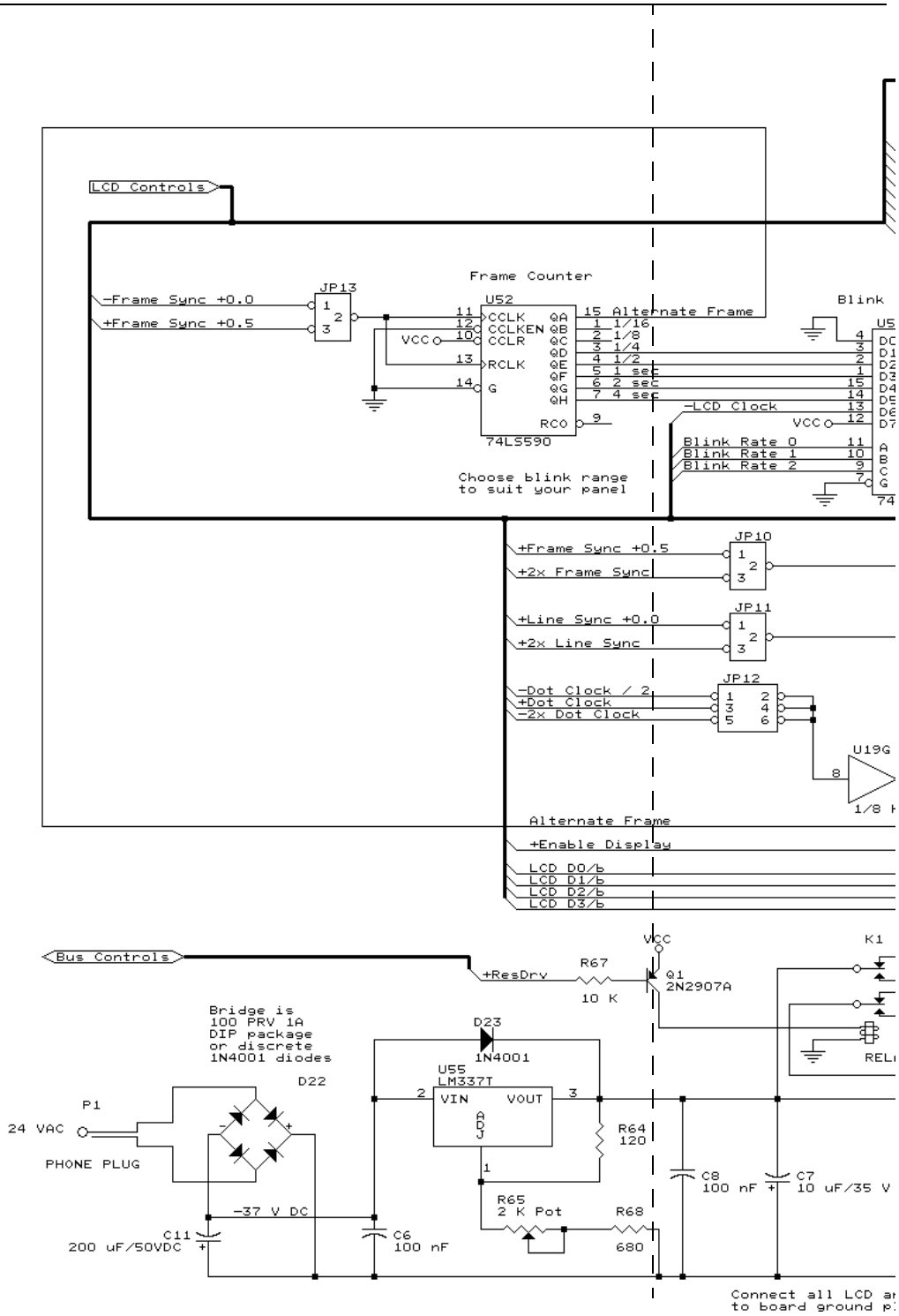
Schematic 9: Timer and LCD Clocking
The 82C54 timer can supply generally useful interrupts or control the Graphic LCD interface, the latter of which accounts for most of the support circuitry in this schematic.

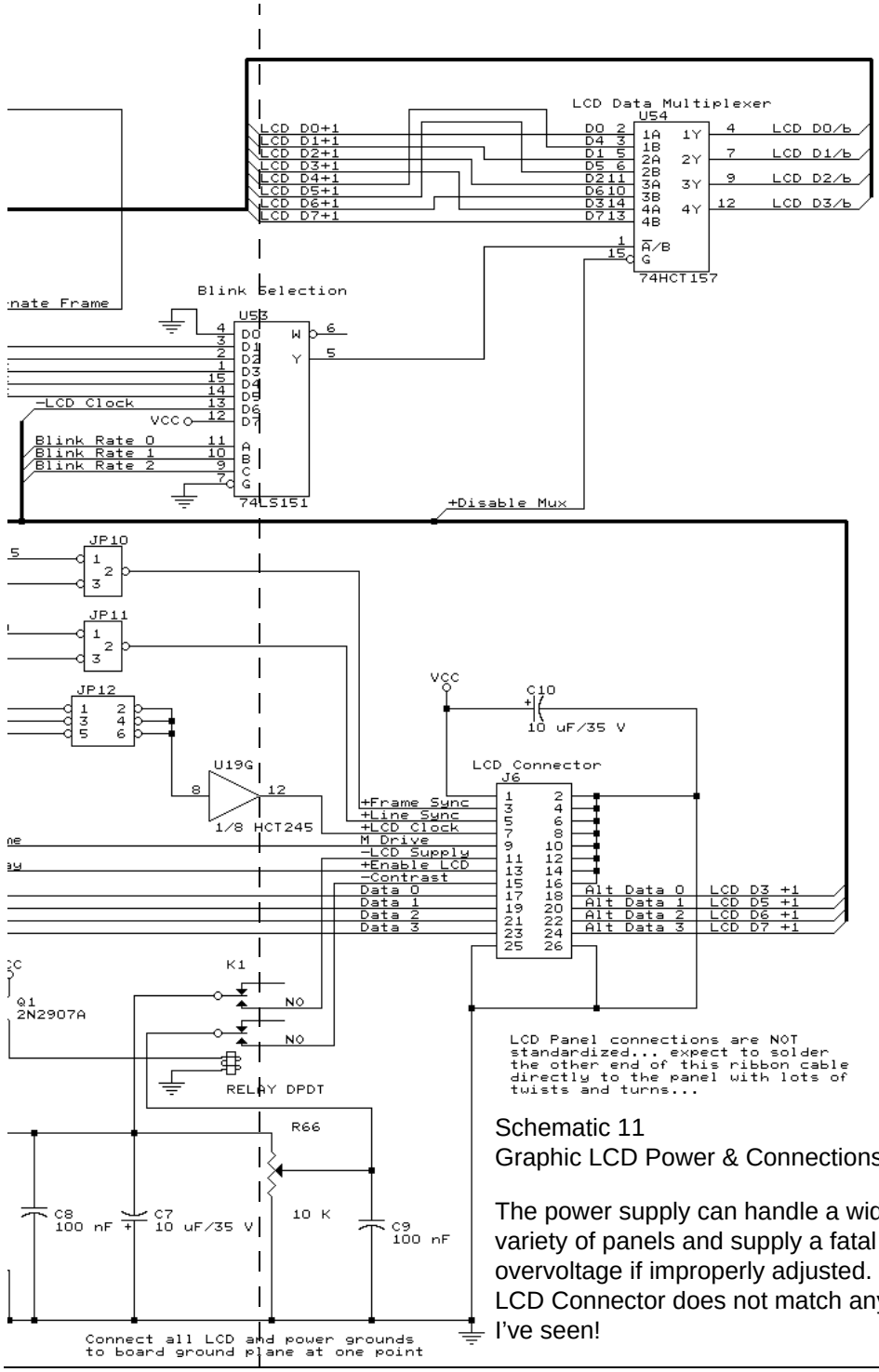




Schematic 10
Graphic LCD Refresh RAM

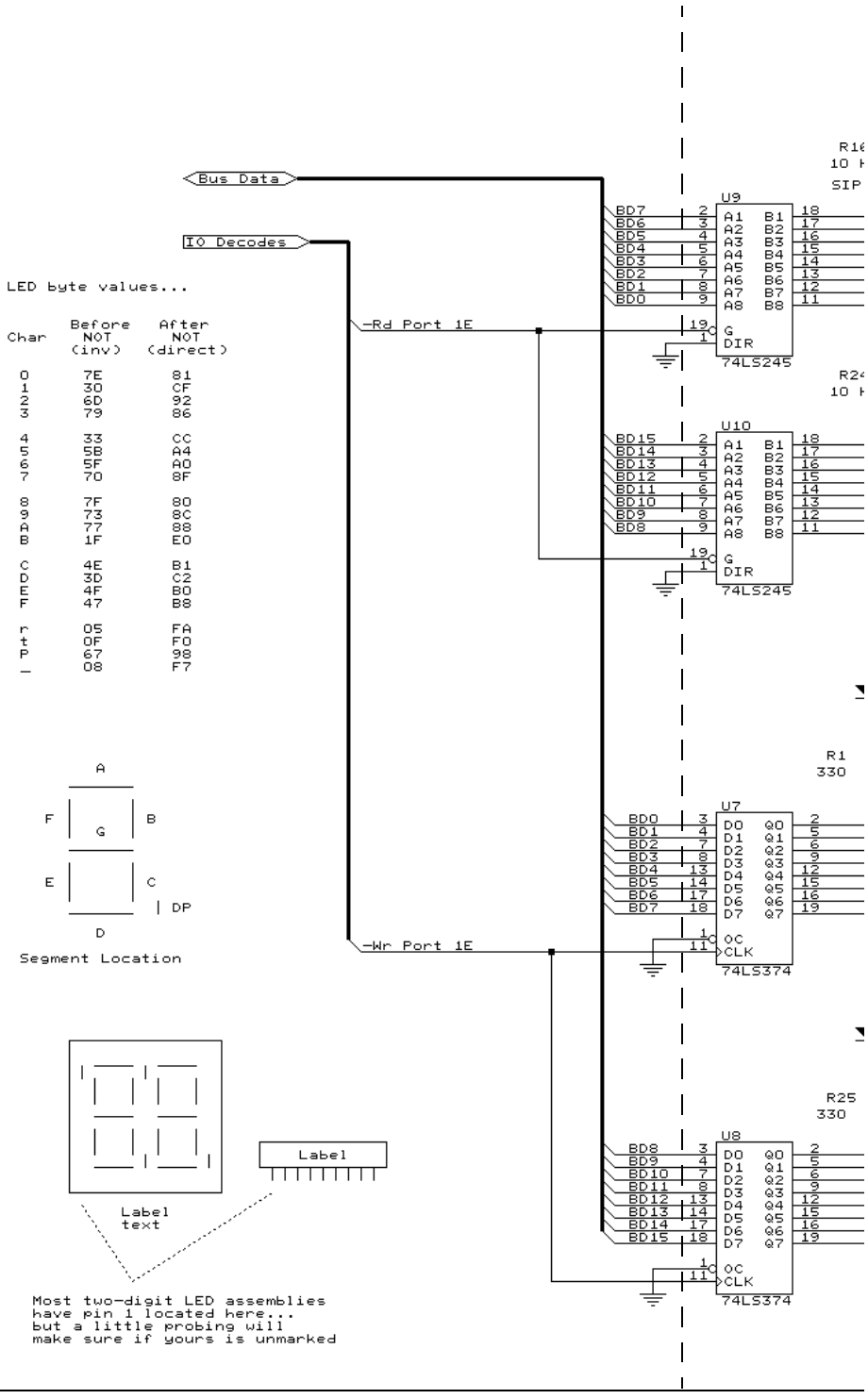
The LCD Refresh RAM address can come from either the LS590 Address Counters or the ISA bus through the LS245 Address Buffers. The LCD panel sees the RAM output through a latch and multiplexer.

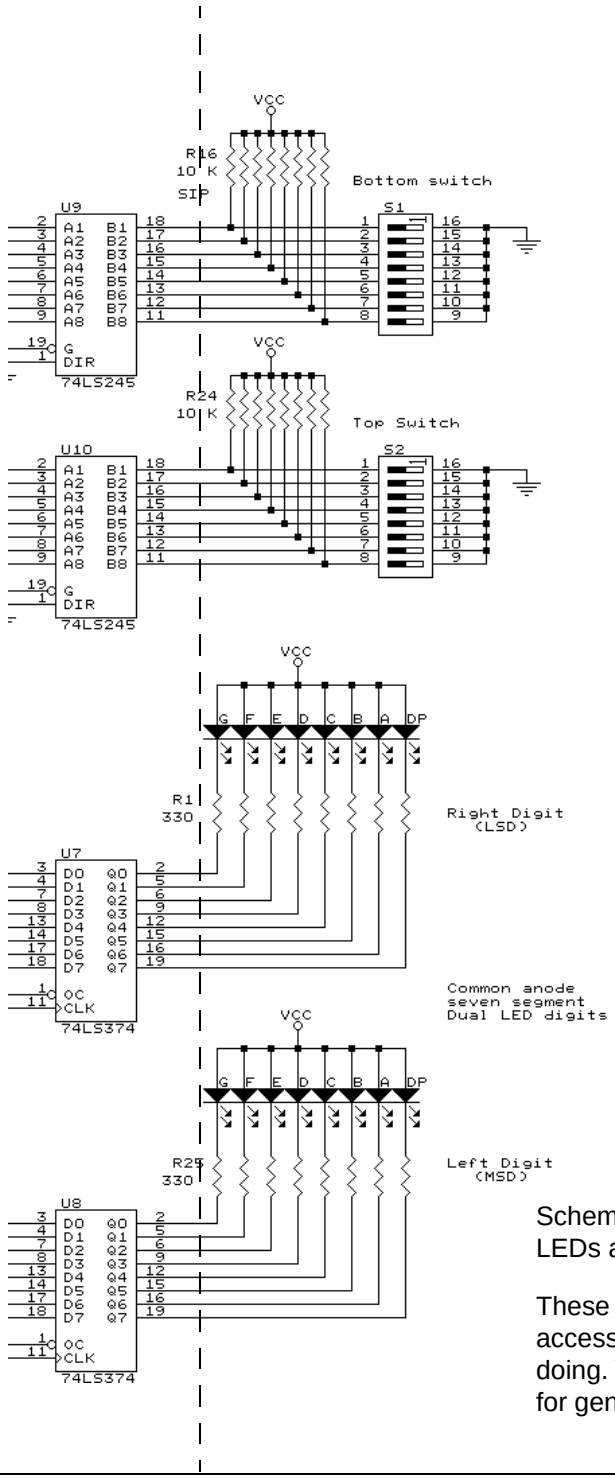

LCD Controls
Frame Counter
JP13
−Frame Sync +0.0
+Frame Sync +0.5
U52
CCLK
CCLKEN
CCLR
RCLK
G
QA
QB
QC
QD
QE
QF
QG
QH
RCO
74LS590
VCC
15 Alternate Frame
1 1/16
2 1/8
3 1/4
4 1/2
5 1 sec
6 2 sec
7 4 sec
9
Blink
−LCD Clock
Blink Rate 0
Blink Rate 1
Blink Rate 2
Choose blink range
to suit your panel
+Frame Sync +0.5
+2x Frame Sync
JP10
+Line Sync +0.0
+2x Line Sync
JP11
−Dot Clock / 2
+Dot Clock
−2x Dot Clock
JP12
U19G
1/8
Alternate Frame
+Enable Display
LCD D0/b
LCD D1/b
LCD D2/b
LCD D3/b
Bus Controls
+ResDrv
R67
10 K
Q1
2N2907A
K1
Bridge is
100 PRV 1A
DIP package
or discrete
1N4001 diodes
D23
1N4001
D22
U55
LM337T
VIN
VOUT
ADJ
P1
24 VAC
PHONE PLUG
−37 V DC
C11
200 uF/50VDC
C6
100 nF
R64
120
R65
2 K Pot
R68
680
C8
100 nF
C7
10 uF/35 V
Connect all LCD a
to board ground p



Schematic 11
Graphic LCD Power & Connections

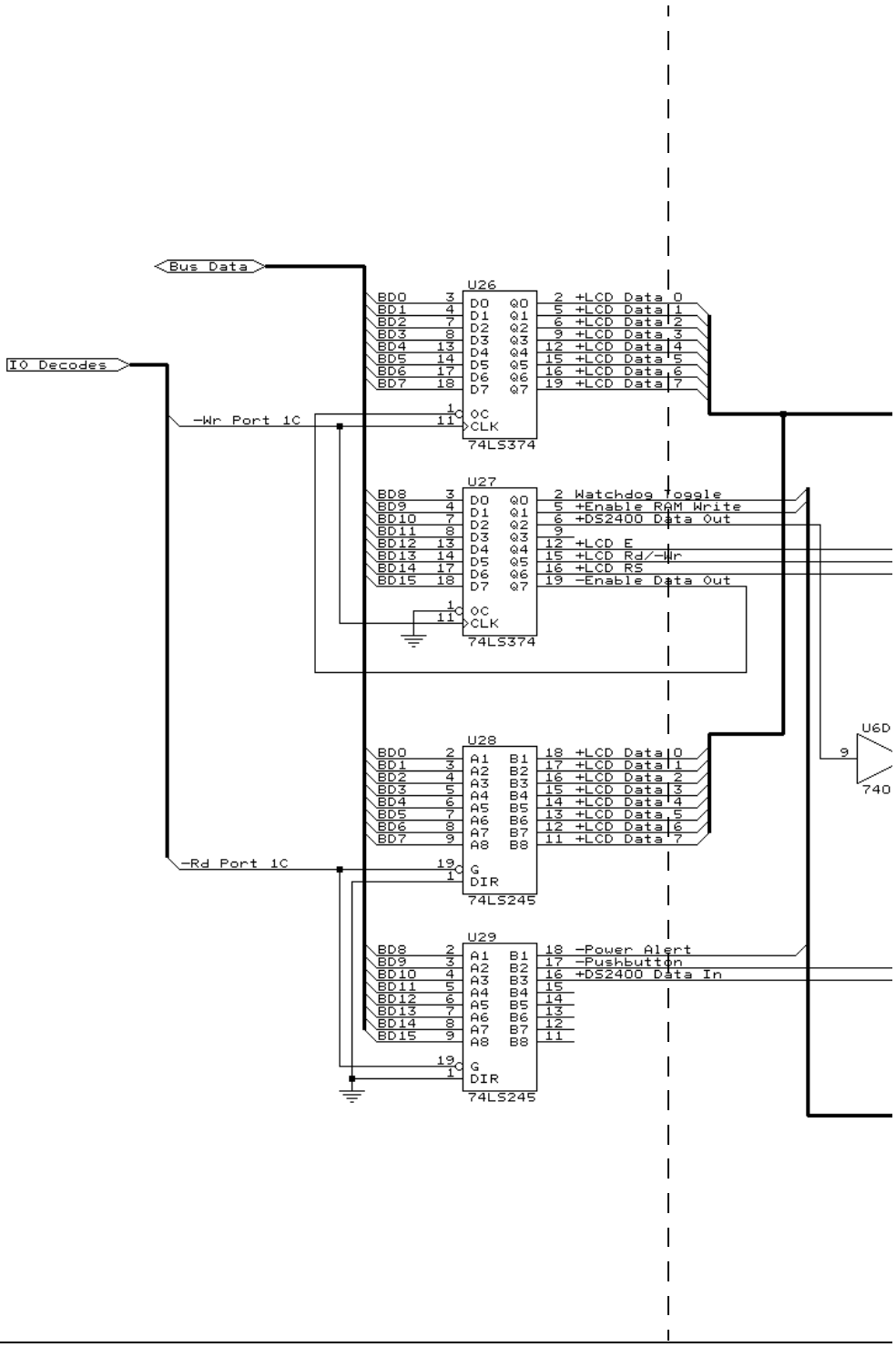
The power supply can handle a wide variety of panels and supply a fatal overvoltage if improperly adjusted. The LCD Connector does not match any panel I've seen!

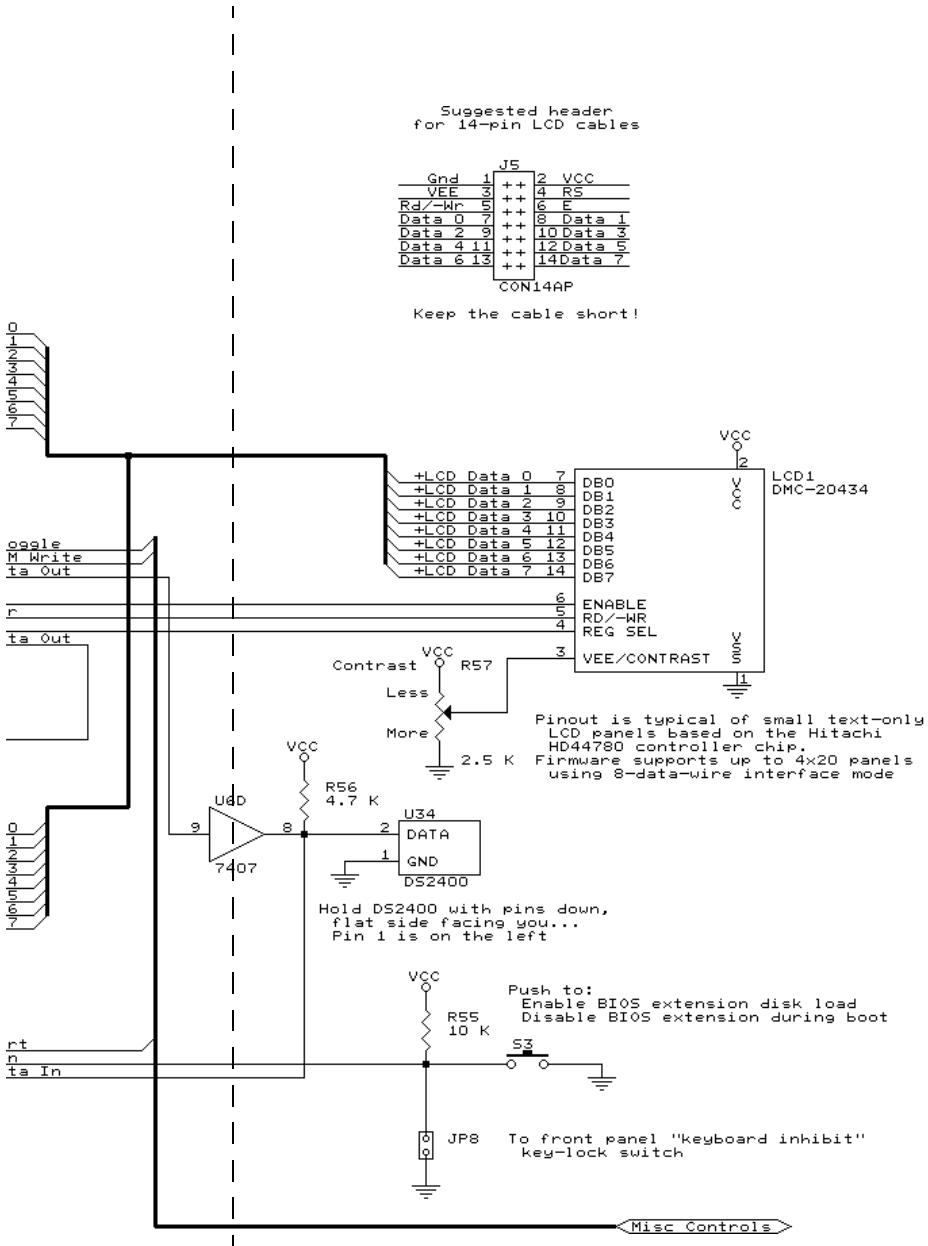

Bus Data
IO Decodes
LED byte values...
Char | Before NOT (inv) | After NOT (direct)
0 7E 81
1 30 CF
2 6D 92
3 79 86
4 33 CC
5 5B A4
6 5F A0
7 70 8F
8 7F 80
9 73 8C
A 77 88
B 1F E0
C 4E B1
D 3D C2
E 4F B0
F 47 B8
r 05 FA
t 0F F0
P 67 98
_ 08 F7
A
F
B
G
E
C
DP
D
Segment Location
Label
Label text
Most two-digit LED assemblies have pin 1 located here... but a little probing will make sure if yours is unmarked
-Rd Port 1E
-Wr Port 1E
U9
U10
U7
U8
74LS245
74LS374
R1
330
R25
330
SIP



Schematic 12
LEDs and DIP Switches

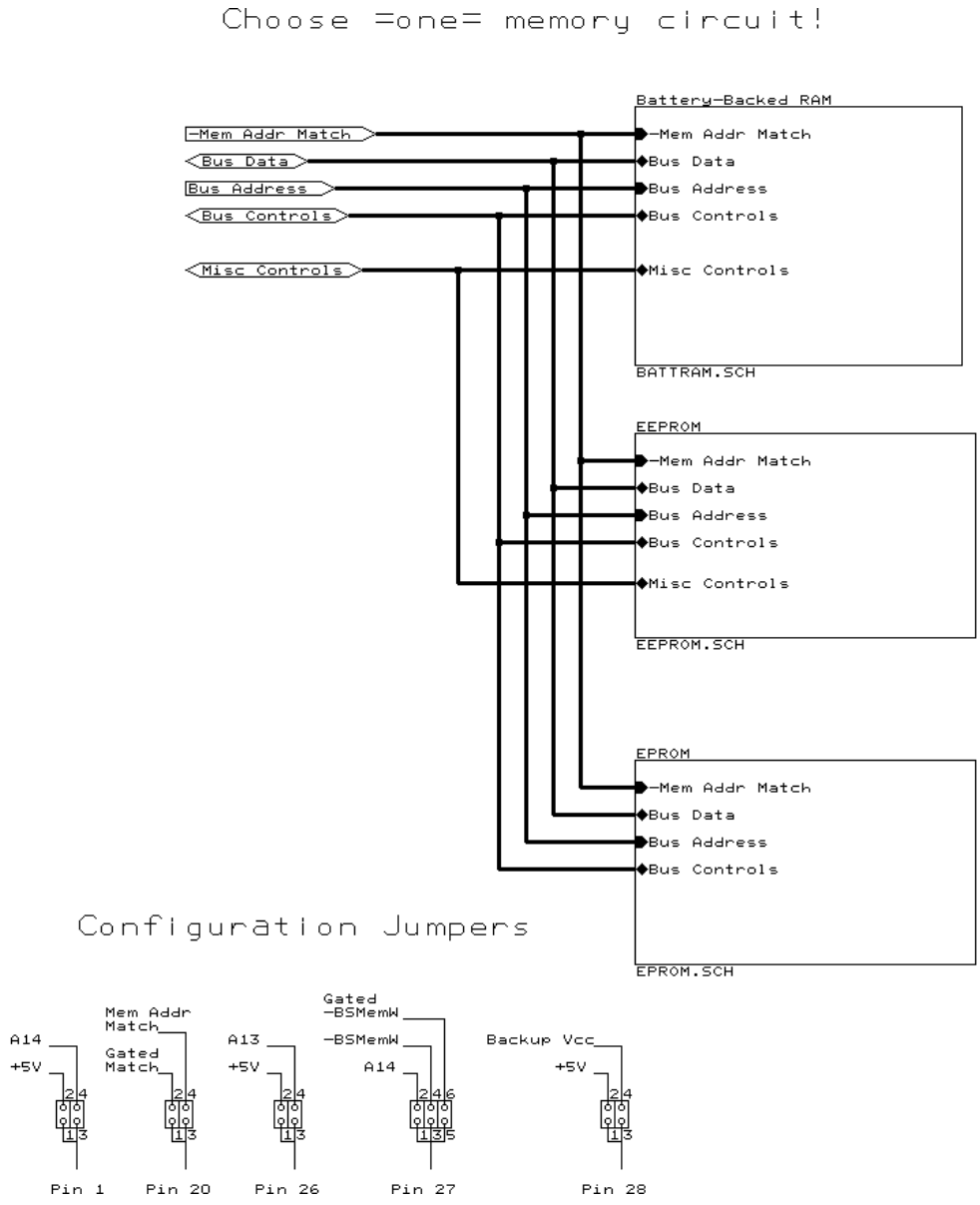
These simple circuits provide convenient access to the firmware and show what it's doing. You can easily modify this circuitry for general bit input and output.

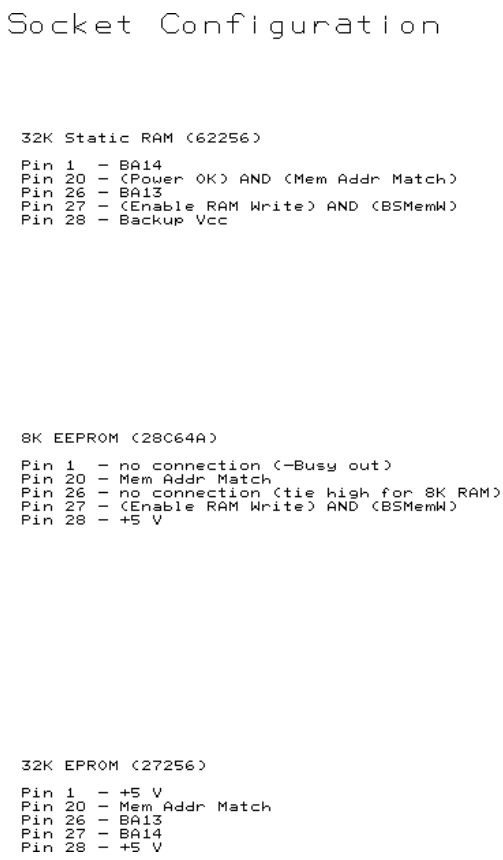

Bus Data
IO Decodes
-Wr Port 1C
-Rd Port 1C
U26
74LS374
U27
74LS374
U28
74LS245
U29
74LS245
U6D
74O
+LCD Data 0
+LCD Data 1
+LCD Data 2
+LCD Data 3
+LCD Data 4
+LCD Data 5
+LCD Data 6
+LCD Data 7
Watchdog Toggle
+Enable RAM Write
+DS2400 Data Out
+LCD E
+LCD Rd/-Wr
+LCD RS
-Enable Data Out
-Power Alert
-Pushbutton
+DS2400 Data In



Schematic 13
Character LCD and I/O bits

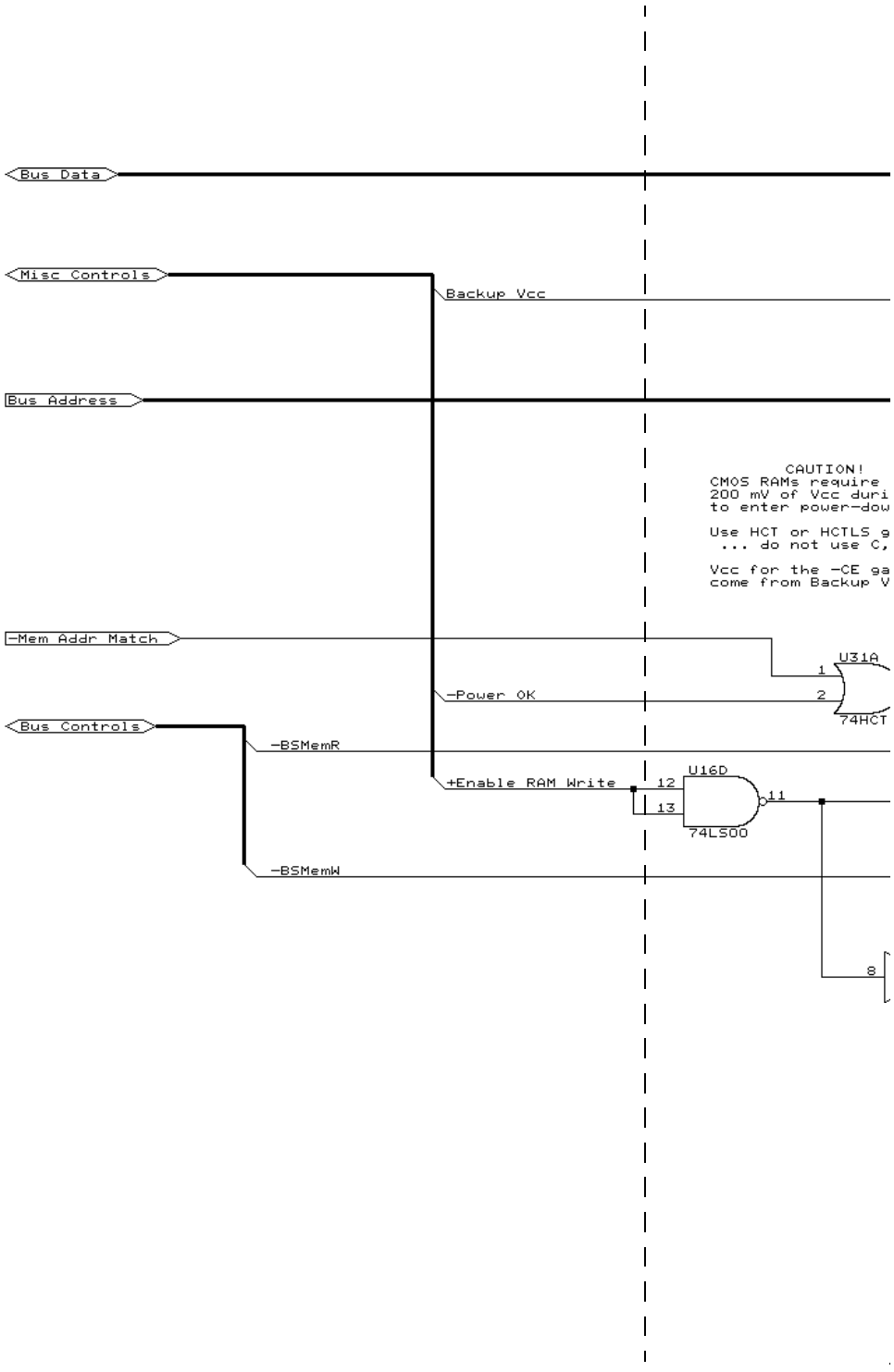
A small text LCD panel can be a useful output device for many systems. This I/O port design eliminates the need for a direct ISA bus connection with all its timing complexities.

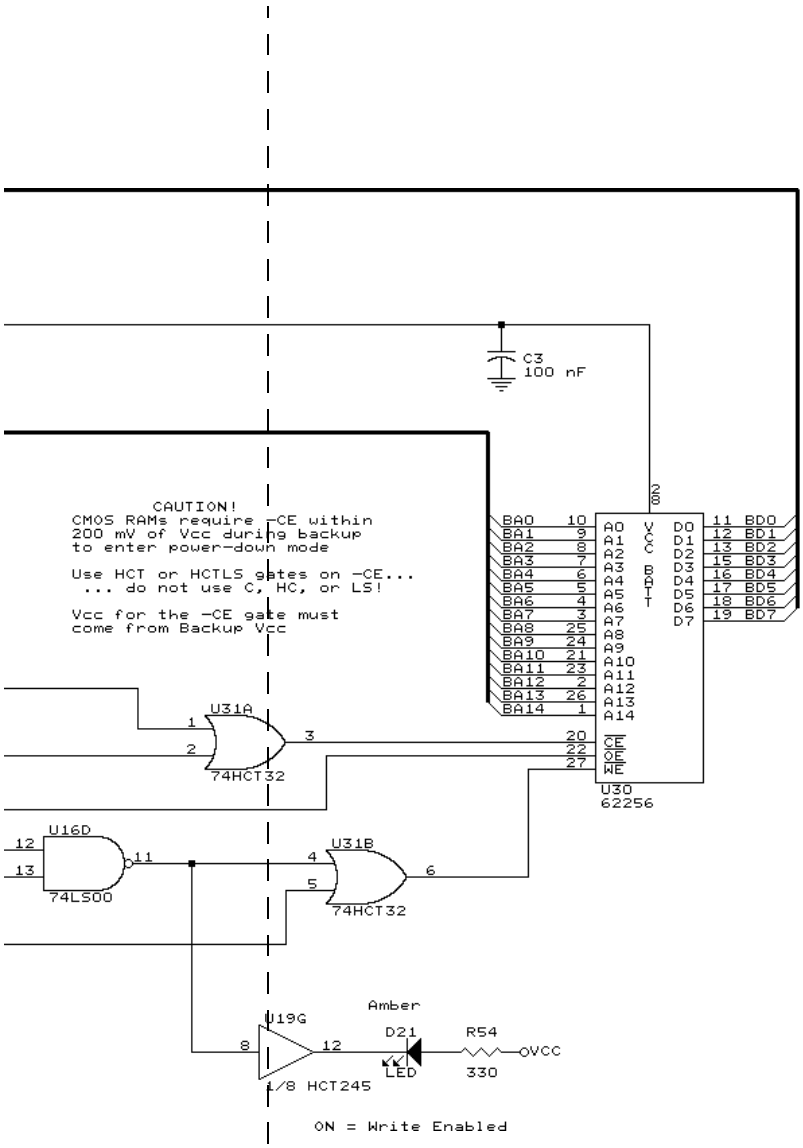

Choose =one= memory circuit!
Battery-Backed RAM
-Mem Addr Match
Bus Data
Bus Address
Bus Controls
Misc Controls
BATTRAM.SCH
EEPROM
EEPROM.SCH
EPROM
EPROM.SCH
Configuration Jumpers
A14
+5V
Mem Addr Match
Gated Match
A13
Gated -BSMemW
-BSMemW
Backup Vcc
Pin 1
Pin 20
Pin 26
Pin 27
Pin 28



Schematic 14
Memory Options

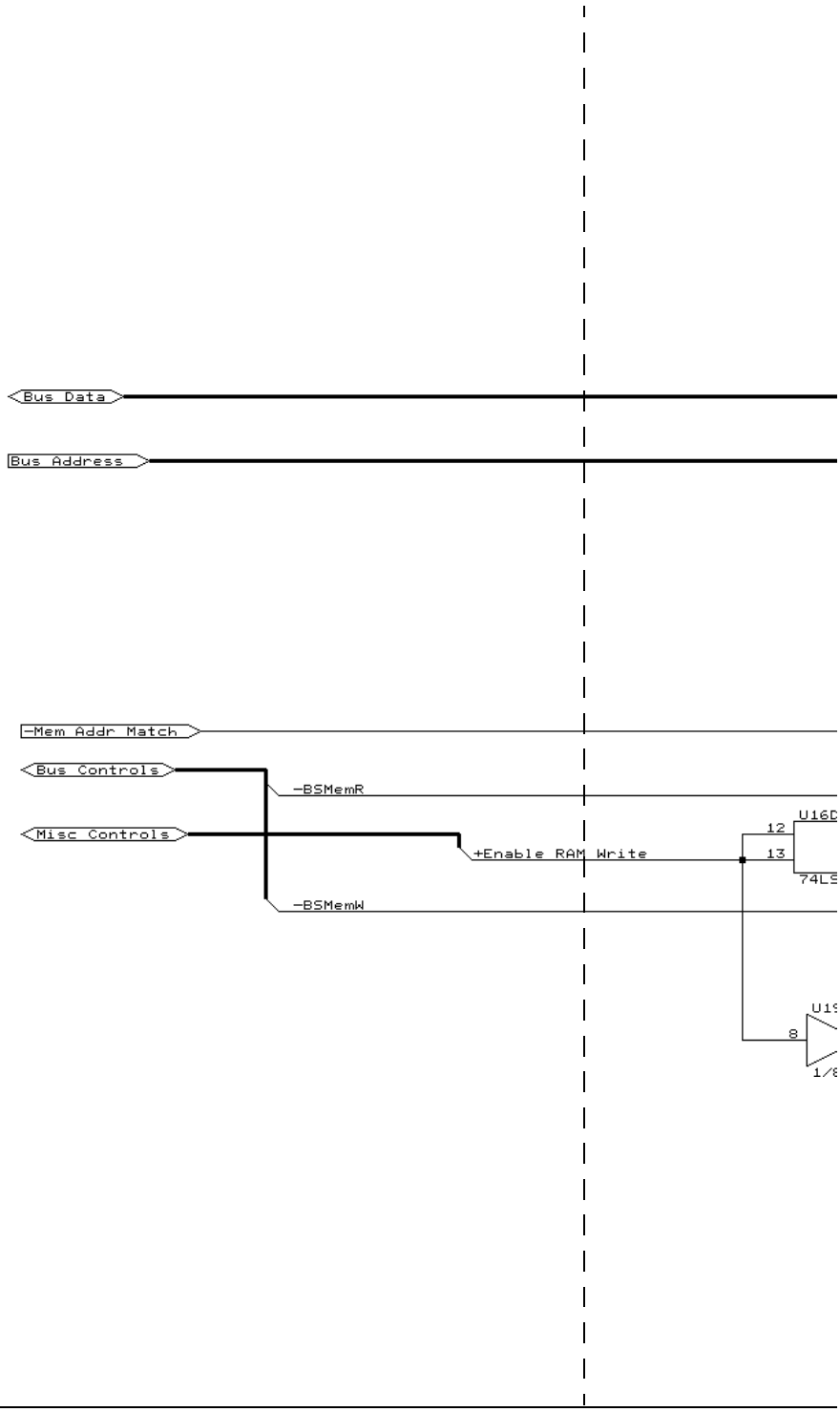
The Firmware Development Board can support nonvolatile memory with EPROM, EEPROM, or battery backed RAM. This schematic shows the various connections and jumper options.

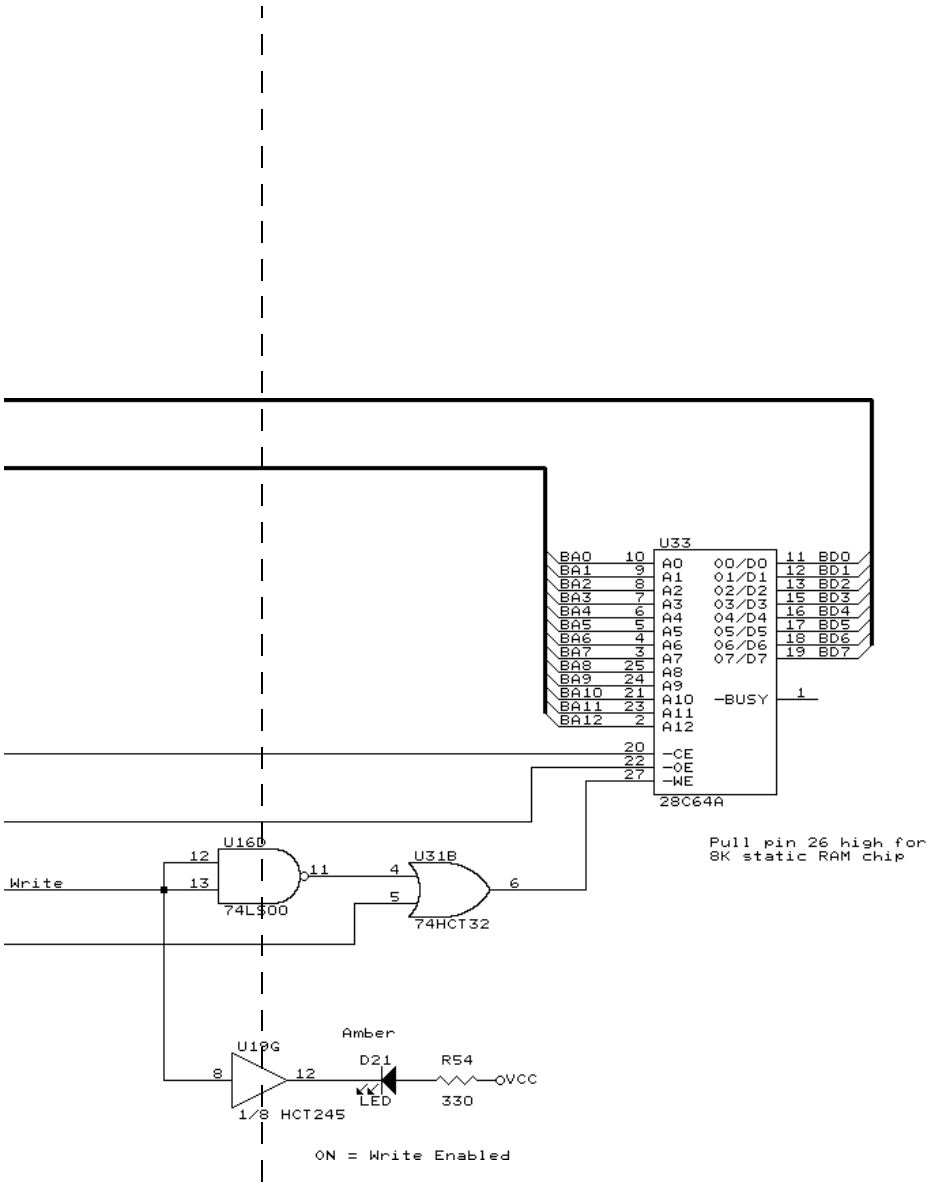

Bus Data
Misc Controls
Backup Vcc
Bus Address
CAUTION!
CMOS RAMs require
200 mV of Vcc duri
to enter power-dow
Use HCT or HCTLS g
... do not use C,
Vcc for the -CE ga
come from Backup V
-Mem Addr Match
U31A
1
-Power OK
2
74HCT
Bus Controls
-BSMemR
U16D
+Enable RAM Write
12
13
11
74LS00
-BSMemW
8



Schematic 15
Battery backed RAM

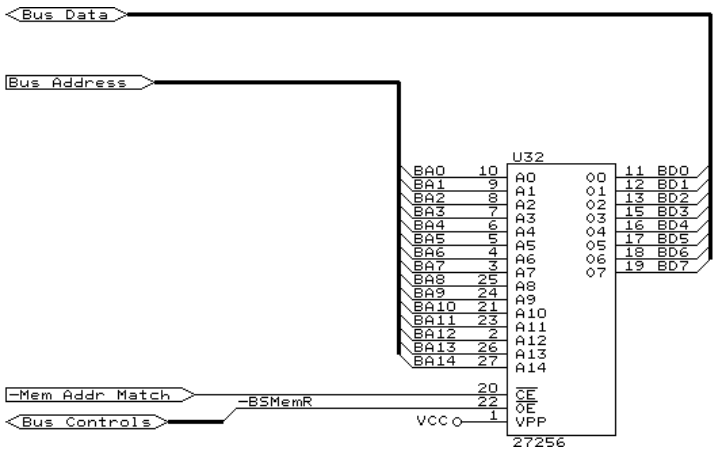
The MAX691 you saw earlier controls the Backup Vcc that drives this RAM and HCT32 gate. The RAM is normally write protected to prevent accidental data changes.


Bus Data
Bus Address
-Mem Addr Match
Bus Controls
-BSMemR
Misc Controls
+Enable RAM Write
12
13
74LS
-BSMemW
8



Schematic 16
EEPROM

Firmware polling determines the write cycle duration for this EEPROM. This chip must also have write protection to prevent accidental changes.



Schematic 17
EPROM

This is about as simple as a memory can get, even if the address and data buffers did appear on previous pages. You obviously don't need any write protection for an EPROM!

Port Addresses

You will find all of the Firmware Development Board I/O port addresses and bits defined in `\ISAbus\Code\Micro-C\FirmDev.h`.

U14, the 74F521 address comparator, decodes all I/O addresses from 0300 through 031F, even if the board doesn't actually have any hardware at a particular address. The Firmware Development Board hardware uses these I/O addresses.

Port	Read	Write
0308	Timer 0 Count/Status	Timer 0 Count
030A	Timer 1 Count/Status	Timer 1 Count
030C	Timer 2 Count/Status	Timer 2 Count
030E	unused	Timer Control Register
031A	unused	Graphic LCD Controls
031C	Board Status Bits	Board + Text LCD Controls
031E	DIP Switches	LED Digits (7 seg + dec pt)

See Schematic 12 for the bit layout in the two seven-segment LED digits at 031E.

Control and Status Bits

These bits at I/O address 031A control the Graphic LCD Interface. Because the interface is write only, there are no corresponding Status bits:

Bit	Write Function
7	unused
6 - 4	Blinking MUX selection
3	unused
2	Enable LCD Panel
1	Disable Blinking MUX
0	Enable Address Counters

These bits at I/O address 031C control various functions and report status conditions throughout the board:

Bit	Read Status	Write Function
15	unused	-Enable Data to Char LCD
14	unused	+RS to Character LCD
13	unused	+Rd/-Wr to Character LCD
12	unused	+E to Character LCD
11	unused	unused
10	+DS2400 Data In	+DS2400 Data Out
9	-Pushbutton	+Enable FDB RAM Write
8	-Power Alert from MAX691	Watchdog Toggle to MAX691
7 - 0	Data from Character LCD	Data to Character LCD

Memory Addresses

The Firmware Development Board occupies two distinct blocks of the CPU's memory address space, as defined by the jumper settings for U22 and U36. The settings used throughout the book are defined in `\ISAbus\Code\Micro-C\FirmDev.h`:

Address	Function
C800:0000 - C800:7FFF	(E)EPROM or RAM
D000:0000 - D000:7FFF	Graphic LCD Refresh RAM

Bill of Materials

This list includes the parts required for the Firmware Development Board, with the exception of the prototyping board itself and sundries such as sockets, jumpers, bypass caps, and so forth, all of which depend on how you plan to construct the hardware.

Remember those bypass capacitors! Although the ISA bus circuitry doesn't run at warp speed, you must still pay attention to your construction techniques. A prototype board with solid power planes will work much better than daisy chained Wire-Wrap links.

The EEPROM, EPROM, and battery backed RAM share common circuits, so you won't need quite as many parts as you see on those pages. Decide which versions you'll build and plan accordingly.

Most of the LEDs appear in the two seven-segment digits in Schematic 12, which doesn't show their reference numbers. The remainder, all discrete LEDs, are scattered over the board to indicate key logic states.

Item	Quan	Ref	Description
1	1	BT1	3V Lithium
2	2	C1	47 pF
		C5	47 pF
3	1	C2	1 nF
4	4	C3	100 nF
		C6	100 nF
		C8	100 nF
		C9	100 nF
5	1	C4	1-10 nF
6	2	C7	10 uF/35 V
		C10	10 uF/35 V
7	1	C11	200 uF/50VDC
8	21	D1	LED
		D2	LED
		D3	LED
		D4	LED
		D5	LED
		D6	LED
		D7	LED
		D8	LED
		D9	LED
		D10	LED
		D11	LED
		D12	LED
		D13	LED
		D14	LED
		D15	LED
		D16	LED
		D18	LED
		D19	LED
		D20	LED
		D21	LED
9	1	D17	1N4148
10	1	D22	BRIDGE
11	1	D23	1N4001
12	4	JP_1	JMP 2X2
		JP_20	JMP 2X2
		JP_26	JMP 2X2
		JP_28	JMP 2X2
13	1	JP_27	JMP 2X3
14	3	JP1	HEADER 5X2
		JP6	HEADER 5X2
		JP9	HEADER 5X2
15	5	JP2	JMP
		JP3	JMP
		JP5	JMP
		JP7	JMP
		JP8	JMP
16	3	JP10	3 HEADER
		JP11	3 HEADER
		JP13	3 HEADER
17	1	JP12	HEADER 3X2
18	1	J1	CON AT62B
19	1	J2	CON AT36B
20	2	J3	CON2
		J4	CON2
21	1	J5	CON14AP
22	1	J6	CON26A
23	1	K1	RELAY DPDT
24	1	LCD1	DMC-20434
25	1	P1	PHONE PLUG
26	1	Q1	2N2907A
27	35	R1	330
		R2	330
		R3	330
		R4	330
		R5	330
		R6	330
		R7	330
		R8	330
		R9	330
		R10	330
		R11	330
		R12	330
		R13	330
		R14	330
		R15	330
		R17	330
		R18	330
		R19	330
		R20	330
		R21	330
		R22	330
		R23	330
		R25	330
		R26	330
		R27	330
		R28	330
		R29	330
		R30	330
		R31	330
		R32	330
		R47	330
		R48	330
		R49	330
		R54	330
28	7	R16	10 K
		R24	10 K
		R38	10 K
		R53	10 K
		R55	10 K
		R66	10 K
		R67	10 K
29	6	R33	4.7 K
		R34	4.7 K
		R35	4.7 K
		R36	4.7 K
		R37	4.7 K
		R56	4.7 K
30	1	R39	25 K
31	1	R40	2.7 K
32	10	R41	R
		R42	R
		R43	R
		R44	R
		R45	R
		R58	R
		R59	R
		R60	R
		R61	R
		R62	R
33	1	R46	560
34	2	R50	2.5 K
		R57	2.5 K
35	1	R51	45 K
36	1	R52	15 K
37	1	R63	100
38	1	R64	120

Item	Quan	Ref	Description
39	1	R65	2 K Pot
40	1	R68	680
41	2	S1	SW DIP-8
		S2	SW DIP-8
42	1	S3	SW PUSHBUTTON
43	14	U1	74LS245
		U2	74LS245
		U3	74LS245
		U4	74LS245
		U5	74LS245
		U9	74LS245
		U10	74LS245
		U20	74LS245
		U21	74LS245
		U28	74LS245
		U29	74LS245
		U46	74LS245
		U47	74LS245
		U49	74LS245
44	1	U6	7407
45	5	U7	74LS374
		U8	74LS374
		U26	74LS374
		U27	74LS374
		U48	74LS374
46	3	U11	74LS139
		U41	74LS139
		U56	74LS139
47	2	U12	74LS138
		U13	74LS138
48	3	U14	74F521
		U22	74F521
		U36	74F521
49	1	U15	74LS221
50	2	U16	74LS00
		U40	74LS00
51	1	U17	82C54
52	2	U18	74LS74
		U39	74LS74
53	1	U19	1/8 HCT245
54	1	U24	MAX691
55	2	U30	62256
		U45	62256
56	1	U31	74HCT32
57	1	U32	27256
58	1	U33	28C64A
59	1	U34	DS2400
60	1	U35	74LS08
61	3	U37	74HCT74
		U39	74HCT74
		U42	74HCT74
62	1	U38	74LS109
63	3	U43	74LS590
		U44	74LS590
		U52	74LS590
64	1	U50	74LS32
65	2	U57	74HCT374
		U51	74HCT374
66	1	U53	74LS151
67	1	U54	74HCT157
68	1	U55	LM337T